
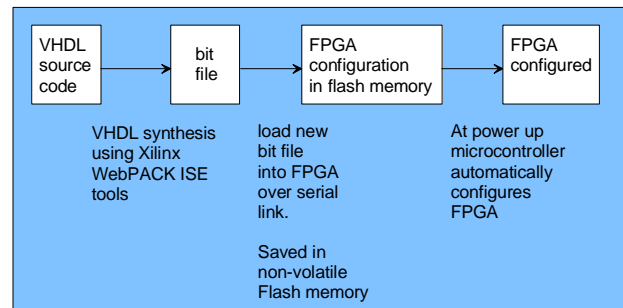


Key Features

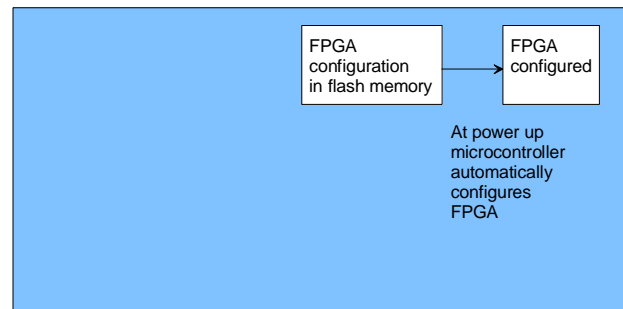
- Develop custom signal processing applications on FPGA using this generic development platform.
- Xilinx Spartan-II XC2S200 FPGA features 200,000 system gates, including 57Kbit of dual port memory.
- Free VHDL development tools available from Xilinx (WebPACK ISE).
- Modules can be stacked for larger designs development.
- FPGA configuration remains in non-volatile flash memory and is automatically reloaded at power up.
- User-friendly utilities for remote monitoring and control over simple serial link. This includes loading FPGA configuration file (.mcs) into flash.
- This module is interface compatible with other pre-programmed ComBlock modules.
- 40 MHz internal clock rate. External clock selection.
-  **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Single 5V supply with reverse voltage and overvoltage protection. Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom). Interfaces with 5V and 3.3V logic.



Application Development Process



Development environment.



Run-time environment.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1000.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm.

Electrical Interface

Interfaces	Definition
J2(29:2)	J2 connector (left)
J3(29:1)	J2 connector (right)
J4(29:1)	J2 connector (bottom)
TEST_POINTS(10:1)	Ten test points are provided for easy access by an oscilloscope probe.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 300mA.

Development tools

Free VHDL development tools entitled WebPACK ISE are available from Xilinx. These tools are available for download after registration at <http://www.xilinx.com/support/download.htm>.

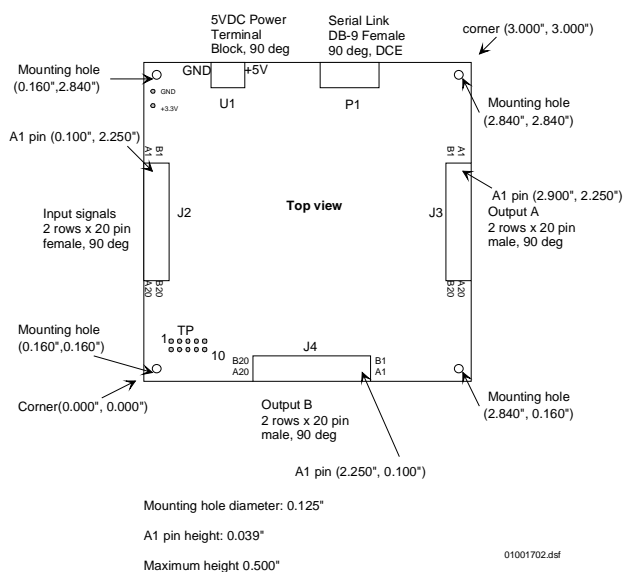
VHDL code samples

VHDL project samples are available on-line at http://www.comblock.com/download/com1000template_002.zip.

Each project includes:

- the VHDL source code (.vhd)
- the constraint file (.ucf) listing all pin assignments.
- The Xilinx project with the synthesis and implementation settings.
- The resulting bit file (.mcs) ready to be loaded into flash memory.

Mechanical Interface



The sample code describes how the application interfaces with the ComBlock Control Center graphical user interface through control and monitoring registers. The ComBlock Control user manual is available at

www.comblock.com/download/cchelp.pdf

It also describes how to capture key internal signals in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.

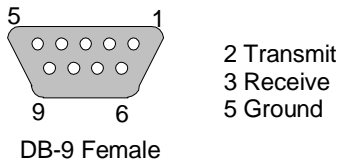
Schematics

The board schematics are available on-line at www.ComBlock.com/download/com_1000schematics.pdf.

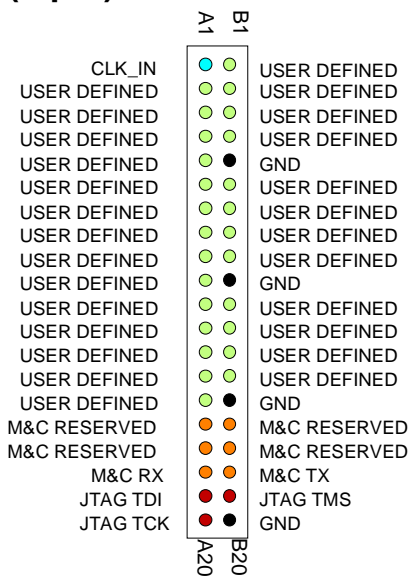
Pinout

Serial Link P1

The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.

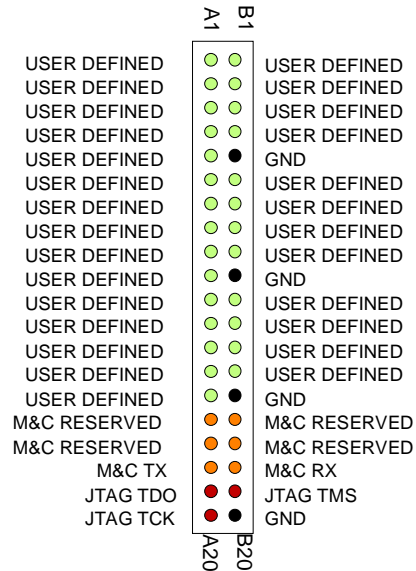


(Input) Connector J2



Note: although the J2 connector is generally referred to as 'Input', individual user-defined pins can be configured as 'IN', 'OUT', or 'INOUT' in the user VHDL source code.

(Output) Connectors J3, J4



Note: although the J3 and J4 connectors are generally referred to as 'Output, individual user-defined pins can be configured as 'IN', 'OUT', or 'INOUT' in the user VHDL source code.

Configuration Management

This specification is to be used in conjunction with VHDL code template software revision 2, and the ComBlock Control Center revision 2.31 or above.

ComBlock Ordering Information

COM-1000 FPGA / VHDL development platform

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