



COM-1001 BPSK/QPSK/OQPSK DEMODULATOR VHDL SOURCE CODE OVERVIEW

Overview

The COM-1001 ComBlock Module comprises two pieces of software:

- VHDL code to run within the FPGA for all signal processing functions.
- C/Assembly code running within the Atmel ATmega8515L microprocessor for non application-specific monitoring and control functions.

The VHDL code interfaces to the monitoring and control functions by exchanging byte-wide registers on the Atmel microcontroller 8-bit data bus. The control and monitoring registers are defined in the specifications [1].

The Atmel microprocessor code is generic (i.e. non application specific), not user-programmable and functionally transparent to the user. It is thus not described here.

The COM-1001 VHDL code runs on the generic COM-1000 hardware platform. The schematics [2] for this platform are available in this CD.

Reference documents

- [1] specifications: com1001.pdf
- [2] hardware schematics: com_1000schematics.pdf
- [3] VHDL source code in directory com-1001_027/src
- [4] .ucf constraint file com-1001_027/src/root_demod.ucf
- [5] .mcs FPGA bit files com-1001_027\com1001B_027.mcs com-1001_027\com1001E_027.mcs

Configuration Management

The current software revision is 27.

Configuration Options

In order to provide configuration flexibility without unduly increasing the hardware complexity, some features require generating different firmware versions. In particular, the channel filter (root raised cosine square root) rolloff can take four distinct values: 20%, 25% and 40%.

Three versions of the *raised_cos4x* root raised filters are included in the source code .src directory. To change the filter:

- (a) change the OPTION constant in the *root_demod.vhd* file so that the resulting bit file can later be correctly identified.
- (b) Change the RAISED_COS4x statements in three places within the *demod.vhd* file: declaration and two instantiations.

VHDL development environment

The VHDL software was developed using the Xilinx ISE 4.1 development environment. The synthesis tool is FPGA Express 3.6.

Target FPGA

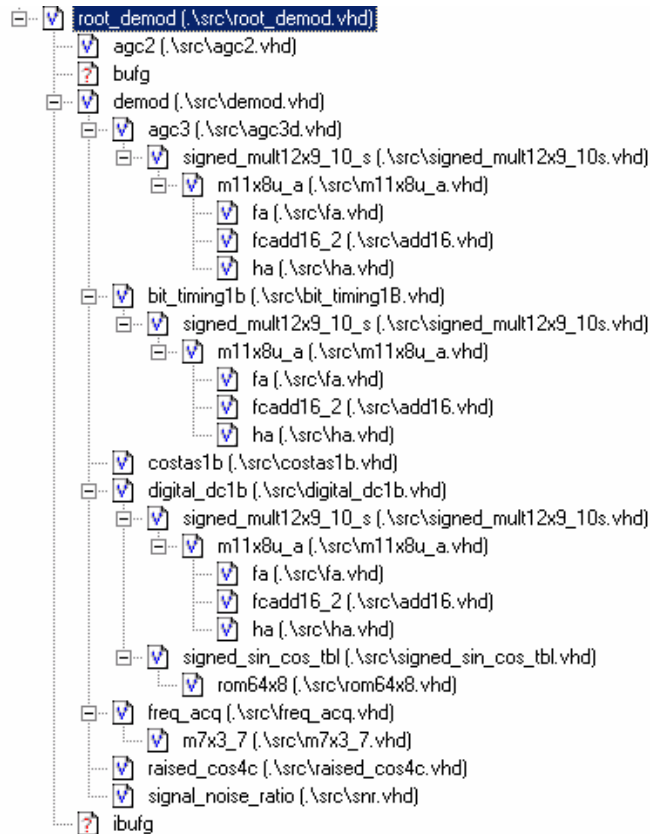
The VHDL code was synthesized for the Xilinx Spartan-II XC2S200-5PQ208 FPGA.

Xilinx-specific code

The VHDL source code was written in generic VHDL with few Xilinx primitives. No Xilinx CORE is used. The Xilinx primitives are:

- BUFG
- IBUFG

VHDL software hierarchy



The code is stored with one, and only one, entity per file as shown above.

The root program (highlighted) is *root_demod.vhd*.

Clock / Timing

All signal processing, inputs and outputs are synchronous with the external 40 MHz clock supplied on CLK_IN2.

Block Diagram

The hierarchical nature of the VHDL code reflects the block diagram below:

- *root_demod* is the root program which includes the demodulator *demod*, the analog AGC *agc2* to prevent saturation at the external A/D converters and ancillary functions such as monitoring and control functions (interface with microprocessor).
- the main BPSK/QPSK functions are encapsulated within *demod*.

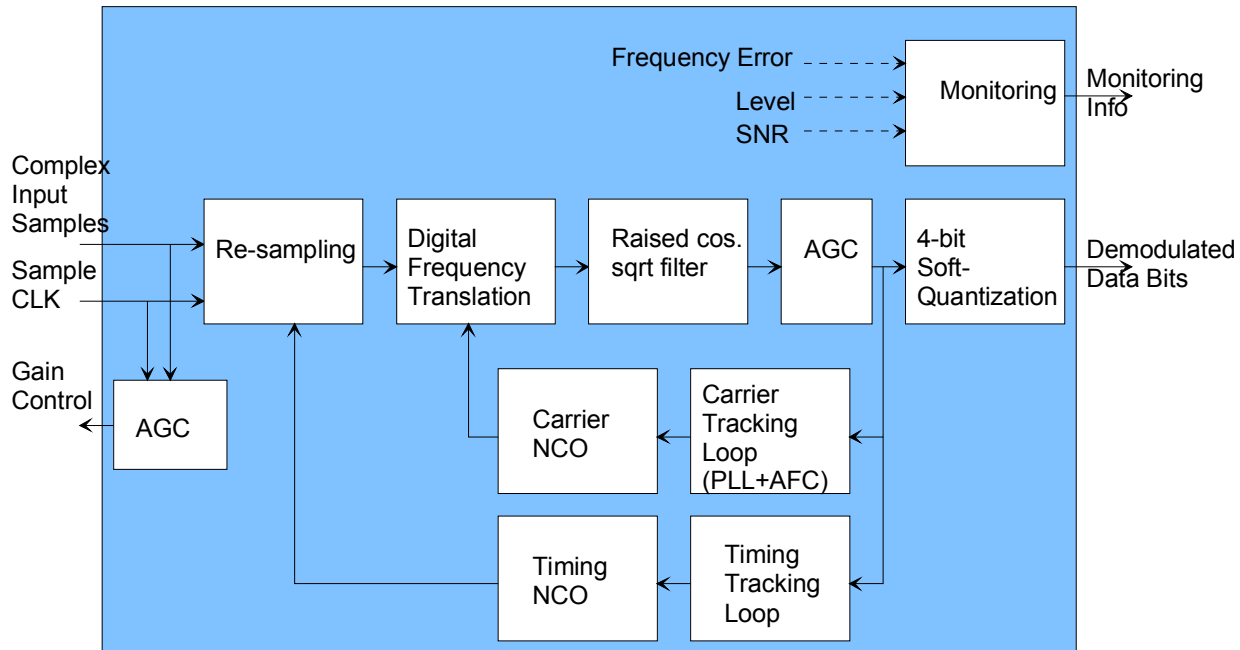
- the frequency translation is implemented within *digital_dc1b*. The frequency translation is realized in the form of a complex vector rotation, using sine/cosine lookup tables (*signed_sin_cos_tbl*) and pipeline multipliers (*signed_mult12x9_10_s*) made of half adders *ha* and full adders *fa*.
- channel filtering is made by means of two root raised cosine filters *raised_cos4c*, one for each complex axis.
- Bit timing recovery is implemented in the *bit_timing1b* component. The bit timing is a classic Gardner loop: It works on (I,Q) input signals sampled at twice the symbol rate. The input signals are taken after center frequency compensation, root raised cosine filtering and AGC. One first computes the timing error as follows: $(I_{j-1/2} * (I_j - I_{j-1})) + (Q_{j-1/2} * (Q_j - Q_{j-1}))$ where $I_{j-1/2}$ denotes a half symbol offset with respect to sample I_j . When the loop is tracking, $I_{j-1/2}$ is at the center of the symbol (optimum sampling instant) and I_j and I_{j-1} are at the time of bit transition. When averaged over all data bit patterns, $(I_j - I_{j-1})$ is zero when the loop is tracking. Because the bit timing errors are usually small (200ppm max due to crystal frequency offsets), the bit timing loop is a first order loop. The bit timing error is scaled to control the bit timing NCO around the nominal value. (no accumulation, no integration, just a simple first order loop). The bit timing NCO controls the resampling of the input samples at the demodulator input. Prior to the resampling (decimation), the input samples are first subject to a simple x2 interpolation so that the granularity of the resampling is at most 1/8th of a symbol. The bit timing NCO is part of the *demod* entity.
- A digital AGC *agc3* is used to normalize the despread signal and to condition the resulting signal in a variety of formats: 4-bit unsigned (soft-quantization), 8-bit signed (for carrier tracking loop processing).
- Most carrier acquisition, carrier tracking and AFC functions are implemented within the *costas* entity. The Costas carrier tracking loop is a second-order loop which

cancels the average phase error and the average frequency error when tracking. The actual carrier NCO is part of the *demod* entity.

samples around the noiseless 1111/0000 values. The standard deviation is averaged over 4096 symbols, thus resulting in an accuracy better than 0.6 dB.

- The inverse signal-to-noise ratio is obtained in *snr.vhd* by computing the standard deviation of the 4-bit soft-quantized

Block Diagram



FPGA Occupancy

Design Summary

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Number of errors:      0
Number of warnings:   2
Number of Slices:     2,350 out of 2,352  99%
Number of Slices containing
  unrelated logic:    204 out of 2,350  8%
Number of Slice Flip Flops:  2,998 out of 4,704  63%
Total Number 4 input LUTs:  3,645 out of 4,704  77%
  Number used as LUTs:      3,609
  Number used as a route-thru: 36
Number of bonded IOBs:    72 out of 140  51%
  IOB Flip Flops:          32
Number of GCLKs:          3 out of 4  75%
Number of GCLKIOBs:       1 out of 4  25%
Total equivalent gate count for design: 54,402
Additional JTAG gate count for IOBs: 3,504
  
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Contact Information

MSS • 18221 Flower Hill Way #A •
 Gaithersburg, Maryland 20879 • U.S.A.
 Telephone: (240) 631-1111
 Facsimile: (240) 631-1676
 E-mail: info@comblock.com