COM-1002
BPSK/QPSK/OQPSK MODULATOR
VHDL SOURCE CODE OVERVIEW

Overview

The COM-1002 ComBlock Module comprises two pieces of software:

- VHDL code to run within the FPGA for all signal processing functions.
- C/Assembly code running within the Atmel ATMega8515L microprocessor for non application-specific monitoring and control functions.

The VHDL code interfaces to the monitoring and control functions by exchanging byte-wide registers on the Atmel microcontroller 8-bit data bus. The control and monitoring registers are defined in the specifications [1].

The Atmel microprocessor code is generic (i.e. non application specific), not user-programmable and functionally transparent to the user. It is thus not described here.

The COM-1002 VHDL code runs on the generic COM-1000 hardware platform. The schematics [2] for this platform are available in this CD.

Reference documents

[1] specifications: com1002.pdf

[2] hardware schematics: com_1000schematics.pdf

[3] VHDL source code in directory com-1002_031\src

[4] .ucf constraint file com-1002_031\src\root_mod.ucf

[5] .mcs FPGA bit files
com-1002_031\com1002B_031.mcs
com-1002_031\com1002E_031.mcs

Configuration Management

The current software revision is 31.

Configuration Options

In order to provide configuration flexibility without unduly increasing the hardware complexity, some features require generating different firmware versions. In particular, the channel filter (root raised cosine square root) rolloff can take four distinct values: 20%, 25% and 40%.

Three versions of the *raised_cos4x* root raised filters are included in the source code .src directory. To change the filter:

(a) change the OPTION constant in the *root_mod.vhd* file so that the resulting bit file can later be correctly identified.

(b) Change the RAISED_COS4x statements in three places within the *modulator.vhd* file: declaration and two instantiations.

VHDL development environment

The VHDL software was developed using the Xilinx ISE 4.1 development environment. The synthesis tool is FPGA Express 3.6.

Target FPGA

The VHDL code was synthesized for the Xilinx Spartan-II XC2S200-5PQ208 FPGA.

Xilinx-specific code

The VHDL source code was written in generic VHDL with few Xilinx primitives. No Xilinx CORE is used. The Xilinx primitives are:

- BUFG
- IBUFG
- RAMB4_S16_S16

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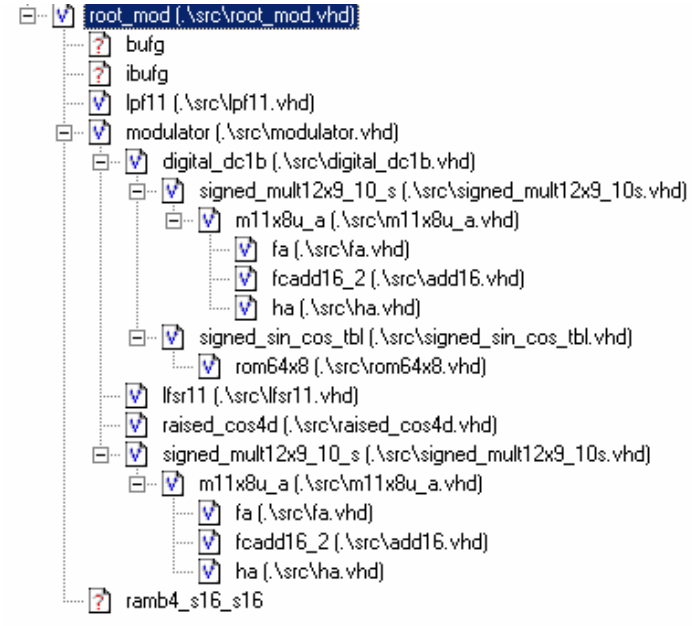
VHDL software hierarchy



The code is stored with one, and only one, entity per file as shown above.

The root program (highlighted) is *root_mod.vhd*.

Clock / Timing

At any given time, the software uses one of two possible clocks:

- An external clock CLK_IN2.
- A 40 MHz internal clock CLK_IN1.

Selection of the internal versus external reference clock depends on the control register REG8 bit 0, under user control. The resulting selected clock is routed through global buffers. It serves as processing clock, output clock and input clock. The external clock should be selected in all cases, except when in test mode (the PRBS-11 pseudo-random sequence is generated internally, there is no external input).

The code is written to meet the timing requirements on the target FPGA at a speed of at least 40 MHz.

Block Diagram

The hierarchical nature of the VHDL code reflects the block diagram below:

- *root_mod* is the root program which includes the modulator *modulator*, the three successive interpolation filters *lpf11* and ancillary functions such as monitoring and control functions (interface with microprocessor).
- the main BPSK/QPSK functions are encapsulated within *modulator*.
- the frequency translation is implemented within *digital_dc1b*. The frequency translation is realized in the form of a complex vector rotation, using sine/cosine lookup tables (*signed_sin_cos_tbl*) and pipeline multipliers (*signed_mult12x9_10_s*) made of half adders *ha* and full adders *fa*.
- Spectrum shaping is made by means of two root raised cosine filters *raised_cos4x*, one for each complex axis.
- the PRBS-11 pseudo-random test pattern is generated within the *lfsr11* entity.

Monitoring and Control information is exchanged through 8-bit registers mapped on the 8-bit bus as follows:

- 10 control registers at microprocessor address 0 through 9
- 0 monitoring register.

A few registers are also reserved for special functions such as

- serial communication with the other comblocks on each of the four sides (REG254/REG255).
- VHDL code *REVISION* (REG253).
- VHDL code *OPTION* (REG252).

The bus address and data are multiplexed over the same 8-bit data lines. The address is valid when the Address Latch Enable (*UC_ALE*) signal is active high. Read and write cycles are identified by the *UC_RDN* and *UC_WRN* active-low signals respectively. Although the microprocessor is much slower than the FPGA, the Atmel uC timing can be difficult to meet, especially during write cycles because data is removed very shortly after the end of the write cycle when *UC_WRN* goes to '1'. Thus, it is wise to route the *UC_WRN* signal through a global buffer for best timing.

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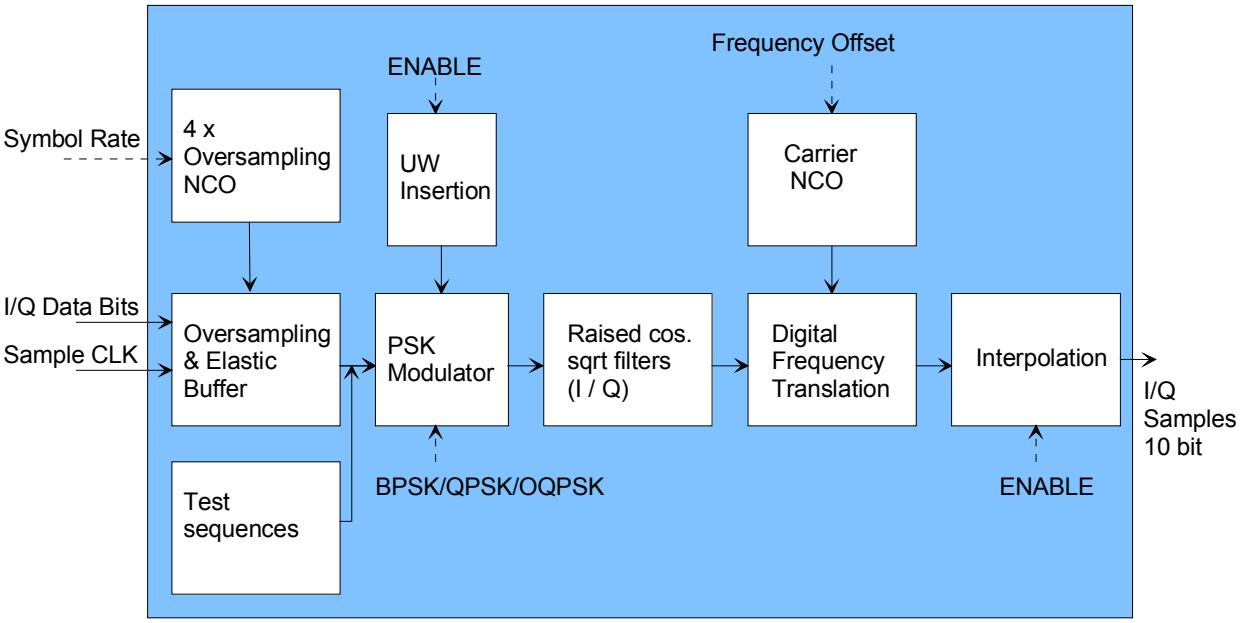
Block Diagram



FPGA Occupancy

```
Design Summary
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   Number of errors:      0
   Number of warnings:   10
   Number of Slices:              2,350 out of  2,352   99%
   Number of Slices containing
      unrelated logic:              293 out of  2,350   12%
   Number of Slice Flip Flops:    3,363 out of  4,704   71%
   Total Number 4 input LUTs:     3,076 out of  4,704   65%
      Number used as LUTs:                   3,055
      Number used as a route-thru:              21
   Number of bonded IOBs:            79 out of    140   56%
      IOB Flip Flops:                           14
   Number of Block RAMs:              2 out of     14   14%
   Number of GCLKs:                   4 out of      4  100%
   Number of GCLKIOBs:                2 out of      4   50%
Total equivalent gate count for design:  84,984
Additional JTAG gate count for IOBs:  3,888
```

Contact Information

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