COM-1012 DIRECT-SEQUENCE SPREAD-SPECTRUM MODULATOR 10 Mchip/s

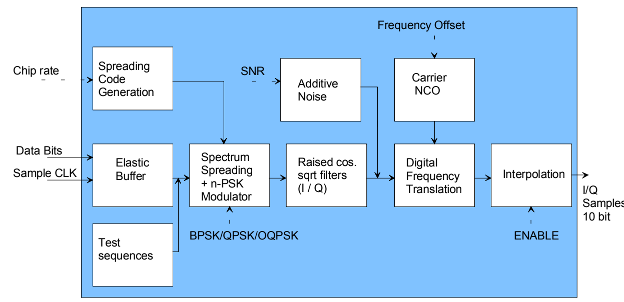
Key Features

- Direct sequence spread-spectrum (DS-SS) modulator.
- Programmable chip rates up to 10 Mchip/s.
- Spreading codes:
    - Gold sequences (up to 2^{23}-1 chips)
    - Maximal length sequences, (max length 2^{23}-1 chips)
    - Barker codes (length 11, 13)
- Code modulation: BPSK/QPSK/OQPSK with output spectral shaping filter: raised cosine square root filter with 20%, 25%, or 40% rolloff.
- Internal generation of PRBS-11 pseudo-random bit stream and unmodulated carrier for test purposes.
- Built-in channel impairments generation:
  - additive white Gaussian noise
  - frequency offset (Doppler)
- Single 5V supply. Connectorized 3"x 3" module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom). Interfaces with 5V and 3.3V logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1012.pdf. These specifications are subject to change without notice.

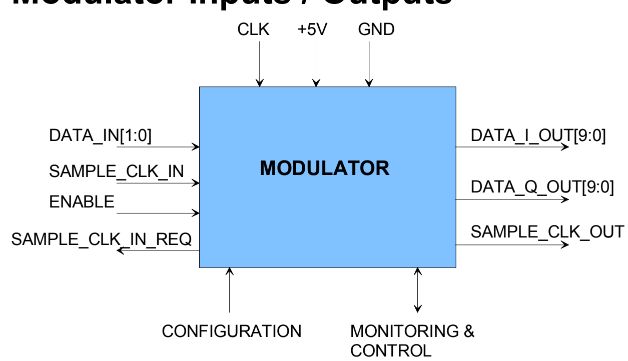
For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

Block Diagram



Electrical Interface

Modulator Inputs / Outputs



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Input Module Interface	Definition
DATA_IN[1:0]	Input data stream. In 1-bit serial mode, use DATA_IN[0] only. In 2-bit parallel mode, DATA_IN[0] is the I data bit DATA_IN[1] is the Q data bit The Q data bit is ignored in BPSK mode.
SAMPLE_CLK_IN	Input data clock. One CLK-wide pulse. Read the input signals at the rising edge of CLK when SAMPLE_CLK_IN = '1'.
ENABLE	Modulator enable input. Internally pulled high. Qualifies the SAMPLE_CLK_IN. Used for burst-mode transmission. In continuous mode, keep at '1'.
SAMPLE_CLK_IN_REQ	One CLK-wide pulse. Requests a sample from the module upstream. For flow-control purposes.
CLK_IN	Input reference clock for synchronous I/O and processing. Yields internal CLK clock. Typically 40 MHz.
Output Module Interface (Output data pushed out)	**Definition**
DATA_I_OUT[9:0]	Modulated output signal, real axis. 10-bit precision. Format: 2's complement or unsigned, selected by configuration bit 1.
DATA_Q_OUT[9:0]	Modulated output signal, imaginary axis. 10-bit precision. Same format as DATA_I_OUT.
SAMPLE_CLK_OUT	Output signal sampling clock. Read the output signal at the rising edge of CLK when SAMPLE_CLK_OUT = '1'. Sampling rate is either 4 x symbol rate or fclk (interpolation off/on configuration bit 7). SAMPLE_CLK_OUT can stay high when output samples are transmitted in successive CLK periods.
DAC_CLK_OUT	Output sampling clock for Digital to Analog Converters. DAC reads the output sample at the rising edge.
CLK_OUT	Output reference clock. Same as CLK internal processing clock. Typically 40 MHz.
Output Module Interface (Output data pulled)	**Definition**
SAMPLE_CLK_REQ_IN	Input. 100 MHz clock requesting output samples.
DATA_OUT[13:0]	Output. Quadrature baseband samples, 14-bit precision, 2's complement format. Bit 13 is the most significant bit. The in-phase (I) and quadrature (Q) samples alternate. Output samples are synchronous with the falling edge of SAMPLE_CLK_REQ_IN.
TX_ENABLE	Output. Transmit enable. Active high. The first sample after TX_ENABLE becomes active is an in-phase (I) sample.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 300mA.

Configuration (via Serial Link / LAN)

Complete assemblies can monitored and controlled centrally over a single serial or LAN connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

This module operates at a fixed internal clock rate $\mathbf{f_{clk}}$, determined by CLK_IN (typically 40 MHz).

Most processing is done at the sampling rate / $\mathbf{f_{sample\_clk}}$ = 4 * chip rate.

Parameters	**Configuration**
Chip rate	24-bit signed integer (2's complement) expressed as fchip rate * 2^{24} / $\mathbf{f_{clk}}$. The maximum chip rate is slightly less than $\mathbf{f_{clk}}$ /4 (a 1% margin is recommended to let the demodulator code tracking loop 'move' around the nominal settings). REG0 = bit 7-0 REG1 = bit 15 – 8 REG2 = bit 23 – 16
Spreading factor (Processing gain)	Spreading code period Range: 1 – 2^{23}-1 • When using Gold codes or maximal length sequences, it is important that this field be consistent with the G1 and G2 generator polynomials below. Length is always in the form 2^n-1, where n is an integer. • When using Barker codes, the spreading factor must be either 11 (0x0B) or 13 (0x0D). REG3 bits 7-0 (LSB) REG4 bits 7-0 REG5 bits 7-0 (MSB)
Code selection	001 = Gold code 010 = Maximal length sequences 011 = Barker code REG6 bits 2-0
Gold sequence / Maximal Length Sequence generator polynomial G1	24-bit. Describes the taps in the linear feedback shift register 1: Bit 0 is the leftmost tap (2^0 in the polynomial). The largest non-zero bit is the polynomial order n. n determines the code period 2^n –1. Example: $G1 = 1 + x^3 + x^6 + x^7 + x^9 + x^{10} + x^{14} + x^{16} + x^{17}$ is represented as 0x01 A3 64. REG7 = bit 7 – 0 REG8 = bit 15 – 8 REG9 = bit 23 – 16
Gold code generator polynomial G2	24-bit. Describes the taps in the linear feedback shift register 2: Bit 0 is the leftmost tap (2^0 in the polynomial). The largest non-zero bit is the polynomial order n. n determines the code period 2^n –1. Example: $G2 = 1 + x^9 + x^{13} + x^{14} + x^{17}$ is represented as 0x01 31 00. REG10 = bit 7 – 0 REG11 = bit 15 – 8 REG12 = bit 23 - 16
Offset carrier frequency ($\mathbf{f_c}$)	24-bit signed integer (2's complement) expressed as $\mathbf{f_c}$ * 2^{24} / fchip rate x 4. REG13 = bit 7 – 0 REG14 = bit 15 – 8 REG15 = bit 23 - 16
Signal gain (for 1012-xN firmware version only)	Signal level. 8-bit unsigned integer. Maximum level 255, Minimum level 0. When the maximal level (255) is selected, the peak-to-peak dynamic range is +/- 371 out of a +/-512 (10-bit) range and the standard deviation is 249. REG16 = bit 7-0
Noise gain (for 1012-xN firmware version only)	Additive white Gaussian noise level. 8-bit unsigned integer. Maximum level 255, Minimum level 0. The noise samples standard deviation is 111 for a maximum noise gain setting of 255. (The noise bandwidth is +/- 2* symbol rate). REG17 = bit 7-0
Internal / External clock selection	0 = internal clock 1 = external clock REG18 bit 0
Output sample format	0 = 2's complement 1 = unsigned (for example to COM-2001) REG18 bit 1
Modulation	00 = BPSK 01 = QPSK 10 = OQPSK REG18 bit 3 – 2
Test mode	00 = disabled 01 =PRBS-11, internal generation of 2047-bit periodic pseudo-random bit sequence as modulator input. (overrides external input bit stream). 10 = unmodulated carrier. (overrides external input bit stream)

	REG18 bit 5 – 4
Spectrum inversion	Invert Q bit. 0 = off 1 = on REG18 bit 6
Interpolation	Interpolation to maximum clock rate. 0 = off 1 = on REG18 bit 7
Output data flow	0 = output data is pushed to the next module (for example to COM-2001, or COM-1011) 1 = output data is pulled by next module (for example by the COM-4004) REG19 bit 0
Input format	0 = 1-bit serial 1 = 2-bit parallel REG19 bit 1
Ouput spectrum shaping filter enabled	Enables/Disables raised cosine square root output spectrum shaping filter. 0 = disabled 1 = enabled REG19 bit 2
Spreading	Enable/Disable spectrum spreading. 0 = disabled 1 = enabled REG19 bit 3

Writing to REG19 resets the output interface. When interfacing with the COM-4004 70 MHz modulator, any configuration change in the COM-4004 should be followed by an interface reset.

Operation

Configuration Files

In order to provide for configuration flexibility without unduly increasing the hardware complexity, some features require uploading different firmware into the ComBlock using the ComBlock control center.

- Channel filter (raised cosine square root) rolloff: 20%, 25% and 40%.
- AWGN generator.

All firmware versions can be downloaded from www.comblock.com/download.

COM-1012-A Direct sequence spread-spectrum modulator 20% rolloff (best sidelobes rejection).

COM-1012-B Direct sequence spread-spectrum modulator 25% rolloff (best sidelobes rejection).

COM-1012-E Direct sequence spread-spectrum modulator 40% rolloff (best sidelobes rejection).

COM-1012-AN Direct sequence spread-spectrum modulator 40% rolloff with built-in noise generator.

COM-1012-BN Direct sequence spread-spectrum modulator 25% rolloff with built-in noise generator.

COM-1012-EN Direct sequence spread-spectrum modulator 40% rolloff with built-in noise generator.

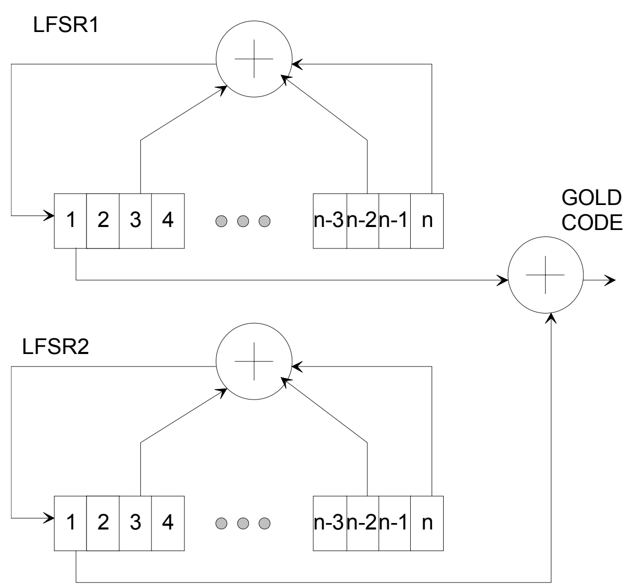
Spreading codes

Spreading codes are pseudo random sequences which falls within the following categories:

- Gold sequences, for best autocorrelation properties
- Maximal length sequences
- Barker codes (length 11, 13)

Gold sequences

Gold sequences are generated using two linear feedback shift registers LFSR1 and LFSR2 as illustrated below:



The code period is 2^n-1, where n is the number of taps in the shift register. The LFRSa are initialized to all 1's at the start of each period. The LFRSs will generate all possible n-bit combinations, except the all zeros combination.

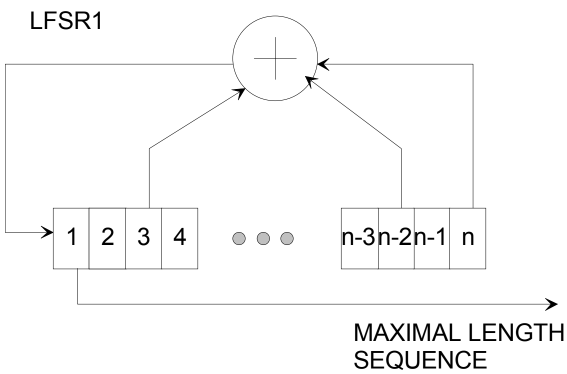
Each sequence is uniquely described by its two generator polynominals. The highest order is n. The generator polynominals are user programmable.

A few commonly used Gold sequences are listed below:

n = 17
$G1 = 1 + x^3 + x^6 + x^7 + x^9 + x^{10} + x^{14} + x^{16} + x^{17}$
$G2 = 1 + x^9 + x^{13} + x^{14} + x^{17}$

Maximal length sequences

Maximal length sequences are generated using one linear feedback shift register LFSR1 as shown below:



The code period is 2^n-1, where n is the number of taps in the shift register. The LFRSa are initialized to all 1's at the start of each period. The LFRSs will generate all possible n-bit combinations, except the all zeros combination.

Each sequence is uniquely described by its generator polynominal. The highest order is n. The generator polynominal is user programmable.

A few commonly used maximal length sequences are listed below:

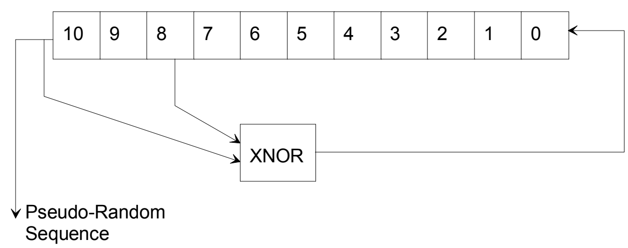
N = 4: $G1 = 1 + x + x^4$
N = 5: $G1 = 1 + x^2 + x^5$
N = 6: $G1 = 1 + x + x^6$
N = 7: $G1 = 1 + x + x^7$
N = 8: $G1 = 1 + x^2 + x^3 + x^4 + x^8$
N = 9: $G1 = 1 + x^4 + x^9$
N = 10: $G1 = 1 + x^3 + x^{10}$

Barker Codes

11 bit Barker code: 101 1011 1000, or 0x5B8
13 bit Barker code: 1 1111 0011 0101, or 0x1F35

PRBS-11 Pseudo-Random Bit Stream (Test Pattern)

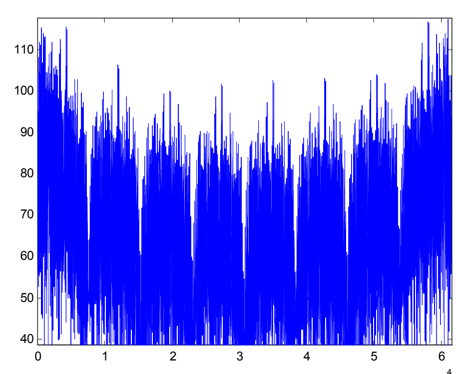
A periodic pseudo-random sequence can be used as modulator source instead of the input data stream. A typical use would be for end-to-end bit-error-rate measurement of a communication link. The sequence is 2047-bit long maximum length sequence generated by a 11-tap linear feedback shift register:



The first 100 bits of the PN sequence are as follows:
0000000000 0111111111 0011111110 0001111100
1100111000 0000010011 1111010001 1110110100
1101001100 0011000001

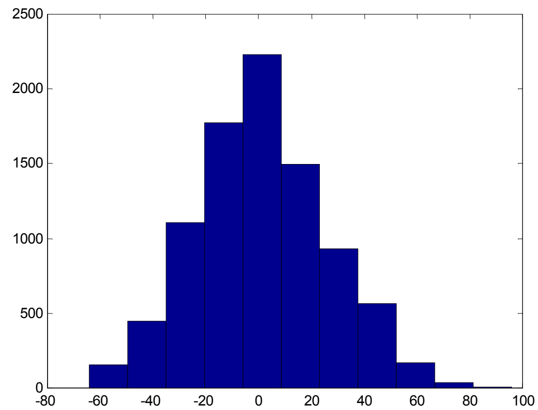
Additive White Gaussian Noise (Test Mode)

To help simulating link impairements, a simple digitally generated noise source is built in this module. The equivalent noise bandwidth is +/- 2 x chip rate. The noise samples do not undergo raised cosine square root filtering. Therefore its wideband spectrum tends towards a sin(x)/x function.



(Noise samples power spectrum over 66,000 samples)

The noise samples standard deviation is 27.8 for a noise gain setting of 64. Below is the amplitude histogram for this noise gain setting.



(Noise amplitude histogram, noise gain 64)

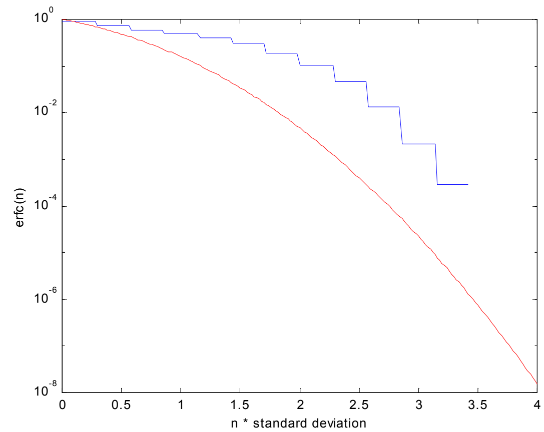
The noise standard deviation is proportional to the noise gain setting.

Below are a few useful reference points for setting the signal to noise ratio. All SNRs are measured in the modulated signal bandwidth, assuming QPSK modulation.

SNR (QPSK modulation)	Signal Gain	Noise Gain
19.3 dB	x40	x20
13.3 dB	x40	x40
10 dB	x40	x5B
7.3 dB	x40	x80
6.1 dB	x40	x90
5.3 dB	x40	xA0
4.5 dB	x40	xB0
3.7 dB	x40	xC0
3.0 dB	x40	xD0
2.3 dB	x40	xE0
1.2 dB	x40	xFF

When BPSK modulation is selected, the SNR is 3 dB lower for a given signal gain and noise gain setting: the reason is that noise is still added on both I and Q channels, whereas data is only transmitted on the I channel.

This noise generator is accurate as far as SNR measurements are concerned. However, it only <u>approximates</u> the Gaussian distribution. Therefore, this noise generator can only be used for bit error rate measurements if it is calibrated. The calibration plot below shows the erfc function for a theoretical Gaussian random variable (red) and for the built-in noise generator (blue).

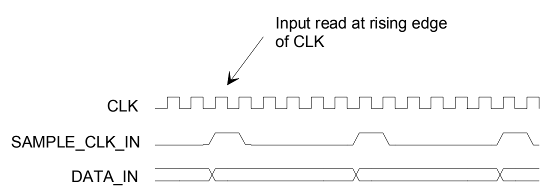


Noise generator distribution calibration (erfc function)

Timing

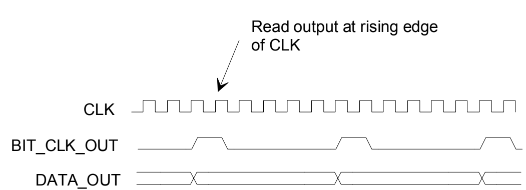
The I/O signals are synchronous with the rising edge of the reference clock CLK (i.e. all signals transitions always occur after the rising edge of the reference clock CLK). The maximum CLK frequency is 40 MHz.

Input



Output

(REG19 bit0 = 0)



Test Points

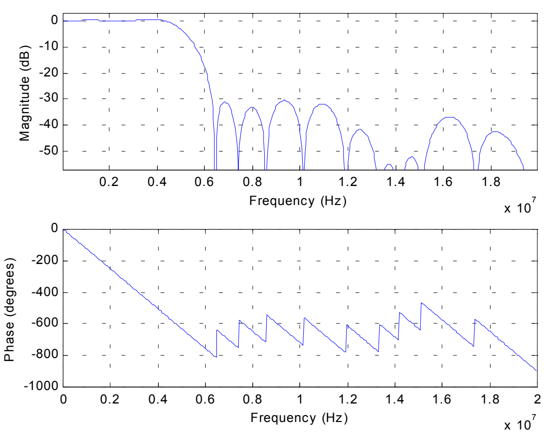
Test points are provided for easy access by an oscilloscope proble.

Test Point	Definition
TP1	Chip clock
TP2	Bit clock
TP3	PN code
TP4	PRBS-11 clock
TP5	PRBS-11 data bits
TP6	PRBS-11 start of periodic sequence
TP7	Data stream bit clock
TP8	Data stream, I channel
TP9	Data stream, Q channel

Performance

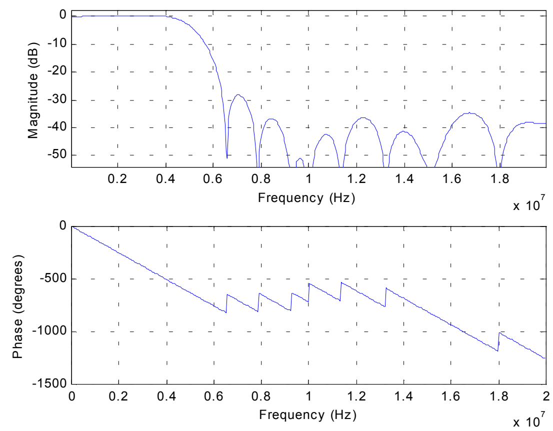
The module is configured at installation with a 20% rolloff filter. The filter rolloff can be selected among 20%, 25% and 40%. Changing the rolloff selection requires re-loading the firmware using the ComBlock control center.

Filter Response (20% rolloff)



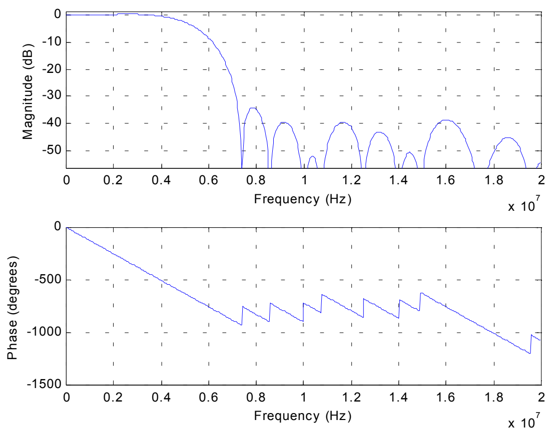
The raised cosine square root filter with 20% rolloff is a 29-tap FIR filter with the following impulse response:
Coeff(0) = -8/1024
Coeff(1) = -16/1024
Coeff(2) = -8/1024
Coeff(3) = 8/1024
Coeff(4) = 24/1024
Coeff(5) = 24/1024
Coeff(6) = 12/1024
Coeff(7) = -16/1024
Coeff(8) = -48/1024
Coeff(9) = -52/1024
Coeff(10) = -16/1024
Coeff(11) = 64/1024
Coeff(12) = 160/1024
Coeff(13) = 240/1024
Coeff(14) = 272/1024
Coeff(j=15:28) = coeff(28-j);

Filter Response (25% rolloff)



The raised cosine square root filter with 25% rolloff is a 29-tap FIR filter with the following impulse response:
Coeff(0) = -4/1024
Coeff(1) = -12/1024
Coeff(2) = -8/1024
Coeff(3) = 2/1024
Coeff(4) = 16/1024
Coeff(5) = 24/1024
Coeff(6) = 12/1024
Coeff(7) = -16/1024
Coeff(8) = -48/1024
Coeff(9) = -48/1024
Coeff(10) = -16/1024
Coeff(11) = 64/1024
Coeff(12) = 160/1024
Coeff(13) = 240/1024
Coeff(14) = 272/1024
Coeff(j=15:28) = coeff(28-j);

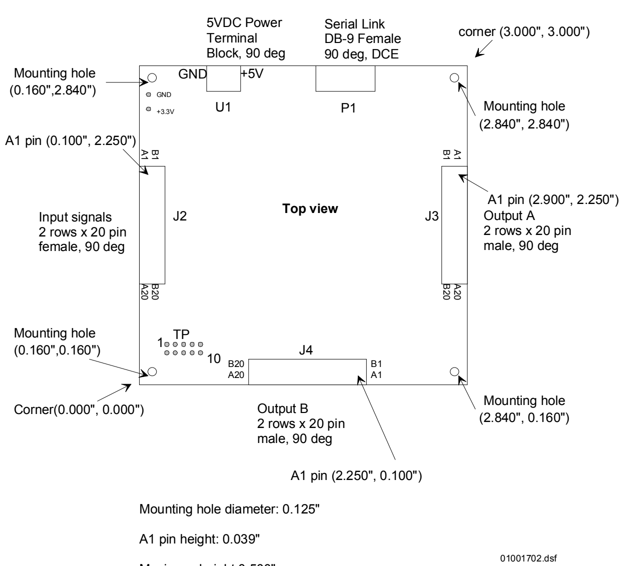
Filter Response (40% rolloff)



The raised cosine square root filter with 40% rolloff is a 29-tap FIR filter with the following impulse response:

Coeff(0) = 4/1024
Coeff(1) = 1/1024
Coeff(2) = -4/1024
Coeff(3) = -4/1024
Coeff(4) = 2/1024
Coeff(5) = 12/1024
Coeff(6) = 14/1024
Coeff(7) = -2/1024
Coeff(8) = -30/1024
Coeff(9) = -48/1024
Coeff(10) = -24/1024
Coeff(11) = 48/1024
Coeff(12) = 152/1024
Coeff(13) = 248/1024
Coeff(14) = 284/1024
Coeff(j=15:28) = coeff(28-j);

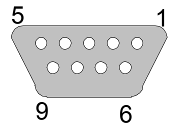
Mechanical Interface



Pinout

Serial Link P1

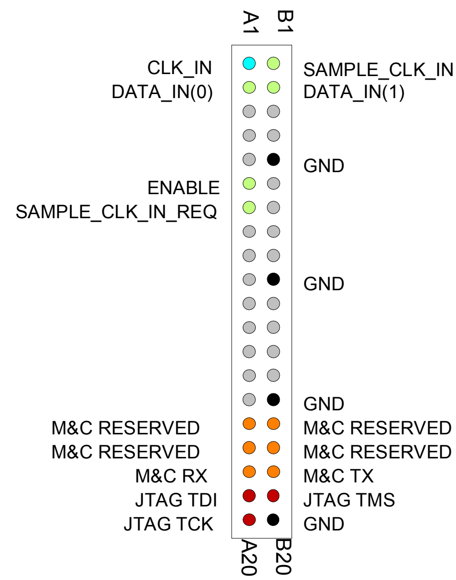
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



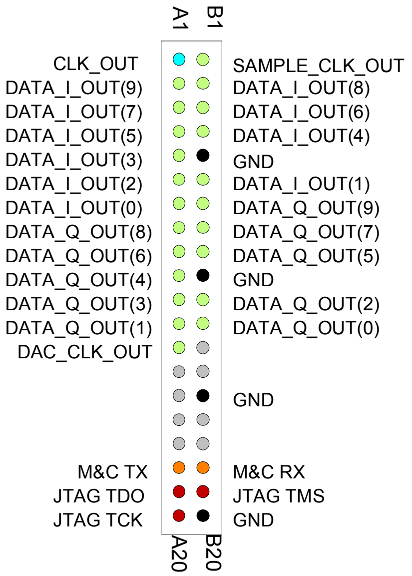
2 Transmit
3 Receive
5 Ground

DB-9 Female

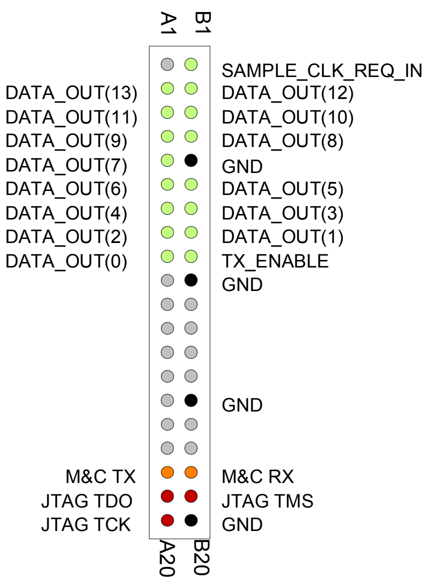
Input Connector J2



Output Connectors J3, J4



This connector is used when output data is pushed out (configuration REG19 bit 0 = 0).



This connector is used when output data is pulled out by the next module (configuration REG19 bit 0 = 1).

I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-1010 Convolutional encoder	COM-1011/1018 DSSS Demodulator (back to back)
COM-7001 Turbo Code Error correction encoder	COM-2001 digital-to-analog converter (baseband).
COM-8001 Arbitrary waveform signal generator 256MB/1GB	COM-4004 70 MHz IF modulator
	COM-1023 BER generator, Additive White Gaussian Noise Generator
	COM-1024 Multipath simulator.

ComBlock Ordering Information

COM-1012
Direct-sequence spread-spectrum modulator

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