


COM-1018 DIRECT SEQUENCE SPREAD-SPECTRUM DEMODULATOR 20 Mchip/s

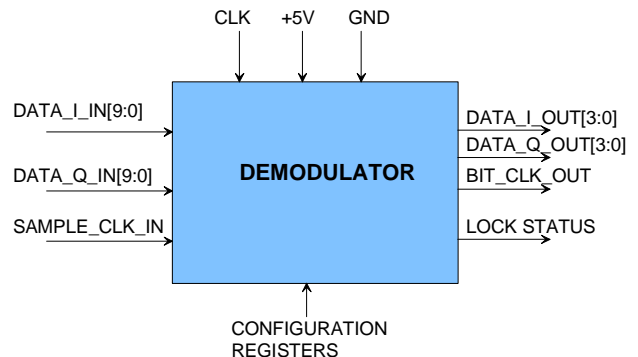
Key Features

- Direct sequence spread-spectrum demodulator.
- Variable chip rate up to 20 Mchips/s.
- Spreading codes:
 - Gold sequences (up to $2^{23}-1$ chips)
 - Maximal length sequences, (max length $2^{23}-1$ chips)
 - Barker codes (length 11, 13)
 - GPS C/A codes.
- BPSK, QPSK selectable.
- Demodulation performances: within 1.5 dB from theory at threshold SNR of 5 dB.
- Sequential code search.
- 4-bit soft-quantized demodulated bits.
- Monitoring:
 - Receiver lock
 - Carrier frequency error
-  **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right). Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.



Electrical Interface

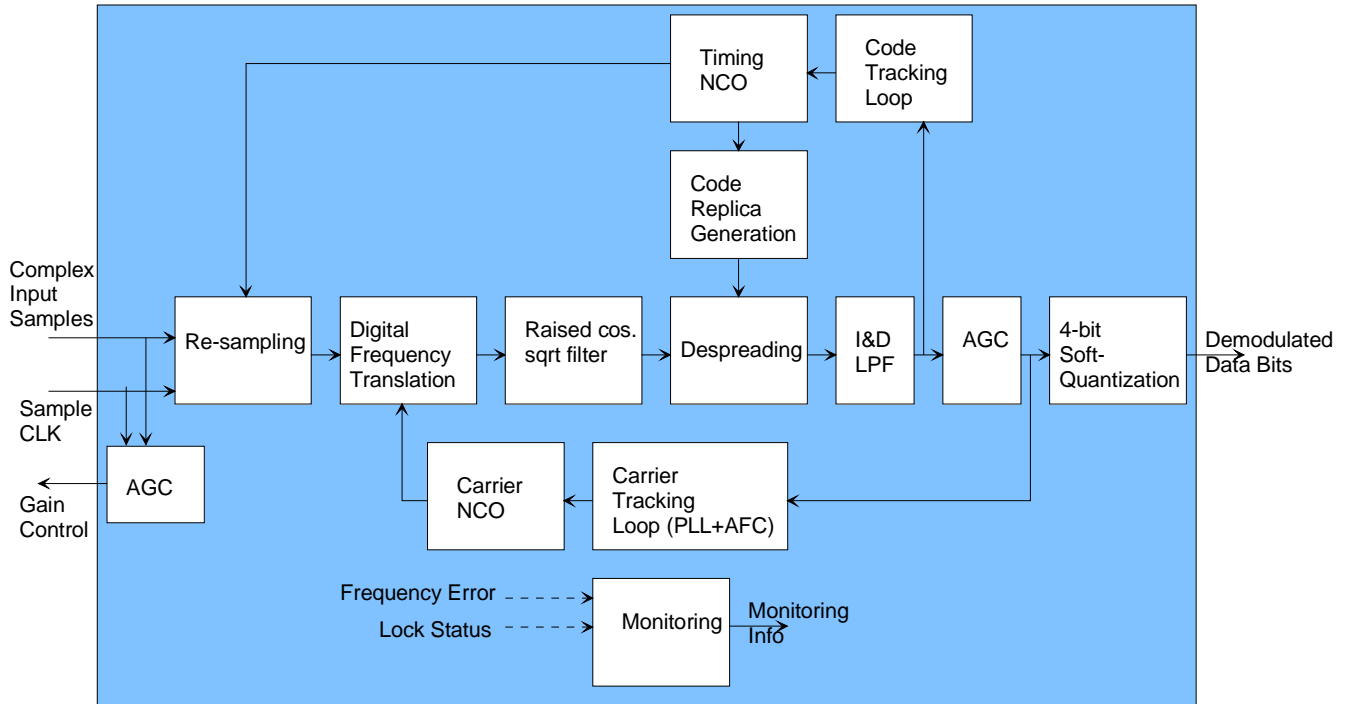
Demodulator Inputs / Outputs



For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1018.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm.

Block Diagram



Input Module Interface	Definition
DATA_I_IN[9:0]	Modulated input signal, real axis. 10-bit precision. Format: 2's complement or unsigned. Unused LSBs are pulled low. LVTTL 0 – 3.3V
DATA_Q_IN[9:0]	Modulated input signal, imaginary axis. 10-bit precision. Same format as DATA_I_IN. Unused LSBs are pulled low. LVTTL 0 – 3.3V
SAMPLE_CLK_IN	Input signal sampling clock. One CLK-wide pulse. Read the input signal at the rising edge of CLK when SAMPLE_CLK_IN = '1'. Nominal sampling rate is between 4 and 8 samples per symbol. Samples can be consecutive. Signal is pulled-up. LVTTL 0 – 3.3V
AGC_OUT	Output. When this demodulator is connected directly to an analog receiver, it generates a pulse-width modulated signal to control the analog gain prior to A/D conversion. The purpose is to use the maximum dynamic range while

	preventing saturation at the A/D converter. 0 is the maximum gain, +3V is the minimum gain.
CLK_IN	Input reference clock for synchronous I/O. DATA_x_IN and SAMPLE_CLK_IN are read at the rising edge of CLK_IN. Maximum 40 MHz.

Two basic types of output connections are available for user selection:

- direct connection between demodulator and data destination.
- Shared data bus connecting multiple demodulators to a single data destination (for signal diversity combining)

Output Module Interface	Definition
Direct connection between two ComBlocks, REG18(7) = '0'	
DATA_I_OUT[3:0]	4-bit soft-quantized demodulated bits, real axis. Unsigned representation: 0000 for maximum amplitude '0', 1111 for maximum amplitude

	<p>'1'. When the serial output mode is selected, I and Q samples are transmitted one after another on this interface. I is transmitted before Q.</p>
DATA_Q_OUT[3:0]	<p>4-bit soft-quantized demodulated bits, imaginary axis. Same format as DATA_I_OUT. When the serial output mode is selected, this interface is unused.</p>
BIT_CLK_OUT	<p>Demodulated bit clock. One CLK-wide pulse. Read the output signal at the rising edge of CLK when BIT_CLK_OUT = '1'.</p>
RX_LOCK	<p>'1' when the demodulator is locked, '0' otherwise. The lock status is based on the code lock.</p>
CLK_OUT	<p>40 MHz output reference clock. Generated by dividing the internal processing clock: $f_{clk}/2$</p>

Output Module Interface	Definition
Shared bus, REG18(7) = '1'	
BUS_CLK_IN	40 MHz input reference clock for use on the synchronous bus.
BUS_ADDR[3:0]	Bus address. Input (since this module is a bus slave). Designates which slave module is targeted for this read transaction. Read at the rising edge of BUS_CLK_IN
BUS_RWN	Read/Write#. Input (since this module is a bus slave). Indicates whether a read (1) or write (0) transaction is conducted. Read at the rising edge of BUS_CLK_IN. Read and Write refer to the bus master's perspective.
BUS_DATA[15:0]	<p>Bi-directional data bus. Input when BUS_RWN='0'. Output when BUS_RWN='1'. Read latency is 2 BUS_CLK_IN periods. Minimum read cycle is 3 BUS_CLK_IN periods. Reading can be continuous.</p> <p>Functional definition during read:</p> <ul style="list-style-type: none"> bit 0 BIT_CLK_OUT. '1' when DATA_I_OUT is available bits(4:1) DATA_I_OUT[3:0] demodulated data stream. bit 5 RX_LOCK.

	<ul style="list-style-type: none"> bits(10:6) test points. bits(15:11) undefined.
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Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 20 Mchip/s is 450mA.

Important: I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration

Complete assemblies can be monitored and controlled centrally over a single serial, LAN/TCP-IP, USB 2.0 or PCMCIA/CardBus connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

This module operates at a fixed internal clock rate f_{clk} of 80 MHz.

Most processing is done at the sampling rate / $f_{sample_clk} = 4 * \text{chip rate}$.

Parameters	Configuration
Chip rate	<p>24-bit integer expressed as $f_{chip\ rate} * 2^{24} / f_{clk}$.</p> <p>The maximum practical chip rate is $0.99 * f_{clk} / 4$ to allow for at 4 samples per chip. The 99% factor is to leave code tracking loop some margin between nominal and actual received chip rates.</p> <p>REG0 = bit 7-0 REG1 = bit 15 – 8 REG2 = bit 23 – 16</p>
Spreading factor (Processing gain)	<p>Spreading code period Range: $1 - 2^{23} - 1$</p> <ul style="list-style-type: none"> When using Gold codes or maximal length sequences, it is important that this field be consistent with the G1 and G2 generator polynomials below. Length is always in the form $2^n - 1$, where n is an integer. When using Barker codes, the spreading factor must be either 11 (0x0B) or 13 (0x0D). <p>REG3 bits 7-0 (LSB)</p>

	REG4 bits 7-0 REG5 bits 7-0 (MSB)
Code selection	001 = Gold code 010 = Maximal length sequences 011 = Barker code 100 = GPS C/A codes REG6 bits 2-0
Gold sequence / Maximal Length Sequence generator polynomial G1	24-bit. Describes the taps in the linear feedback shift register 1: Bit 0 is the leftmost tap (2^0 in the polynomial). The largest non-zero bit is the polynomial order n. n determines the code period $2^n - 1$. Example: $G1 = 1 + x^3 + x^6 + x^7 + x^9 + x^{10} + x^{14} + x^{16} + x^{17}$ is represented as 0x01 A3 64. REG7 = bits 7 – 0 REG8 = bits 15 – 8 REG9 = bits 23 – 16
Gold code generator polynomial G2	24-bit. Describes the taps in the linear feedback shift register 2: Bit 0 is the leftmost tap (2^0 in the polynomial). The largest non-zero bit is the polynomial order n. n determines the code period $2^n - 1$. Example: $G2 = 1 + x^9 + x^{13} + x^{14} + x^{17}$ is represented as 0x01 31 00. REG10 = bit 7 – 0 REG11 = bit 15 – 8 REG12 = bit 23 - 16
GPS satellite ID	GPS signals from different satellites are designated by a PRN signal number in the range 1 – 37. This field is used only if GPS C/A codes are selected. REG10 = bit 5 – 0
Nominal carrier center frequency (f_c)	Nominal center frequency. This value is subtracted from the received signal actual center frequency. 24-bit signed integer (2's complement) expressed as $f_c * 2^{24} / f_{chip} \text{ rate} * 4$. Maximum range to avoid aliasing is $\pm 1.5 * f_{chip} \text{ rate}$. REG13 = bit 7 – 0 REG14 = bit 15 – 8 REG15 = bit 23 - 16
Input sample format	0 = 2's complement 1 = unsigned REG16 bit 1
Carrier frequency loop gain	00 = nominal 01 = 2x loop gain 10 = 4x loop gain 11 = 8x loop gain REG16 bits 3-2
AFC enable	The Automatic Frequency Control

	(AFC) circuit extends the frequency acquisition over $\pm 10\%$ of the unspread symbol rate. When disabled, the receiver only means of carrier acquisition is the carrier frequency tracking loop which is inherently limited to approximately 1% of the unspread symbol rate. 0 = AFC disabled. Carrier tracking loop only 1 = AFC enabled. REG16 bit 4
Spectrum inversion	Invert Q bit. 0 = off 1 = on REG16 bit 5
Reserved	0 REG16 bit 6
Freeze monitoring data	As the monitoring data is constantly changing, it is important to be able to prevent changes while reading a multi-byte parameter. Write a zero in bit 7 to freeze the monitoring data prior to reading it. Write a one to re-enable the update. REG16 bit 7
Output sample format	00 = I/Q parallel. The Q-channel data is meaningless in case of BPSK modulation. 01 = I/Q serial. I is sent before Q in the case of QPSK. I-only samples in the case of BPSK. REG17 bits 1-0
BPSK / QPSK decoding	00 = BPSK 01 = QPSK REG17 bits 3-2
Code sweep period N_{lock}	Duration (in bits) of the search for a given code position during the code acquisition phase. This allows one to tradeoff acquisition time versus threshold SNR. 000 = 2 001 = 4 010 = 8 011 = 16 100 = 32 101 = 64 110 = 128 REG17 bits 6-4
Force Acquisition	A one-time write of '1' forces all loops (code, carrier PLL, AFC) back into acquisition mode. This can be used to get out of a false lock condition. There is no need to clear this bit. REG17 bit 7.
Bus address	Unique 4-bit address identifying this module on the output bus (if the output bus is enabled in REG18 bit 7). Ignore otherwise. This module acts as bus

	slave: it performs the read transaction requested by the bus master if and only if the bus address matches its own address defined here. This address must be unique among modules connected to the same bus in order to avoid conflicts. REG18 bits 3-0
Point-to-point vs shared bus output	Controls whether the output connection is point-to-point or multipoint-to-point over a shared data bus (via a COM-9003 multiplexing connector for example). The J4 output connector pinout is affected by this control bit. 0 = direct connection. Point to point. 1 = shared data bus. REG18 bit 7

Baseline configurations can be found at www.comblock.com/tsbasic_settings.htm and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

Monitoring

Monitoring registers are read-only.

Parameters	Monitoring
Carrier frequency offset	Residual frequency offset with respect to the nominal carrier frequency. 24-bit signed integer (2's complement) expressed as $f_{c\delta} * 2^{24} / f_{chip\ rate} * 4$ REG18 = bit 7 - 0 REG19 = bit 15 - 8 REG20 = bit 23 - 16
AGC gain	Digital AGC gain settings 8 bit unsigned REG21 bit 7-0.
Reserved	REG22: bit 7 - 0
Carrier Lock status	REG23 bit 0 0 = unlocked 1 = locked
Code Lock status	REG23 bit 1 0 = unlocked 1 = locked
Code Acquisition	REG23 bit 2 0 = code tracking mode 1 = code acquisition mode
Option o / Version v	Returns '1018ov' when prompted for option o and version v numbers.

ComScope Monitoring

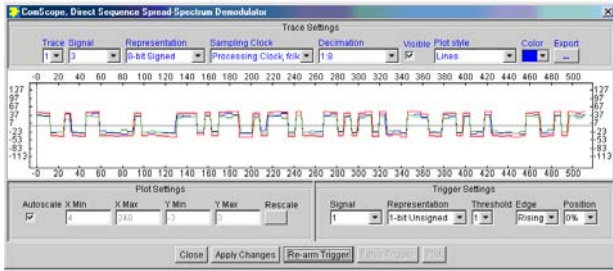
Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-1018 signal traces and trigger are defined as follows:

Trace 1 signals	Format	Nominal sampling rate	Buffer length (samples)
1: Input I signal	8-bit signed or unsigned. (8MSB/10)	Input sampling rate	512
2: spread I-channel after root raised cosine filter	8-bit signed (8MSB/12)	4 samples/chip	512
3: Despread I-channel, center, after I&D	8-bit signed (8MSB/12)	1 sample / symbol	512
4: Frequency error (AFC)	8-bit signed or unsigned. (8MSB/24)	1 sample / symbol	512
Trace 2 signals	Format	Nominal sampling rate	Buffer length (samples)
1: Input Q signal	8-bit signed or unsigned. (8MSB/10)	Input sampling rate	512
2: Code replica. Compare with spread input signals	8-bit signed	4 samples/chip	512
3: front-end AGC	8-bit unsigned (8MSB/10)	f_{clk} (80 MHz)	512
4: Phase error (Costas Loop)	8-bit signed (8MSB/10)	1 sample / symbol	512
Trigger Signal	Format		
1: Start of code replica	binary		

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk} processing clock as real-time sampling clock.

In particular, selecting the f_{clk} processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.

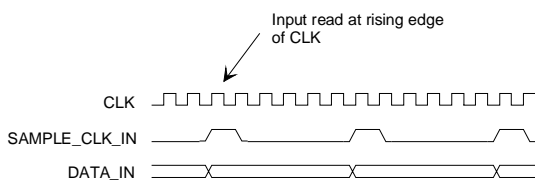


ComScope Window Sample: showing despread signal after integrate & dump.

Timing

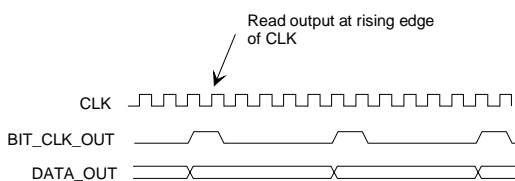
The I/O signals are synchronous with the rising edge of the reference clock CLK (i.e. all signals transitions always occur after the rising edge of the reference clock CLK). The maximum CLK frequency is 40 MHz.

Input



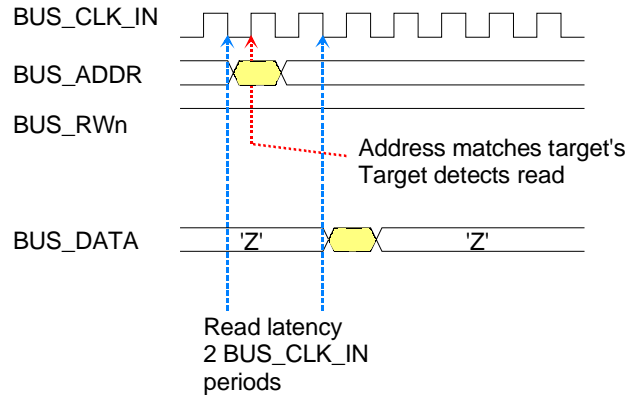
Output

(Point to point connection, REG18 bit7 = '0')



Output

(Shared bus, REG18 bit7 = '1')



Test Points

Test points are provided for easy access by an oscilloscope probe at the J4 male connector. (Note: test points are disabled when the output is configured for shared data bus interface).

Test Point	Definition
J4/A7	Carrier lock
J4/B7	Code lock (1) or scanning (0)
J4/A8	Recovered carrier
J4/B8	Recovered bit timing (i.e. start of code period). Useful to monitor code acquisition and tracking. Compare with modulator bit timing.
J4/A9	Spreading code replica
J4/B9	Spread I signal (MSB) (compare with spreading code replica at J4/A9)

Implementation

Spreading codes

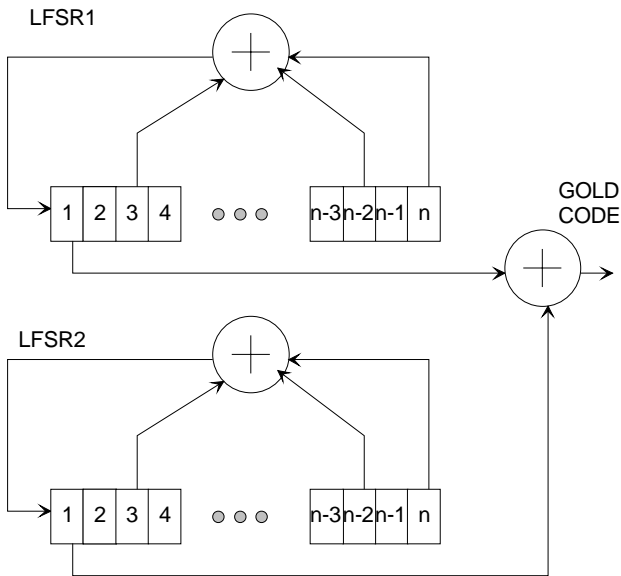
Spreading codes are pseudo random sequences which falls within the following categories:

- Gold sequences, for best autocorrelation properties
- Maximal length sequences
- Barker codes (length 11, 13)
- GPS C/A codes.

The same spreading code is used on both the in-phase (I) and quadrature (Q) channels.

Gold sequences

Gold sequences are generated using two linear feedback shift registers LFSR1 and LFSR2 as illustrated below:



The code period is $2^n - 1$, where n is the number of taps in the shift register. The LFSRs are initialized to all 1's at the start of each period. The LFSRs will generate all possible n-bit combinations, except the all zeros combination.

Each sequence is uniquely described by its two generator polynomials. The highest order is n. The generator polynomials are user programmable.

A few commonly used Gold sequences are listed below:

n = 5 (length 31):

$$G1 = 1 + x^2 + x^5$$

$$G2 = 1 + x + x^2 + x^4 + x^5$$

$$REG3 = x1F \quad REG4 = x00 \quad REG5 = x00$$

$$REG7 = x12 \quad REG8 = x00 \quad REG9 = x00$$

$$REG10 = x1B \quad REG11 = x00 \quad REG12 = x00$$

n = 6 (length 63):

$$G1 = 1 + x^5 + x^6$$

$$G2 = 1 + x + x^4 + x^5 + x^6$$

$$REG3 = x3F \quad REG4 = x00 \quad REG5 = x00$$

$$REG7 = x30 \quad REG8 = x00 \quad REG9 = x00$$

$$REG10 = x39 \quad REG11 = x00 \quad REG12 = x00$$

n = 7 (length 127):

$$G1 = 1 + x^3 + x^7$$

$$G2 = 1 + x + x^2 + x^3 + x^4 + x^5 + x^7$$

$$REG3 = x7F \quad REG4 = x00 \quad REG5 = x00$$

$$REG7 = x44 \quad REG8 = x00 \quad REG9 = x00$$

$$REG10 = x5F \quad REG11 = x00 \quad REG12 = x00$$

n = 9 (length 511):

$$G1 = 1 + x^5 + x^9$$

$$G2 = 1 + x^3 + x^5 + x^6 + x^9$$

$$REG3 = xFF \quad REG4 = x01 \quad REG5 = x00$$

$$REG7 = x10 \quad REG8 = x01 \quad REG9 = x00$$

$$REG10 = x34 \quad REG11 = x01 \quad REG12 = x00$$

n = 10 (length 1023):

$$G1 = 1 + x^7 + x^{10}$$

$$G2 = 1 + x^2 + x^7 + x^8 + x^{10}$$

$$REG3 = xFF \quad REG4 = x03 \quad REG5 = x00$$

$$REG7 = x40 \quad REG8 = x02 \quad REG9 = x00$$

$$REG10 = xC2 \quad REG11 = x02 \quad REG12 = x00$$

n = 11 (length 2047):

$$G1 = 1 + x^9 + x^{11}$$

$$G2 = 1 + x^3 + x^6 + x^9 + x^{11}$$

$$REG3 = xFF \quad REG4 = x07 \quad REG5 = x00$$

$$REG7 = x00 \quad REG8 = x05 \quad REG9 = x00$$

$$REG10 = x24 \quad REG11 = x05 \quad REG12 = x00$$

n = 17 (length 131071):

$$G1 = 1 + x^5 + x^6 + x^7 + x^9 + x^{10} + x^{14} + x^{16} + x^{17}$$

$$G2 = 1 + x^9 + x^{13} + x^{14} + x^{17}$$

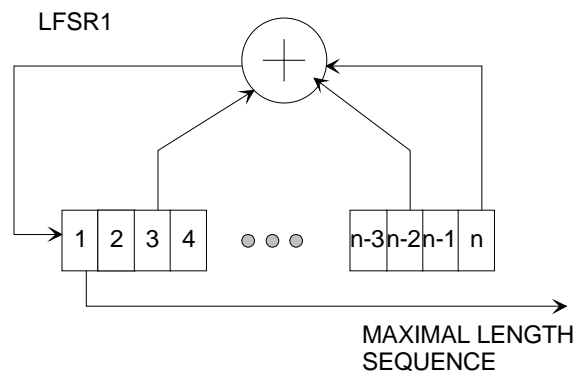
$$REG3 = xFF \quad REG4 = xFF \quad REG5 = x01$$

$$REG7 = x64 \quad REG8 = xA3 \quad REG9 = x01$$

$$REG10 = x00 \quad REG11 = x31 \quad REG12 = x01$$

Maximal length sequences

Maximal length sequences are generated using one linear feedback shift register LFSR1 as shown below:



The code period is $2^n - 1$, where n is the number of taps in the shift register. The LFSRs are initialized to all 1's at the start of each period. The LFSRs will

generate all possible n-bit combinations, except the all zeros combination.

Each sequence is uniquely described by its generator polynomial. The highest order is n. The generator polynomial is user programmable.

A few commonly used maximal length sequences are listed below:

- n = 4: $G1 = 1 + x + x^4$
- n = 5: $G1 = 1 + x^2 + x^5$
- n = 6: $G1 = 1 + x + x^6$
- n = 7: $G1 = 1 + x + x^7$
- n = 8: $G1 = 1 + x^2 + x^3 + x^4 + x^8$
- n = 9: $G1 = 1 + x^4 + x^9$
- n = 10: $G1 = 1 + x^3 + x^{10}$

Barker Codes

- 11 bit Barker code: 101 1011 1000, or 0x5B8
- 13 bit Barker code: 1 1111 0011 0101, or 0x1F35

The length (11 or 13) must be entered as spreading factor in REG3/4/5.

GPS C/A Codes

GPS C/A codes are modified Gold codes of length 1023 with generator polynomials:

$$G1 = 1 + x^3 + x^{10}$$

$$G2 = 1 + x^2 + x^3 + x^6 + x^8 + x^9 + x^{10}$$

The G2 generator output is slightly modified so as to create a distinct code for each satellite. The G2 output is generated by summing two specific taps of the shift register. In the case of Satellite ID 1 for example, taps 2 and 6 are summed.

The G2 output taps are listed below:

Satellite ID / GPS PRN Signal Number	G2 output taps selection	Satellite ID / GPS PRN Signal Number	G2 output taps selection
1	2 xor 6	21	5 xor 8
2	3 xor 7	22	6 xor 9
3	4 xor 8	23	1 xor 3
4	5 xor 9	24	4 xor 6
5	1 xor 9	25	5 xor 7
6	2 xor 10	26	6 xor 8
7	1 xor 8	27	7 xor 9
8	2 xor 9	28	8 xor 10

9	3 xor 10	29	1 xor 6
10	2 xor 3	30	2 xor 7
11	3 xor 4	31	3 xor 8
12	5 xor 6	32	4 xor 9
13	6 xor 7	33	5 xor 10
14	7 xor 8	34	4 xor 10
15	8 xor 9	35	1 xor 7
16	9 xor 10	36	2 xor 8
17	1 xor 4	37	4 xor 10
18	2 xor 5		
19	3 xor 6		
20	4 xor 7		

Compliant with “Navstar GPS Space Segment / Navigation User Interfaces” specifications, ICD-GPS-200, Revision C. IRN-200C-004, 12 April 2000.

Data Rate

The data rate is determined by the chip rate, the processing gain (i.e. the spreading code period) and the modulation (BPSK/QPSK).

For a QPSK modulated signal, the data rate is $2 * f_{chip} \text{ rate} / \text{processing gain}$

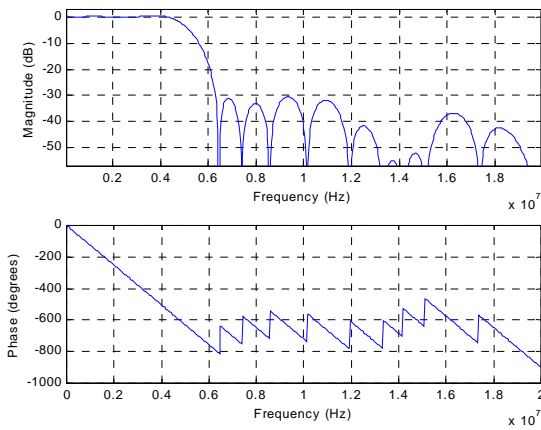
Filter Response

This module is configured at installation with a 40% rolloff filter. The filter rolloff can be selected among 20%, 25%, 35% and 40%. Changing the rolloff selection requires re-loading the firmware using the ComBlock control center.

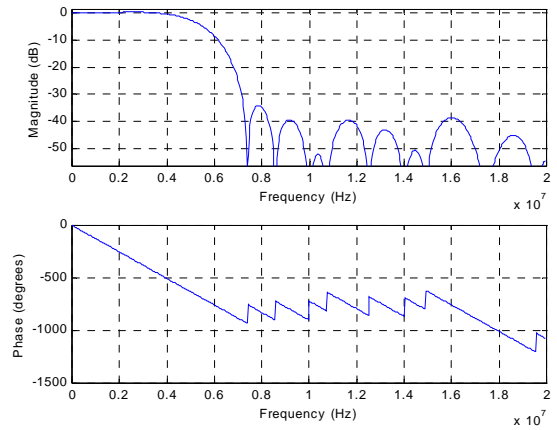
All firmware versions can be downloaded from www.comblock.com/download.

- COM-1018-A DSSS demodulator 20% rolloff
- COM-1018-B DSSS demodulator 25% rolloff
- COM-1018-D DSSS demodulator 35% rolloff
- COM-1018-E DSSS demodulator 40% rolloff

Filter Response (20% rolloff)

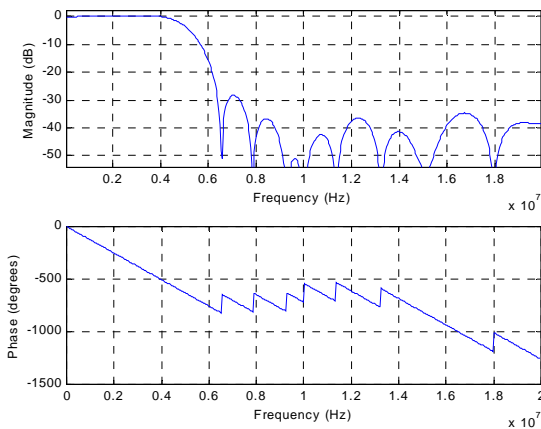


Filter Response (40% rolloff)

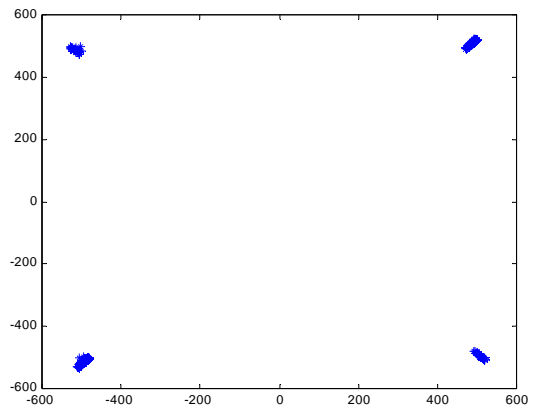


(filter response normalized for 4*symbol rate = 40 MHz)

Filter Response (25% rolloff)

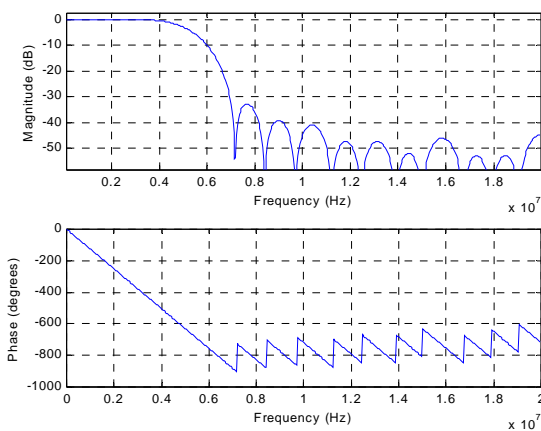


(filter response normalized for 4*symbol rate = 40 MHz)



I/Q constellation at the center of a spreading chip. Captured at the demodulator raised cosine square root filter output. QPSK. 40% rolloff. (digital modulator-demodulator back to back).

Filter Response (35% rolloff)



(filter response normalized for 4*symbol rate = 40 MHz)

Frequency Tracking

The demodulator comprises both a phase locked loop (PLL) and an Automatic Frequency Control (AFC) loop. The AFC is to quickly detect and compensate for carrier frequency offsets, generally around the time of the code acquisition. The PLL is to detect and compensate for carrier phase errors.

The PLL is a second order loop. It can track the center frequency over a range of $\pm 1.5 * \text{symbol rate}$. The digital implementation of the Costas PLL has a small frequency acquisition range of about $\pm 1\%$ of the despread symbol rate.

The main purpose of the AFC is to increase the frequency acquisition window to about $\pm 10\%$ of the

despread symbol rate (typical). Once acquisition is achieved, the AFC can be disabled (see REG16 bit4).

If the unknown received carrier frequency uncertainty is larger, the user must program some search algorithm using the nominal center frequency control registers (REG13/14/15).

For high data rates (> 100 Kbps), carrier phase noise is generally negligible. For lower data rates, it is may be necessary to adjust the carrier tracking loop gain as a tradeoff between carrier phase noise (originating at the modulator, up-converter, down-converter, etc) and thermal noise. To this effect, the user is given control of the loop gain over a range of $x1$, $x2$, $x4$ and $x8$.

The higher loop gain can also be used temporarily during acquisition to increase the frequency acquisition window from approximately 1% to 3% of the symbol rate. However, use of the AFC is preferred because of the faster acquisition time and larger acquisition range.

In some conditions, such as no input signal, the AFC and PLL loops can drift out and inhibit (re-)acquisition. It is possible for the user to reset the accumulators within the AFC and PLL loops by writing a '1' in REG17 bit7.

Code Tracking Loop

The code tracking loop is a coherent delay lock loop (DLL) of the 1st order.

Code Acquisition

When code lock is not detected for N_{lock} consecutive bits, the receiver goes into code acquisition mode. The code replica is swept until code lock is detected (sequential code search). The rate at which the code replica is scanned is one chip every N_{lock} bits. The search stops as soon as code lock is detected. The parameter N_{lock} is user-defined.

Input Interpolation

This module provides fine selection of symbol rates, as long as the input sampling rate is between $x4$ and $x8$ the symbol rate. For higher ratios between input sampling rate / symbol rate, the

COM-1008 variable decimation filter is recommended to prevent aliasing.

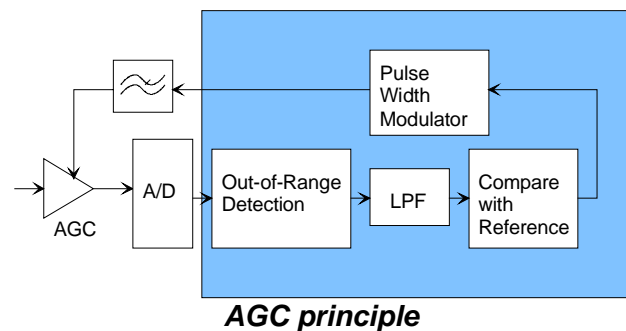
AGC

The COM-1018 comprises two AGC circuits, one at the front-end operating jointly with a front-end analog receiver, the other fully digital after channel filtering.

Front-End AGC

The purpose of this front-end AGC is to prevent saturation at the external A/D converter(s) while making full use of the 10-bit A/D converter dynamic range. The principle of operations is outlined below:

- (a) out-of-range at the A/D converter is detected. An out-of-range condition occurs if the quantized A/D samples are equal to either "1111111111" or "0000000000".
- (b) The AGC will adjust the analog circuitry gain so that out-of-range conditions do not occur more than 1 in 64 samples in the average.
- (c) The resulting gain control signal is a pulse-width modulated (PWM) signal with 10-bit precision.



The analog circuit shall filter this 3.3V low-voltage TTL PWM signal with a low-pass filter prior to controlling the analog gain. The PWM is randomized and its spectral distribution shifted to the higher frequencies so as facilitate the analog low-pass filter design.

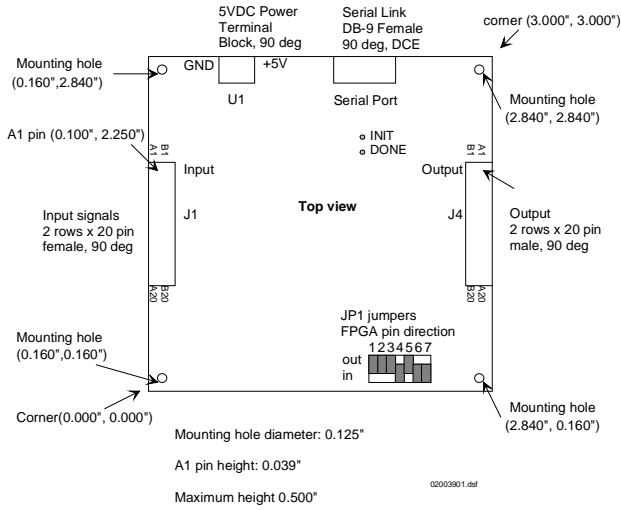
The AGC loop bandwidth is typically 1 Hz when used in conjunction with COM-30xx receivers and a 40 MHz input clock. The loop response time is assymetrical: it responds faster to a saturation condition than to a 'low signal' condition.

The gain control signal will increase if too many out-of-range conditions occur.

Digital AGC

A digital AGC provides 18 dB (3 bits) of dynamic range for signals following the raised cosine filter.

Mechanical Interface

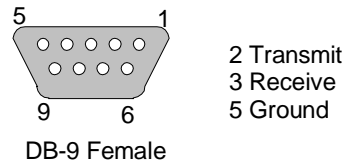


Note: All seven JP1 jumpers must be in the 'IN' location.

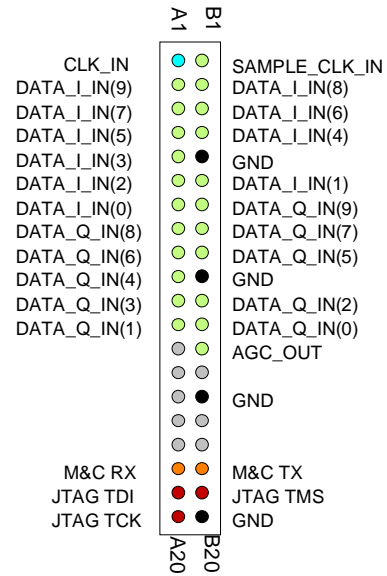
Pinout

Serial Port

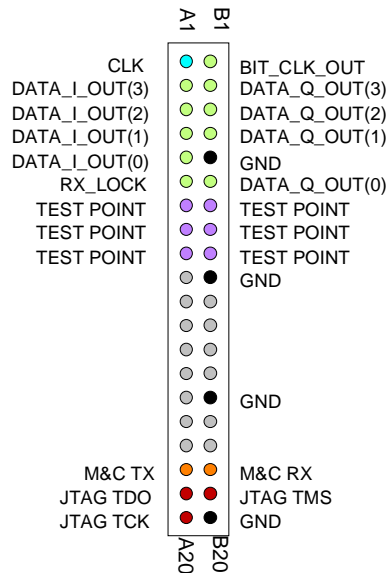
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



Input Connector J1



Output Connectors J4



This connector is used for point-to-point (i.e. direct) connection between two ComBlocks when control register REG18(7) = '0'.

