COM-1852SOFT CCSDS Proximity-1 Modem VHDL source code overview / IP core

Overview

The COM-1852SOFT is a proximity space-link modem for short-range, bi-directional, fixed or mobile radio links, generally used to communicate among probes, landers, rovers, orbiting constellations, and orbiting relays. The modem is fully compliant with the PROXIMITY-1 CCSDS standard [1].

More generally, this IP core is a fairly generic PCM/Bi-Phase L/Phase Modulation modem.

The IP core is intended for implementation in FPGA, SoC or ASIC. It is written in generic portable VHDL.

The entire **VHDL source code** is deliverable. It is portable to a variety of FPGA targets.

This IP core is available as transmitter-only, receiver-only or bundled tx/rx.

Key Features

- PCM/Bi-Phase L/phase modulation modem, 60 deg.
- Programmable symbol rate from 1KS/s to 4096 KS/s
- Large 160 KHz (two-sided) frequency acquisition and tracking.
- Large 1000ppm symbol rate acquisition range
- Tracking threshold E_b/N_0 = 0 dB
- Built-in tools: PRBS-11 pseudo-random test sequence, BER tester, AWGN generator, internal loopback mode, carrier frequency error measurement.

CCSDS standard compliance

Key parameters	CCSDS reference
Modulation: Bi-phase L coding 60° phase modulation	[1] Section 3.3.4
Coded symbol rates R_{cs}: 1000, 2000, 4000, 8000, 16000, 32000, 64000, 128000, 256000, 512000, 1024000, 2048000, 4096000 Channel symbol rate R_{cs} is 2 * R_{cs}	[1] Section 3.3.6.1 *ADC sampling rate must be strictly greater than 4*symbol rate + 1%
Discrete spurious spectral lines in tx spectrum: < 30 dBc below 2* R_{chs} < -60 dBc above 20* R_{cs}	[1] Section 3.4.4
Receiver frequency acquisition window (two-sided): 160 KHz (includes maximum Doppler + RF synthesizer drifts)	[1] Section 3.4.5.1 + extension from 10 KHz to 160 KHz
Receiver tracking	+-160 KHz
Doppler rate: 200 Hz/s max	[1] Section 3.4.5.1
Channel symbol rate offset < 50ppm without idle sequence < 1% with at least 3200-bit long idle sequence	[1] Section 3.3.6.3

Portable VHDL code

The code is written in generic standard VHDL and is thus portable to a variety of FPGAs. The code was developed on a Xilinx 7-series FPGA but is expected to work similarly on other targets. No manufacturer-specific primitive is used.

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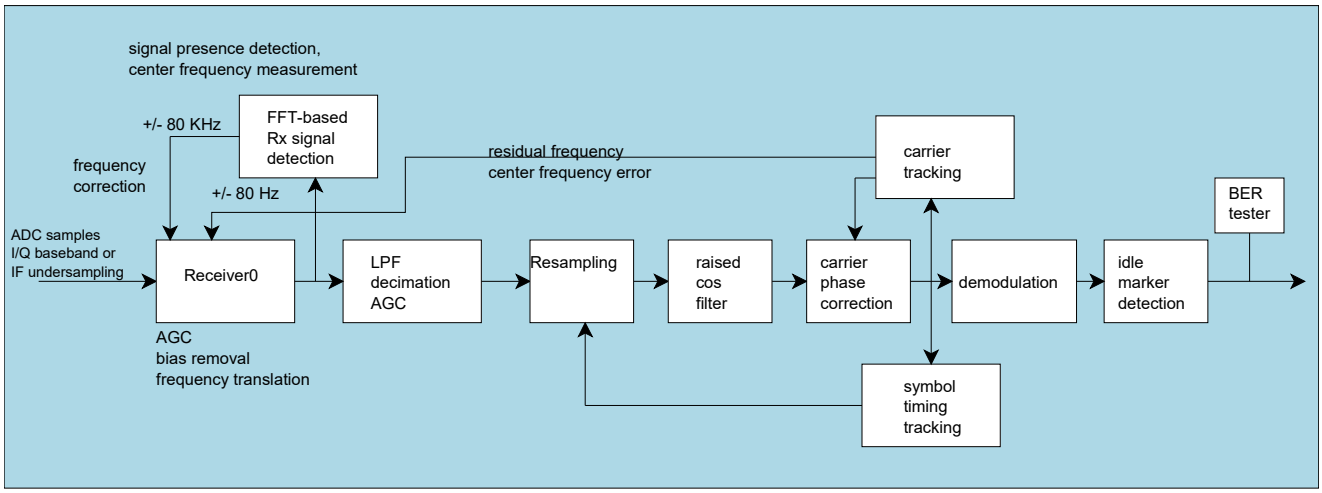
Block Diagram



receiver block diagram

Configuration

Pre-Synthesis configuration parameters

The following constants are user-defined in the component generic section prior to synthesis. These parameters generally affect the size of the embodiment.

Synthesis-time configuration parameters	
Proximity-1 transmitter	
AWGN_EN	'1' to instantiate an Additive White Gaussian Noise generator. '0' during operational conditions to save space in FPGA (and to increase clock speed)
Proximity-1 receiver	
FREQ_ACQUISITION_RANGE	Maximum detectable center frequency error. In Hz. (one-sided)
CLK_FREQUENCY	Synchronous CLK frequency in Hz
BER_INST	'1' to instantiate a Bit Error Rate Tester.
SIMULATION	true during simulation, false for synthesis.

Runtime dynamic configuration

The transmitter and receiver can be configured dynamically at runtime, in parallel (using the VHDL components input parameters).

The top-level components for parallel (I/O) configuration are:
COM1852_TX.vhd
COM1852_RX.vhd

Control registers (Receiver)

SIGNAL designates the I/O signal when configuring the VHDL component directly at its interface.

f_{clk} is the ADC sampling frequency

Demodulator (controls must be synchronous with CLK)	
Parameters	**Configuration**
Nominal input center frequency (f_c)	The nominal center frequency is a fixed frequency offset applied to the input samples. It is used for fine frequency corrections, for example to correct clock drifts. 32-bit signed integer (2's complement representation) expressed as $f_c * 2^{32} / f_{clk}$ **RECEIVER_CENTER_FREQ(31:0)**
Nominal symbol rate f_{symbol_rate}	Nominal symbol rate, defined as $f_{symbol\_rate} * 2^{32} / f_{clk}$ Clarification: this is the symbol rate after Bi-Phase L decoding, i.e. data symbol rate. **NOMINAL_SYMBOL_RATE(31:0)**
External AGC response time	Users can to optimize AGC response time while avoiding instabilities (depends on external factors such as gain signal filtering at the RF front-end and modulation symbol rate). The AGC_DAC gain control signal is updated as follows 0 = every symbol, 1 = every 2 input symbols, 2 = every 4 input symbols, 3 = every 8 input symbols, etc…. 10 = every 1000 input symbols. Valid range 0 to 14. **AGC_RESPONSE(4:0)**
CIC_R	Receiver decimation factor from f_{clk} to f_{clk}/R 1 to bypass. 0 is illegal, otherwise, nominal range is 1 to 16384. Usage: be careful not to decimate too much as the CIC decimation filter is not very sharp and thus can distort the modulated signal. Rule of thumb: the CIC filter output sampling rate should be > 8 samples per data symbol. **CIC_R(15:0)**
Spectrum inversion	Invert Q bit 0 = off 1 = on **DEMOD_CONTROL(0)**

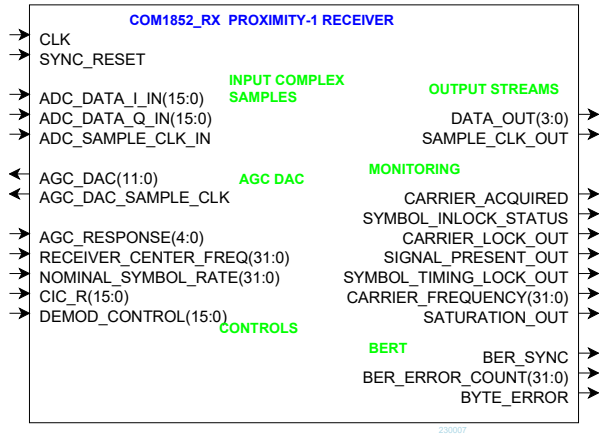
Control registers (Transmitter)

Modulator (controls must be synchronous with CLK)	
Parameters	**Configuration**
Symbol rate f_{symbol_rate}	Nominal symbol rate, defined as $f_{symbol\_rate} * 2^{32} / f_{clk}$ Clarification: this is the data symbol rate before Bi-Phase L encoding. **SYMBOL_RATE(31:0)**
Output Center frequency (f_{c_tx})	Fine tuning of center frequency. Typically 0 Hz. 32-bit signed integer (2's complement representation) expressed as $f_{c\_tx} * 2^{32} / f_{clk}$ For a clean output waveform, we recommend keeping the maximum frequency (center frequency + ½ symbol rate) below 1/10th of the processing clock f_{clk}. Note: as the AWGN noise samples are not frequency translated, noise tests should only be performed while the center frequency translation is smaller than the modulation bandwidth. **CENTER_FREQ(31:0)**
Digital Signal gain	16-bit amplitude scaling factor for the modulated signal. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Therefore, we recommend checking for saturation at the D/A converter when changing either the symbol rate or the signal gain. **GAIN(15:0)**
Additive White Gaussian Noise gain	16-bit amplitude scaling factor for additive white Gaussian noise. Because of the potential for saturation, please check for saturation at the D/A converter when changing this parameter. **NOISE_GAIN(15:0)**
Spectrum inversion	Invert Q bit. (Inverts the modulated spectrum only, not the subsequent frequency translation) 0 = off 1 = on **CONTROL(11)**
Test mode	00 = input is user data 01 = internal PRBS-11 test mode 10 = unmodulated carrier test mode **CONTROL(9:8)**

Status registers (Receiver)

Demodulator (synchronous with CLK)	
Carrier acquired	'1' when the receiver is locked to the received RF signal and '0' when not in lock. This status is a combination of carrier tracking lock and signal presence detection **CARRIER_ACQUIRED**
Symbol lock status	Combination of symbol timing loop lock and signal presence Solid 1 when locked, toggling when unlocked, 0 when no signal presence **SYMBOL_INLOCK_STATUS**
Signal presence detection	'1' when FFT detects the residual carrier. Reliable status. **SIGNAL_PRESENT_OUT**
Carrier frequency offset	Measured frequency offset with respect to the nominal carrier frequency. 32-bit signed integer expressed as $f_{cerror} * 2^{32} / f_{clk}$ **CARRIER_FREQUENCY**
BER	Number of bit errors over 80000 demodulated bits. (the 80000 bit window length can be changed in the generic section of the BER2.vhd component) Valid only when the BER tester is synchronized (BER_SYNC = '1') and the received signal is a PRBS11 test sequence. **BER_COUNT(31:0)**
BERT synchronized	1 when the BERT is synchronized. **BER_SYNC**
Byte error	1 CLK pulse for each wrong Byte detected by the BERT **BYTE_ERROR**
Saturation	monitor miscellaneous saturations bit 0: at receiver0 bit 1: FFT for signal detection bit 2: AGC bit 3: at half-band filter bit 4: resampling bit 5: raised cosine filter **SATURATION_OUT(8:0)**

I/Os



Receiver inputs

ADC_DATA_I/Q_IN(15:0): input samples from one or two external ADCs. (one in the case of IF undersampling, two for near-zero frequency complex inputs). If the ADCs have fewer than 16-bit precision, align the most significant bit with ADC_DATA_IN(15). Format: 2's complement (signed).

ADC_SAMPLE_CLK_IN: '1' when **ADC_DATA_I/Q_IN** is valid. Generally fixed at '1' when input is connected directly to ADCs.

AGC_DAC(11:0): output to an external DAC to control an external AGC. Gain control for the external analog/IF/RF front-end. May need to be inverted depending on the analog front-end. 12-bit unsigned. FFF represents the minimum gain, 000 the maximum gain.
Read when **AGC_DAC_SAMPLE_CLK** is '1'

The above signals are clock-synchronous with ADC sampling clock CLK.

Receiver output

DATA_OUT(3:0): 4 bit soft-quantized demodulator output. 4-bit sample format: 0000 most negative, 1111 most positive, with no zero representation.

DATA_OUT_VALID: 1 clock-wide pulse indicating that **DATA_OUT** is valid.

The output signals are synchronous with the CLK ADC sampling clock.

Transmitter inputs

DATA_IN(7:0): input data is read one Byte at a time.

DATA_IN_VALID: 1 clock-wide pulse indicating that **DATA_IN** is valid.

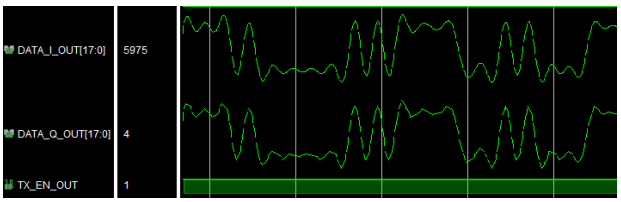
SOF_IN: optional Start Of Frame. 1 clock-wide pulse.

CTS_OUT: "Clear-To-Send" output flow-control signal. The data source should stop sending new Bytes when CTS_OUT = '0';

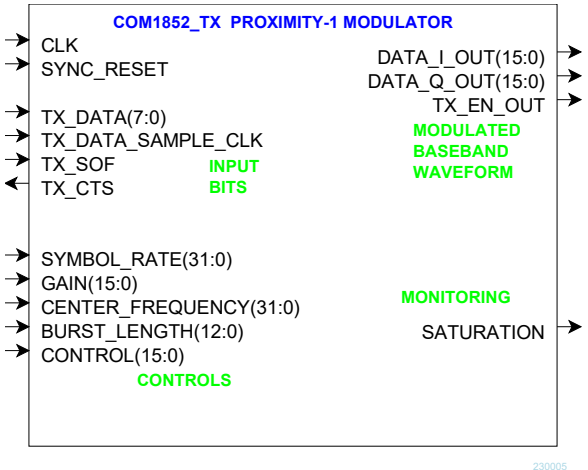
Transmitter outputs

DATA_I/Q_OUT(17:0): Modulated baseband output samples (I = in-phase, Q = quadrature). One output sample every clock. Format: 2's complement (signed)

TX_EN_OUT: goes low to turn off an external power amplifier when the modulator is active. It includes a timing margin at the start/end of burst.

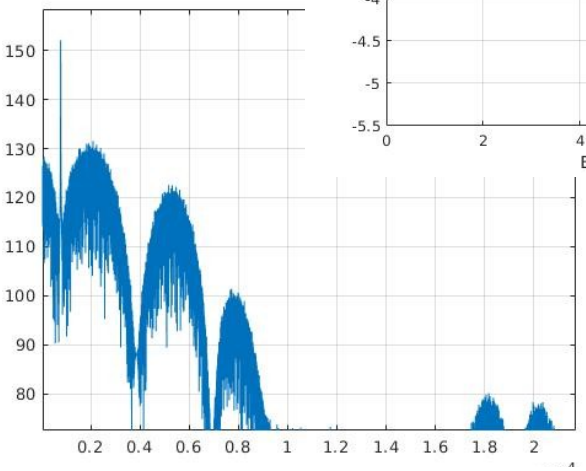


Transmitted spectrum: 32.768 Msamples/s, 64 Ksymbols/s data (Bi-Phase L encoded). Resolution 100Hz.

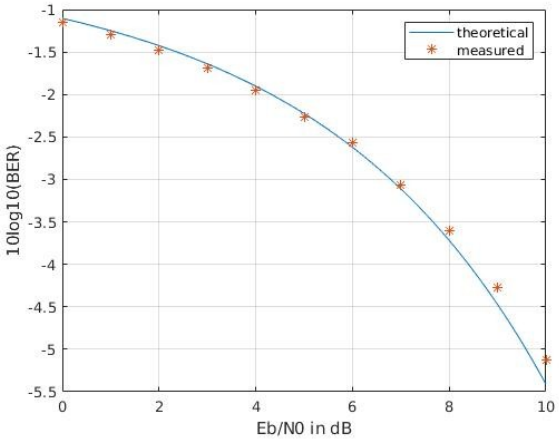


Performance

Output spectrum



Spectrum, symmetric around the residual carrier. No output filtering.



BER vs E_b/N_0 performance

The theoretical BER performance is shown as a blue line. It is generated by the Matlab function `berawgn(0:0.1:10,'psk',2,'nondiff')`

Actual modem BER measurements over 250ms are shown as red stars.

Operation

Clocks

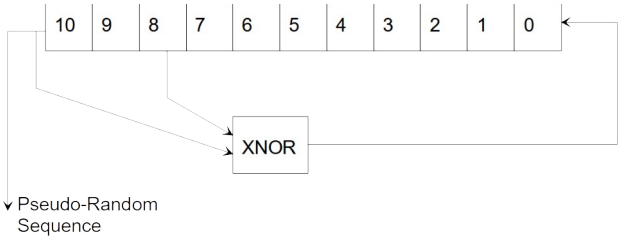
The transmitter COM1852_TX uses a single clock CLK which is the DAC interface sampling clock. The DAC sampling clock selection is independent of the transmit symbol rate.

Likewise, the receiver COM1852_RX uses a single clock which is the ADC sampling clock. Its selection is independent of the received symbol rate.

Both must be global clocks (i.e. go through BUFG global buffers in the FPGA).

Pseudo-Random Bit Stream (Test Pattern)

A periodic pseudo-random sequence can be used as modulator source instead of the input data stream. A typical use would be for end-to-end bit-error-rate measurement of a communication link. The sequence is 2047-bit long maximum length sequence generated by a 11-tap linear feedback shift register:



The first 100 bits of the PN sequence are as follows:
0000000000 0111111111 0011111110 0001111100
1100111000 0000010011 1111010001 1110110100
1101001100 0011000001

Format Conversion

Serial to parallel conversion occurs at the interface between the modem and the application, for example at TX_DATA(7:0) modulator input. The general rule is that the first received bit is placed at the MSb position in the byte.

Receiver AGC

To maintain linearity throughout the receive path, several AGC loops control the signal level. While most AGC loops are internal, an additional AGC loop is dedicated to controlling an external RF/IF/analog front-end.

The purpose of this AGC is to prevent saturation at the external A/D converter(s) while making full use of the A/D converter(s) dynamic range. The controlling signal **AGC_DAC(11:0)** can be read from the receiver status or can be connected directly to an external auxiliary DAC.

The AGC responsiveness can be adjusted using the **RECEIVER_AGC_RESPONSE(4:0)** control.

Software Licensing

The COM-1852SOFT is supplied under the following key licensing terms:

1. A nonexclusive, nontransferable license to use the VHDL source code internally, and
2. An unlimited, royalty-free, nonexclusive transferable license to make and use products incorporating the licensed materials, solely in bit stream format, on a worldwide basis.

The complete VHDL/IP Software License Agreement can be downloaded from http://www.comblock.com/download/softwarelicense.pdf

Configuration Management

The current software revision is 012424

Directory	Contents
/doc	Specifications, user manual, implementation documents
/src	.vhd source code,.pkg packages, .xdc constraint files (Xilinx) One component per file.
/sim	VHDL test benches
/matlab	Matlab.m file for simulating the encoding and decoding algorithms, for generating stimulus files for VHDL simulation, including channel impairments: noise, frequency error, Doppler rate, amplitude changes, etc.
com-1852data	A folder containing ready-to-use stimulus files for receiver VHDL simulation. Use in conjunction with the testbench /sim/tbcom1852_demodonly.vhd

Project files:

Xilinx Vivado v2020 project file:
project_1v2020.xpr
project_1v2020.tcl

VHDL development environment

The VHDL software was developed using the following development environment:

- Xilinx Vivado 2020 for synthesis, place and route and VHDL simulation

Device Utilization Summary

AWGN generator instantiated.

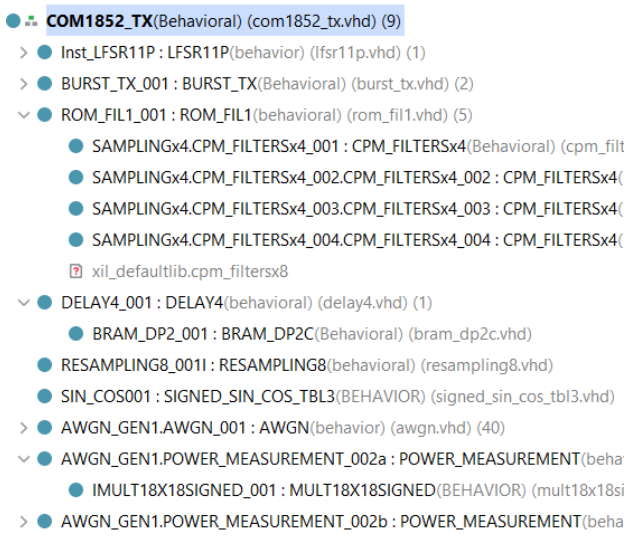
Transmitter COM1852_TX		Artix7-100T utilization
LUTs	6269	9.9%
Registers	2941	2.3%
Block RAM/FIFO 36Kb	9.5	7.0%
DSP	33	13.8%
GCLKs	1	3.1%

BER tester instantiated.

Receiver COM1852_RX		Artix7-100T utilization
LUTs	7528	11.9%
Registers	6941	5.5%
Block RAM/FIFO 36Kb	21.5	15.9%
DSP	64	26.7%
GCLKs	1	3.1%

VHDL components overview

Transmitter top level



COM1852_TX.vhd implements the digital PCM/Bi-Phase L/phase modulation. Its input consists of 8-bit parallel data bits, packed MSb first. Key controls include modulation symbol rate, output signal amplitude, output center frequency and additive noise generation. The modulated complex baseband signal output is in 16-bit 2's complement format at the DAC sampling rate.

The *BURST_TX.vhd* component stores input data in an elastic input buffer, then packs input bits into symbols (1 bit/symbol) at the specified symbol rate.

RESAMPLING8.vhd interpolates the modulated waveform from its native 8 samples/symbol to the DAC sampling rate. The interpolation is based on a 1024-step polyphase filter.

DIGITAL_DC3.vhd translates the modulated signal to a non-zero output center frequency, under the control of the 32-bit NCO *NCO32X.vhd*. The frequency translation uses *SIGNED_SIN_COS_TBL3.vhd* as sine/cosine look-up tables.

BRAM_DP2.vhd is a generic dual-port memory, used as input and output elastic buffers. Memory is inferred for code portability (no primitive is used).

Prior to the DAC, the digital waveform amplitude is adjusted by digital multiplers *MULT18X18SIGNED.vhd*.

Ancillary components

LFSR11P.vhd is a pseudo-random sequence generator used for test purposes. It generates a PRBS11 test sequence commonly used for bit error rate testing at the receiving end of a transmission channel.

AWGN.vhd generates a precise Additive White Gaussian Noise. The noise bandwidth is 2*symbol rate.

POWER_MEASUREMENT.vhd is used to provide independent power measurements for the modulated signal and the AWGN.

SIM2OUTFILE.vhd writes three 12-bit data variables to a tab delimited file which can be subsequently read by Matlab (load command) for plotting or analysis.

Receiver top level

COM1852_RX_001	COM1852_RX(Behavioral)
RECEIVER0_001	RECEIVER0(Behavioral)
RX_DETECT_001	RX_SIGNAL_DETECTION(Behavioral)
CIC_FILTER_001	CIC(behavioral)
CIC_FILTER_002	CIC(behavioral)
AGC21_002	AGC21(behavioral)
FIRHALFBAND32_I1	FIRHALFBAND32(Behavioral)
FIRHALFBAND32_Q1	FIRHALFBAND32(Behavioral)
PROXIMITY_1_DEMOD_001	PROXIMITY_1_DEMOD(behavioral)
phase_006	PROXIMITY_1_DEMOD(behavioral)
RESAMPLING71_001I	RESAMPLING71(behavioral)
RESAMPLING71_001Q	RESAMPLING71(behavioral)
phase_007	PROXIMITY_1_DEMOD(behavioral)
FIR_RC1_001I	FIR_RC1(Behavioral)
FIR_RC1_001Q	FIR_RC1(Behavioral)
phase_009	PROXIMITY_1_DEMOD(behavioral)
SIN_COS001	SIGNED_SIN_COS_TBL3(BEHAVIOR)
phase_010	PROXIMITY_1_DEMOD(behavioral)
CARRIER_TRACK2_003	CARRIER_TRACKING2_1852(behavior
ST_LOOP_003	SYMBOL_TIMING_LOOP5(BEHAVIOR)
MF001	MATCHED_FILTERNx1(Behavioral)
sim2outfile_x	PROXIMITY_1_DEMOD(behavioral)
PX_TO_P8_CONVERSION_003	PX_TO_P8_CONVERSION(behavioral)

RECEIVER0.vhd is the front-end digital receiver which processes digital samples from the A/D converter(s). It performs non modulation-specific tasks, including bias removal, internal and external AGC and fixed frequency translation to (near-zero) baseband. Input digital samples can be complex (in the case of baseband input samples) or real (in the case of IF undersampling). This generic component is not modulation-specific. When enabled, it can control the gain of the external RF/IF front-end receiver.

RX_SIGNAL_DETECTION.vhd detects the received signal presence and estimates the center frequency. The received signal is first low-pass filtered in a CIC decimation filter to reduce the frequency span to 2*frequency acquisition window, then fed into a 2048-point FFT. The decimation factor controls the receiver frequency acquisition range (here +/- 80 KHz). Upon signal detection, the measured SIGNAL_CENTER_FREQUENCY is used to translate the received signal to near-zero frequency baseband in *RECEIVER0.vhd* . The residual frequency error is thus (+/- 2*frequency acquisition window / 2048) = +/- 80 Hz

The near-zero frequency signal undergoes Low-Pass Filtering and decimation through a CIC decimation filter *CIC.vhd*. The decimation ratio is computed so that the resulting sampling rate is slightly but strictly larger than 8*data symbol rate.

Following the *RECEIVER0* front-end, the received signal undergoes CIC decimation filtering (*CIC.vhd*), where the signal is Low-Pass Filtered, then decimated down to slightly more than 8 samples per symbol.

AGC21.vhd normalizes the signal level, since a significant portion of the noise was rejected in the CIC decimation filter.

FIRHALFBAND32.vhd provides some additional low-pass filtering in a half-band FIR filter.

PROMITY_1_DEMOD.vhd performs typical tasks for a coherent demodulation, namely carrier recover, frequency translation to zero center frequency, symbol timing recovery, resampling at exactly 4 samples per symbol and AGC.

The carrier tracking loop (*CARRIER_TRACKING_1852.vhd*) approximates the phase error as DATA10Q when measured at the center of the Bi-Phase L coded symbol. A second-order loop ensues. The PLL loop gains are configured to acquire the +/- 80 Hz residual center frequency error (based on the *RX_SIGNAL_DETECTION.vhd* FFT resolution). The convergence time is typically 100ms. The second-order branch reports the residual frequency error *FREQ_ERROR.* The second-order loop gain LOOP_GAIN2 may be adjusted to meet specific application requirements in terms of Doppler rate.

The carrier tracking loop is reset while the receiver is in STATE 1 (i.e. before FFT signal detection and coarse frequency estimate)

The symbol timing recovery loop *SYMBOL_TIMING_LOOP61.vhd* is a second-order Gardner loop based on the DATA10Q signal sampled twice per symbol. It is configured to acquire a symbol rate error of more than 100ppm. A much larger symbol rate error (up to 1%) can be acquired during the idle signal by detecting the periodic sync marker (see *MATCHED_FILTERNx1.vhd*)

Two small circuits are added to ensure detection and removal of (a) a 0/180deg carrier phase ambiguity and (b) a ½ symbol timing ambiguity.

The 0x352EF853 sync marker (when not FEC encoded) is detected by the *MATCHED_FILTERNx1.vhd* component. Depending on the application, the sync marker could be FEC encoded or not. Therefore, it is up to the user to move and connect this component after the FEC decoder if applicable.

The sync marker detection pulses are use to perform a coarse symbol rate acquisition, thus reducing the symbol rate error from the maximum 1% down to 100ppm or less. The remaining error is 'mopped up' by *SYMBOL_TIMING_LOOP61.vhd*

Ancillary components

INFILE2SIM.vhd reads up to 3 input signals from a text file (input.txt) formatted as 12-bit tab delimited signals.

BER2.vhd is a bit error rate tester expecting to receive a PRBS11 test sequence. It synchronizes with the received bit stream and count errors over a user-defined window. It can be placed immediately after the demodulator, or after the error correction.

VHDL simulation

Two VHDL testbenches are located in the /sim directory.

The `tbcom1852_modemonly.vhd` connects the modulator and demodulator back to back. End-to-end BER tests can be performed as the `com1852_tx.vhd` transmitter includes a built-in pseudo-random sequence generator and the `com1852_rx.vhd` receiver includes a built-in Bit Error Rate Tester.

The `tbcom1852_demodonly.vhd` testbench reads a tab-delimited stimulus files of modulated I/Q baseband complex input samples. The stimulus file *index.txt* is typically generated by a matlab .m program such as `siggen_proximity1.m` in the /matlab folder.

Matlab simulation

Matlab programs are located in the /matlab directory.

The `siggen_proximity1.m` program generates a stimulus file `input.txt` for use as input to the demodulator VHDL simulation (`tbcom1852_demodonly.vhd`). The stimulus file includes a continuous stream of pseudo-random (PRBS11) data bits, additive white Gaussian noise, channel filtering, frequency translation and quantization.

Care must be taken to match the modulator configuration in `siggen_proximity1 .m` and the demodulator configuration in `tbcom1852_demodonly.vhd`.

This setup allows end-to-end BER testing, as the demodulator com1852_rx.vhd includes a built-in bit error rate tester.

The Matlab program demod_ber_pm.m plots theoretical vs actual BER measurements as a function of the E_b/N_0.

The following stimulus waveform files can be downloaded from comblock.com/download/VHDL/COM-1852SOFT/. Use test1.txt file with the tbcom1852_demodonly_test1 testbench in the sim folder, etc.

test1.txt	Over the air 16KSymbols/s E_b/N_0. 20 dB Center frequency offet: 0 Hz Symbol rate offset: 0 Hz Duration: 250ms Carrier: 62.5us Idle sequence: 20ms Data: 230ms ADC sampling rate 32.768KS/s
test2	Over the air 16KSymbols/s E_b/N_0. 8 dB Center frequency offet: 75KHz, 100Hz/s Symbol rate offset: 0 Hz Duration: 250ms Carrier: 10ms Idle sequence: 20ms Data: 220ms ADC sampling rate 32.768KS/s
test3	Over the air 256KSymbols/s E_b/N_0. 5 dB Center frequency offet: 75KHz, 100Hz/s Symbol rate offset: 0 Hz Duration: 250ms Carrier: 10ms Idle sequence: 10ms Data: 230ms ADC sampling rate 32.768KS/s
test4	Over the air 1024KSymbols/s E_b/N_0. 5 dB Center frequency offet: 20KHz, 75Hz/s Symbol rate offset: 0 Hz Duration: 250ms Carrier: 10ms Idle sequence: 10ms Data: 230ms ADC sampling rate 32.768KS/s
test5	Over the air 4096KSymbols/s E_b/N_0. 0 dB Center frequency offet: -81KHz, -200Hz/s Symbol rate offset: 0 Hz Duration: 250ms Carrier: 10ms Idle sequence: 10ms Data: 230ms ADC sampling rate 32.768KS/s

Specifications

[1] CCSDS "Proximity-1 Space Link Protocol: Physical layer", CCSDS 211.1-B-4, December 2013

[2] CCSDS "Proximity-1 Space Link Protocol: coding and synchronization sublayer", CCSDS 211.2-B-3, October 2019

Acronyms

Acronym	Definition
ADC	Analog to Digital Converter
AWGN	Additive White Gaussian Noise
BRAM	Dual-port Block RAM
BER	Bit Error Rate
BERT	Bit Error Rate Tester
CCSDS	Consultative Committee for Space Data Systems
DAC	Digital to Analog Converter
DVB	Digital Video Broadcast
FPGA	Field Programmable Gate Arrays
LSb	Least Significant bit
LSB	Least Significant Byte
M&C	Monitoring and Control
MSb	Most Significant bit
MSB	Most Significant Byte
N/A	Not Applicable
NCO	Numerically Control Oscillator
PRBS-11	Pseudo-Random Binary Sequence, 2047-bit period
R_{cs}	Coded symbol rate
R_{chs}	Channel symbol rate
SoC	System on Chip
UART	Universal Asynchronous Receiver/Transmitter

ComBlock Ordering Information

COM-1852SOFT CCSDS Proximity-1 modem, , VHDL source code / IP core

- transmit-only
- receive-only
- tx/rx bundle

ECCN: EAR99

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