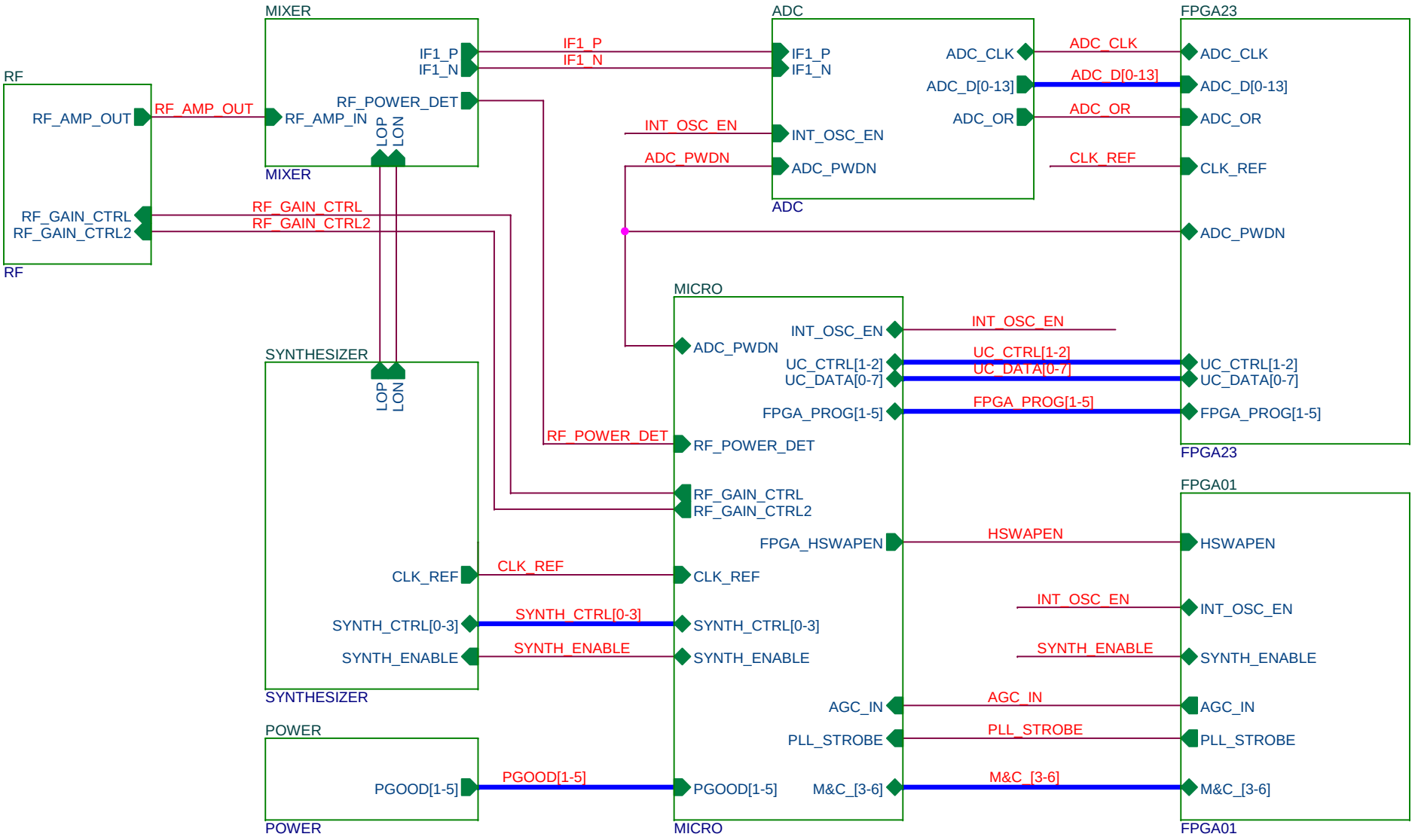


TABLE OF CONTENTS

MAIN.....1
ADC.....2
FPGA01.....3
FPGA23.....4
MICRO..... 5
MIXER..... 6
POWER..... 7
RF..... 8
SYNTHESIZER..... 9

General Layout Notes:
- use RC0603 for all 0603
- use RC0402 for all 0402
- Label all TPs' names on SST

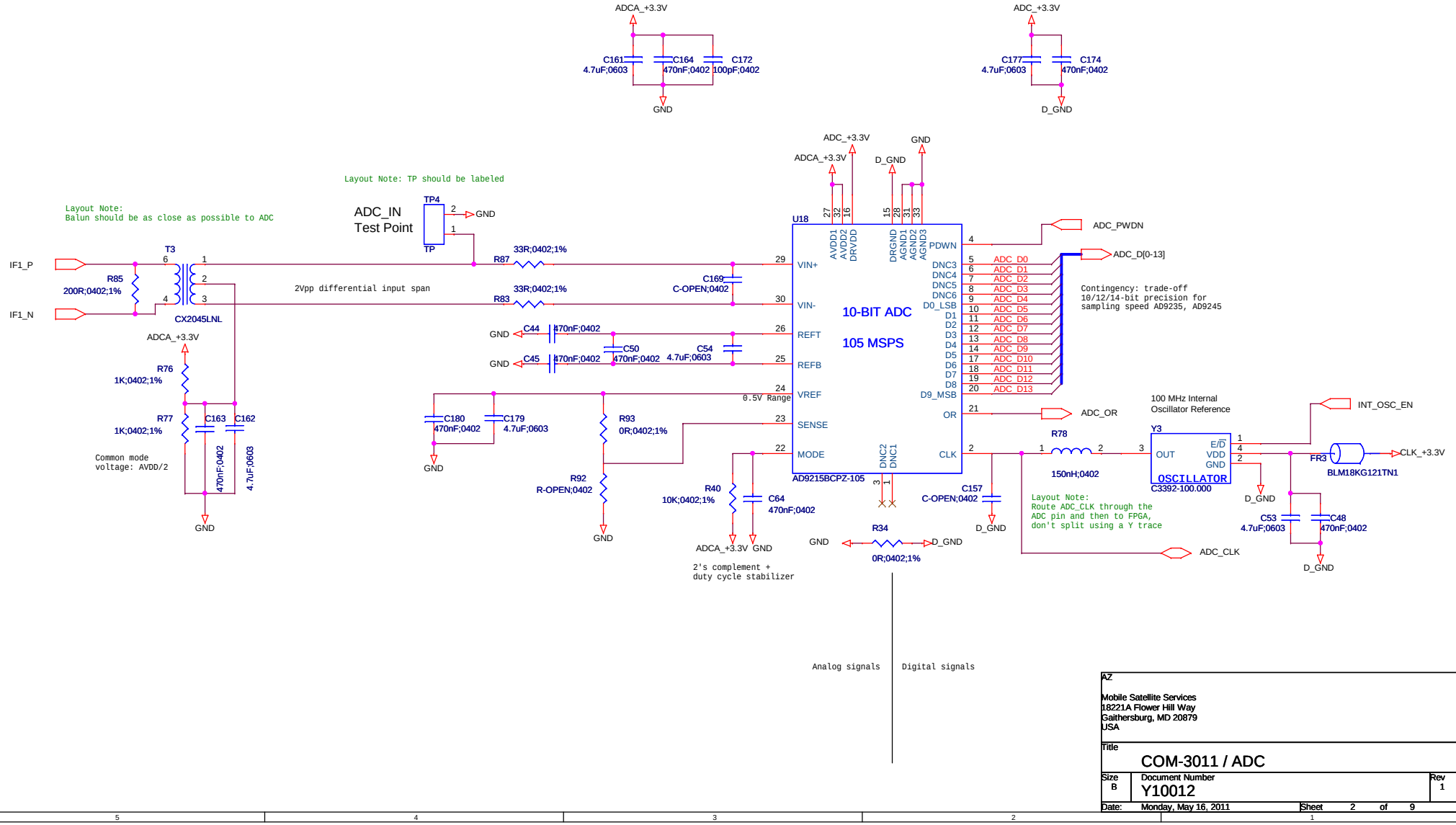
AZ

Mobile Satellite Services
18221A Flower Hill Way
Gaithersburg, MD 20879
USA

Title: COM-3011 / MAIN

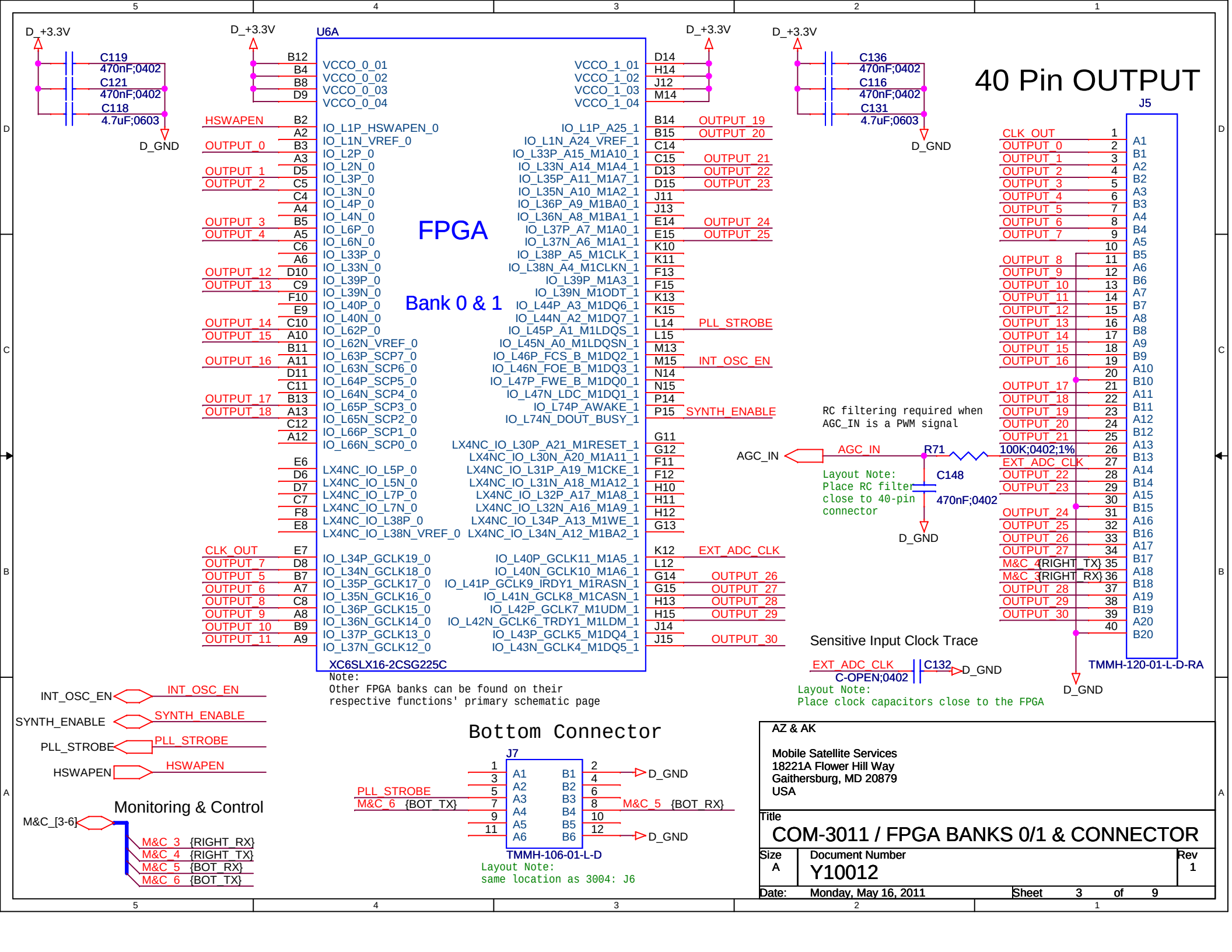
Size	Document Number	Rev
A	Y10012	1

Date: Monday, May 16, 2011 Sheet 1 of 9



AZ	
Mobile Satellite Services 18221A Flower Hill Way Gaithersburg, MD 20879 USA	
Title	COM-3011 / ADC
Size: B	Document Number: Y10012 — Rev: 1
Date: Monday, May 16, 2011	Sheet 2 of 9

40 Pin OUTPUT



AZ & AK

Mobile Satellite Services
18221A Flower Hill Way
Gaithersburg, MD 20879
USA

Title

COM-3011 / FPGA BANKS 0/1 & CONNECTOR

Size	Document Number	Rev
A	Y10012	1

Date: Monday, May 16, 2011 Sheet 3 of 9

Note:
Other FPGA banks can be found on their
respective functions' primary schematic page

U6B

FPGA

Bank 2 & 3

D2	VCCO_3_01	VCCO_2_01	M7
G4	VCCO_3_02	VCCO_2_02	P12
H2	VCCO_3_03	VCCO_2_03	P4
M2	VCCO_3_04	VCCO_2_04	P8
M4	IO_L1P_3	PROGRAM_B_2	R2
L3	IO_L1N_VREF_3	IO_L1P_CCLK_2	N12
P2	IO_L2P_3	IO_L3N_MOSI_CSI_B_MISO0_2	R11
P1	IO_L2N_3	IO_L48N_RDWR_B_VREF_2	R6
N2	IO_L37P_M3DQ0_3	DONE_2	R14
N1	IO_L37N_M3DQ1_3	IO_L65P_INIT_B_2	P3
M3	IO_L38P_M3DQ2_3	SUSPEND	L13
M1	IO_L38N_M3DQ3_3	CMPCS_B_2	L10
L2	IO_L39P_M3LDQS_3		
L1	IO_L39N_M3LDQSN_3	IO_L3P_D0_DIN_MISO_MISO1_2	P11
K3	IO_L40P_M3DQ6_3	IO_L12P_D1_MISO2_2	M11
K1	IO_L40N_M3DQ7_3	IO_L12N_D2_MISO3_2	N11
K5	IO_L45P_M3A3_3	IO_L49P_D3_2	P5
J4	IO_L45N_M3ODT_3	IO_L49N_D4_2	R5
F3	IO_L46P_M3CLK_3	IO_L62P_D5_2	L6
F1	IO_L46N_M3CLKN_3	IO_L62N_D6_2	L5
E2	IO_L52P_M3A8_3	IO_L48P_D7_2	N6
E1	IO_L52N_M3A9_3		
D4	IO_L53P_M3CKE_3	IO_L1N_M0_CMPMISO_2	R12
E3	IO_L53N_M3A12_3	IO_L13P_M1_2	N10
D3	IO_L54P_M3RESET_3		
D1	IO_L54N_M3A11_3		
C2	IO_L83P_3	IO_L2P_CMPCLK_2	P13
C1	IO_L83N_VREF_3	IO_L2N_CMPMOSI_2	R13
J5		IO_L14P_D11_2	L9
H4	LX4NC_IO_L47P_M3A0_3	IO_L14N_D12_2	M10
G5	LX4NC_IO_L47N_M3A1_3	IO_L16P_2	P9
G3	LX4NC_IO_L48P_M3BA0_3	IO_L16N_VREF_2	R9
H6	LX4NC_IO_L48N_M3BA1_3	IO_L63P_2	N4
H5	LX4NC_IO_L49P_M3A7_3	IO_L63N_2	R4
F5	LX4NC_IO_L49N_M3A2_3	IO_L64P_D8_2	M5
F4	LX4NC_IO_L50P_M3WE_3	IO_L64N_D9_2	N5
E5	LX4NC_IO_L50N_M3BA2_3	IO_L13N_D10_2	R10
E4	LX4NC_IO_L51P_M3A10_3	IO_L65N_CSO_B_2	R3
	LX4NC_IO_L51N_M3A4_3		M9
J2		LX4NC_IO_L15P_2	N9
J1	IO_L41P_GCLK27_M3DQ4_3	LX4NC_IO_L15N_2	L7
H3	IO_L41N_GCLK26_M3DQ5_3	LX4NC_IO_L47P_2	M6
H1	IO_L42P_GCLK25_TRDY2_M3UDM_3	LX4NC_IO_L47N_2	
K4	IO_L42N_GCLK24_M3LDM_3		N8
J3	IO_L43P_GCLK23_M3RASN_3	IO_L29P_GCLK3_2	R8
G2	IO_L43N_GCLK22_IRDY2_M3CASN_3	IO_L29N_GCLK2_2	M8
G1	IO_L44P_GCLK21_M3A5_3	IO_L30P_GCLK1_D13_2	N7
	IO_L44N_GCLK20_M3A6_3	IO_L30N_GCLK0_USERCCLK_2	K8
		IO_L31P_GCLK31_D14_2	L8
A14		IO_L31N_GCLK30_D15_2	P7
E10	TCK	IO_L32P_GCLK29_2	R7
D12	TDI	IO_L32N_GCLK28_2	
E13	TDO		
	TMS		

JTAG inputs internally pulled-up, see ug380 Ch. 5

XC6SLX16-2CSG225C

R68
0R;0402;1%
JTAG Disabled
D_GND

D_+3.3V
D_+3.3V
C140 470nF;0402
C135 470nF;0402
C149 4.7uF;0603
D_GND

R2 {PROGB} FPGA_PROG1
N12 {ALE_CCLK} UC_CTRL1
R11 {CSIB} FPGA_PROG5
R6 {REB_RDWRB} UC_CTRL2
R14 {DONE} FPGA_PROG2
P3 {INITB} FPGA_PROG3
L13 {SUSPEND} FPGA_PROG4
TP1 DONE

L10 D_+3.3V

UC_DATA[0-7]
P11 UC_DATA0
M11 UC_DATA1
N11 UC_DATA2
P5 UC_DATA3
R5 UC_DATA4
L6 UC_DATA5
L5 UC_DATA6
N6 UC_DATA7

µC Interface

R12 D_GND
N10 D_+3.3V
Slave SelectMAP Programming Configuration

ADC_D[0-13]
P13 ADC_D13
R13 ADC_D12
L9 ADC_D11
M10 ADC_D10
P9 ADC_D9
R9 ADC_D8
N4 ADC_D7
R4 ADC_D6
M5 ADC_D5
N5 ADC_D4
R10 ADC_D3
R3 ADC_D2

N8 ADC_D0
R8 ADC_D1
N7 ADC_PWDN
K8 ADC_OR
P7 ADC_CLK
R7 CLK_REF

Sensitive Input Clock Trace

UC_CTRL1 {ALE_CCLK} C142 C-OPEN;0402 D_GND

Layout Note:
Place clock capacitors close to the FPGA

FPGA CONFIGURATION

D_+3.3V R28 4.7K;0402;1% FPGA_PROG1 {PROGB}
D_+3.3V R31 R-OPEN;0402 UC_CTRL1 {ALE_CCLK}
D_GND R30 R-OPEN;0402
D_+3.3V R32 330R;0402 FPGA_PROG2 {DONE}
D_+3.3V R29 4.7K;0402;1% FPGA_PROG3 {INITB}

Layout Note:
- Route UC_CTRL1 as 50ohm trace
- place termination R-OPENs closest to FPGA

FPGA Programming

FPGA_PROG[1-5]
FPGA_PROG1 {PROGB}
FPGA_PROG2 {DONE}
FPGA_PROG3 {INITB}
FPGA_PROG4 {SUSPEND}
FPGA_PROG5 {CSIB}

UC_CTRL[1-2]
UC_CTRL1 {ALE_CCLK}
UC_CTRL2 {REB_RDWRB}

CLK_REF CLK_REF

CLK_REF: 20 MHz Sampling clock
(from synthesizer's oscillator)

ADC_CLK ADC_CLK

ADC_CLK: 100 MHz Input sampling clock (from internal oscillator) or TBD MHz from FPGA PLL

ADC_PWDN ADC_PWDN
ADC_OR ADC_OR

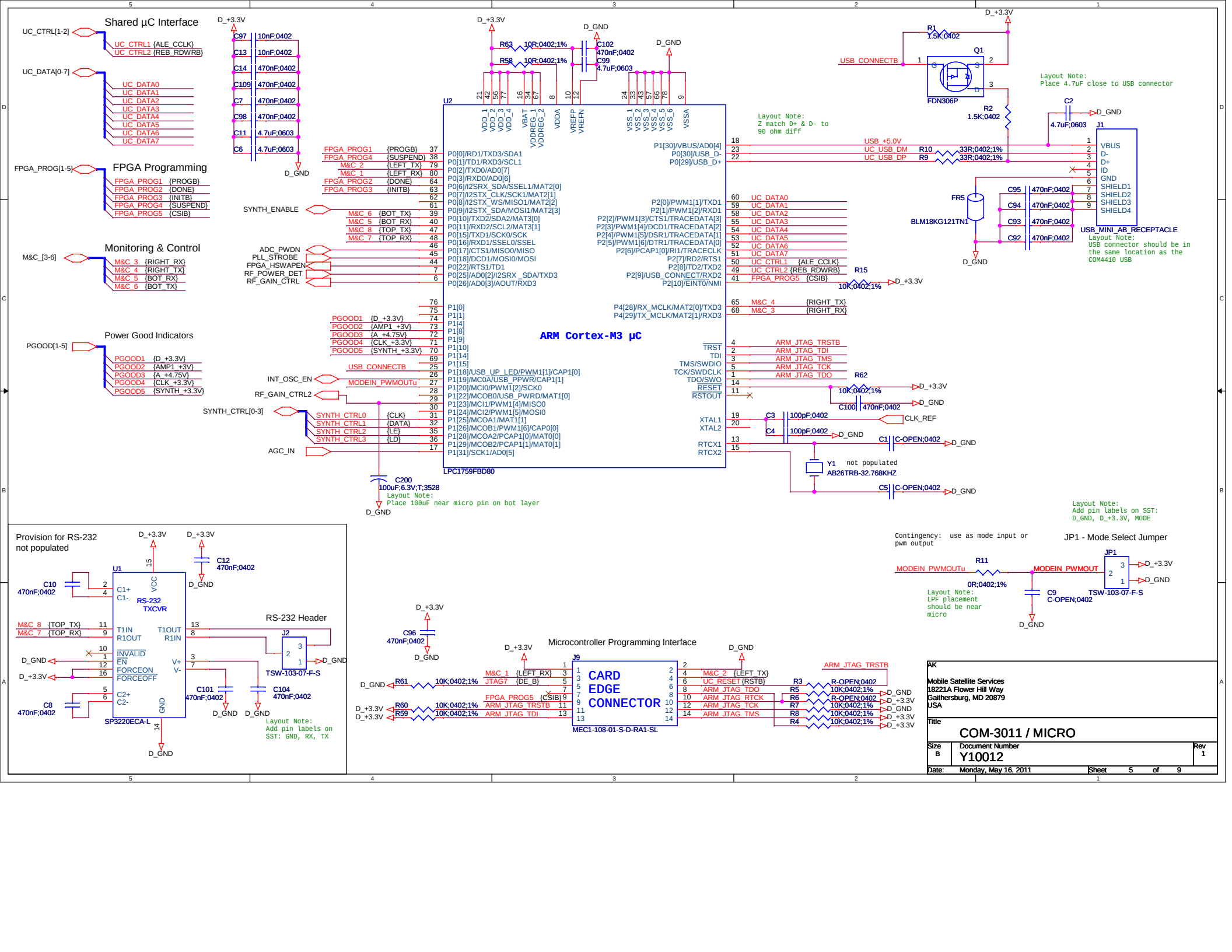
AK & AZ

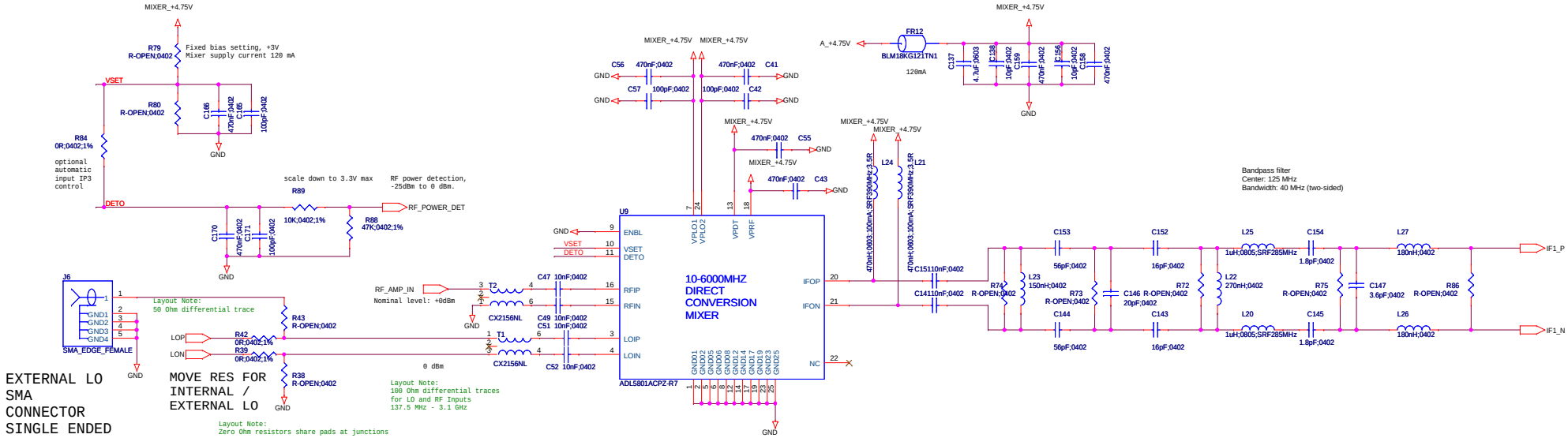
Mobile Satellite Services
18221A Flower Hill Way
Gaithersburg, MD 20879
USA

Title
COM-3011 / FPGA BANKS 2/3

Size	Document Number	Rev
A	Y10012	1

Date: Monday, May 16, 2011 Sheet 4 of 9


Shared µC Interface
UC_CTRL[1-2]
UC_CTRL1 {ALE_CCLK}
UC_CTRL2 {REB_RDWRB}
UC_DATA[0-7]
UC_DATA0
UC_DATA1
UC_DATA2
UC_DATA3
UC_DATA4
UC_DATA5
UC_DATA6
UC_DATA7
FPGA Programming
FPGA_PROG[1-5]
FPGA_PROG1 {PROGB}
FPGA_PROG2 {DONE}
FPGA_PROG3 {INITB}
FPGA_PROG4 {SUSPEND}
FPGA_PROG5 {CSIB}
Monitoring & Control
M&C_[3-6]
M&C_3 {RIGHT_RX}
M&C_4 {RIGHT_TX}
M&C_5 {BOT_RX}
M&C_6 {BOT_TX}
Power Good Indicators
PGOOD[1-5]
PGOOD1 {D_+3.3V}
PGOOD2 {AMP1_+3V}
PGOOD3 {A_+4.75V}
PGOOD4 {CLK_+3.3V}
PGOOD5 {SYNTH_+3.3V}
D_+3.3V
D_GND
C97 10nF;0402
C13 10nF;0402
C14 470nF;0402
C109 470nF;0402
C7 470nF;0402
C98 470nF;0402
C11 4.7uF;0603
C6 4.7uF;0603
R63 10R;0402;1%
R58 10R;0402;1%
C102 470nF;0402
C99 4.7uF;0603
U2
ARM Cortex-M3 µC
LPC1759FBD80
VDD_1
VDD_2
VDD_3
VDD_4
VBAT
VDDREG_1
VDDREG_2
VDDA
VREFP
VREFN
VSS_1
VSS_2
VSS_3
VSS_4
VSS_5
VSS_6
VSSA
FPGA_PROG1 {PROGB}
FPGA_PROG4 {SUSPEND}
M&C_2 {LEFT_TX}
M&C_1 {LEFT_RX}
FPGA_PROG2 {DONE}
FPGA_PROG3 {INITB}
SYNTH_ENABLE
M&C_6 {BOT_TX}
M&C_5 {BOT_RX}
M&C_8 {TOP_TX}
M&C_7 {TOP_RX}
ADC_PWDN
PLL_STROBE
FPGA_HSWAPEN
RF_POWER_DET
RF_GAIN_CTRL
PGOOD1 {D_+3.3V}
PGOOD2 {AMP1_+3V}
PGOOD3 {A_+4.75V}
PGOOD4 {CLK_+3.3V}
PGOOD5 {SYNTH_+3.3V}
USB_CONNECTB
INT_OSC_EN
MODEIN_PWMOUTu
RF_GAIN_CTRL2
SYNTH_CTRL[0-3]
SYNTH_CTRL0 {CLK}
SYNTH_CTRL1 {DATA}
SYNTH_CTRL2 {LE}
SYNTH_CTRL3 {LD}
AGC_IN
C200
100uF;6.3V;T;3528
Layout Note:
Place 100uF near micro pin on bot layer
P0[0]/RD1/TXD3/SDA1
P0[1]/TD1/RXD3/SCL1
P0[2]/TXD0/AD0[7]
P0[3]/RXD0/AD0[6]
P0[6]/I2SRX_SDA/SSEL1/MAT2[0]
P0[7]/I2STX_CLK/SCK1/MAT2[1]
P0[8]/I2STX_WS/MISO1/MAT2[2]
P0[9]/I2STX_SDA/MOSI1/MAT2[3]
P0[10]/TXD2/SDA2/MAT3[0]
P0[11]/RXD2/SCL2/MAT3[1]
P0[15]/TXD1/SCK0/SCK
P0[16]/RXD1/SSEL0/SSEL
P0[17]/CTS1/MISO0/MISO
P0[18]/DCD1/MOSI0/MOSI
P0[22]/RTS1/TD1
P0[25]/AD0[2]/I2SRX_SDA/TXD3
P0[26]/AD0[3]/AOUT/RXD3
P1[0]
P1[1]
P1[4]
P1[8]
P1[9]
P1[10]
P1[14]
P1[15]
P1[18]/USB_UP_LED/PWM1[1]/CAP1[0]
P1[19]/MC0A/USB_PPWR/CAP1[1]
P1[20]/MCI0/PWM1[2]/SCK0
P1[22]/MCOB0/USB_PWRD/MAT1[0]
P1[23]/MCI1/PWM1[4]/MISO0
P1[24]/MCI2/PWM1[5]/MOSI0
P1[25]/MCOA1/MAT1[1]
P1[26]/MCOB1/PWM1[6]/CAP0[0]
P1[28]/MCOA2/PCAP1[0]/MAT0[0]
P1[29]/MCOB2/PCAP1[1]/MAT0[1]
P1[31]/SCK1/AD0[5]
P1[30]/VBUS/AD0[4]
P0[30]/USB_D-
P0[29]/USB_D+
P2[0]/PWM1[1]/TXD1
P2[1]/PWM1[2]/RXD1
P2[2]/PWM1[3]/CTS1/TRACEDATA[3]
P2[3]/PWM1[4]/DCD1/TRACEDATA[2]
P2[4]/PWM1[5]/DSR1/TRACEDATA[1]
P2[5]/PWM1[6]/DTR1/TRACEDATA[0]
P2[6]/PCAP1[0]/RI1/TRACECLK
P2[7]/RD2/RTS1
P2[8]/TD2/TXD2
P2[9]/USB_CONNECT/RXD2
P2[10]/EINT0/NMI
P4[28]/RX_MCLK/MAT2[0]/TXD3
P4[29]/TX_MCLK/MAT2[1]/RXD3
TRST
TDI
TMS/SWDIO
TCK/SWDCLK
TDO/SWO
RESET
RSTOUT
XTAL1
XTAL2
RTCX1
RTCX2
USB_+5.0V
UC_USB_DM
UC_USB_DP
UC_DATA0
UC_DATA1
UC_DATA2
UC_DATA3
UC_DATA4
UC_DATA5
UC_DATA6
UC_DATA7
UC_CTRL1 {ALE_CCLK}
UC_CTRL2 {REB_RDWRB}
FPGA_PROG5 {CSIB}
M&C_4 {RIGHT_TX}
M&C_3 {RIGHT_RX}
ARM_JTAG_TRSTB
ARM_JTAG_TDI
ARM_JTAG_TMS
ARM_JTAG_TCK
ARM_JTAG_TDO
R62 10K;0402;1%
C100 470nF;0402
C3 100pF;0402
C4 100pF;0402
CLK_REF
C1 C-OPEN;0402
Y1 not populated
AB26TRB-32.768KHZ
C5 C-OPEN;0402
R15 10K;0402;1%
Layout Note:
Z match D+ & D- to
90 ohm diff
R1 Y.5K;0402
Q1
FDN306P
USB_CONNECTB
R2 1.5K;0402
C2 4.7uF;0603
Layout Note:
Place 4.7uF close to USB connector
J1
VBUS
D-
D+
ID
GND
SHIELD1
SHIELD2
SHIELD3
SHIELD4
USB_MINI_AB_RECEPTACLE
Layout Note:
USB connector should be in
the same location as the
COM4410 USB
R10 33R;0402;1%
R9 33R;0402;1%
FR5
BLM18KG121TN1
C95 470nF;0402
C94 470nF;0402
C93 470nF;0402
C92 470nF;0402
Layout Note:
Add pin labels on SST:
D_GND, D_+3.3V, MODE
Contingency: use as mode input or
pwm output
JP1 - Mode Select Jumper
JP1
TSW-103-07-F-S
R11 0R;0402;1%
MODEIN_PWMOUT
C9 C-OPEN;0402
Layout Note:
LPF placement
should be near
micro
Provision for RS-232
not populated
U1
RS-232
TXCVR
SP3220ECA-L
C10 470nF;0402
C12 470nF;0402
C8 470nF;0402
C101 470nF;0402
C104 470nF;0402
RS-232 Header
J2
TSW-103-07-F-S
Layout Note:
Add pin labels on
SST: GND, RX, TX
C96 470nF;0402
Microcontroller Programming Interface
J9
CARD
EDGE
CONNECTOR
MEC1-108-01-S-D-RA1-SL
M&C_1 {LEFT_RX}
JTAG7 {DE_B}
FPGA_PROG5 {CSIB}
ARM_JTAG_TRSTB
ARM_JTAG_TDI
M&C_2 {LEFT_TX}
UC_RESET {RSTB}
ARM_JTAG_TDO
ARM_JTAG_RTCK
ARM_JTAG_TCK
ARM_JTAG_TMS
R61 10K;0402;1%
R60 10K;0402;1%
R59 10K;0402;1%
R3 R-OPEN;0402
R5 10K;0402;1%
R6 R-OPEN;0402
R7 10K;0402;1%
R8 10K;0402;1%
R4 10K;0402;1%
AK
Mobile Satellite Services
18221A Flower Hill Way
Gaithersburg, MD 20879
USA
Title
COM-3011 / MICRO
Size B
Document Number
Y10012
Rev 1
Date: Monday, May 16, 2011
Sheet 5 of 9



EXTERNAL LO
SMA
CONNECTOR
SINGLE ENDED

MOVE RES FOR
INTERNAL /
EXTERNAL LO

Layout Note:
Zero Ohm resistors share pads at junctions

AZ		
Mobile Satellite Services 18221A Flower Hill Way Gaithersburg, MD 20879 USA		
Title	COM-3011 / MIXER	
Size: C	Document Number: Y10012	Rev: 1
Date: Monday, May 16, 2011	Sheet 6 of 9	

+5V Supply

Green Terminal Block
OPERATIONAL RANGE: 4.9 - 5.5V

J3 — BATT+ / BATT- — 1757475

FR6 BLM18KG121TN1

Reverse Voltage Protection

Q2 FDN306P

TVS

D5 SMBJ5.0A-E3

Over Voltage Protection (5.85V)

Layout Note: Q2 & Q4 must be placed and routed for a high current throughput.

Q4 FMMT718TA

Q3 FMMT718TA

D4 BZX84C5V1

R56 499R;0402;1%
R55 10K;0402;1%
R57 1K;0402;1%

Layout Note: TVS component placed near Over Voltage Protection circuit away from terminal block

Layout Note: Place Vin caps as close as possible to Vin and PGND pins

C108 10nF;0402
C105 4.7uF;0603
C106 4.7uF;0603
C103 3.3nF;0402

NCP1599MNTWG DC/DC converter:

3A max peak output current
1MHz switching

U15 NCP1599 3A DC/DC Converter — NCP1599MNTWG

R65 3.65K;0402;1%
R64 10K;0402;1%
R66 5.1K;0402;1%

L18 6.8uH;3.1A — Ityp = ~1.5A Vout = 1.21V

C107 100uF;6.3V;T;3528
C110 4.7uF;0603
C111 4.7uF;0603
C112 470nF;0402
C113 4.7uF;0603

FR7 BLM18KG121TN1

D_+1.2V
ATTN_+1.2V

Layout Note: Place 0 Ohm resistors near LRs

R12 0R;0402;1% — return path

Vin

U13 — Imax = 90mA Vout = 3.31V

LP3982IMM-ADJ NOPB

C89 4.7uF;0603
C82 470nF;0402
R50 165K;0402;1%
R53 100K;0402;1%
C91 470nF;0402
C80 100uF;6.3V;T;3528
C75 4.7uF;0603
C70 470nF;0402

FR4 BLM18KG121TN1 — D_+3.3V
ADCA_+3.3V 40mA
C71 4.7uF;0603

FR13 BLM18KG121TN1 — ADC_+3.3V 11mA
C176 4.7uF;0603

PGOOD1 {D_+3.3V}

U16 — Imax = 36mA Vout = 3.00V

R67 0R;0402;1%

LP3982IMM-ADJ NOPB

C124 4.7uF;0603
C125 470nF;0402
R70 140K;0402;1%
R69 100K;0402;1%
C130 470nF;0402
C126 4.7uF;0603
C129 470nF;0402

AMP1_+3V — First 2 RF stages

PGOOD2 {AMP1_+3V}

U17 — Imax = 215mA Vout = 4.75V

LP3982IMM-ADJ NOPB

C155 4.7uF;0603
C150 470nF;0402
R81 280K;0402;1%
R82 100K;0402;1%
C160 470nF;0402
C167 4.7uF;0603
C168 470nF;0402

A_+4.75V — RF amps, mixer, gain control

PGOOD3 {A_+4.75V}

U20 — Imax = 90mA Vout = 3.31V

LP3982IMM-ADJ NOPB

C199 4.7uF;0603
C197 470nF;0402
R101 165K;0402;1%
R100 100K;0402;1%
C192 470nF;0402
C189 4.7uF;0603
C195 470nF;0402

CLK_+3.3V

PGOOD4 {CLK_+3.3V}

U19 — Imax = 90mA Vout = 3.31V

LP3982IMM-ADJ NOPB

C198 4.7uF;0603
C196 470nF;0402
R99 165K;0402;1%
R102 100K;0402;1%
C193 470nF;0402
C191 4.7uF;0603
C194 470nF;0402

FR15 BLM18KG121TN1 — SYNTH_+3.3V
SYNTHA_+3.3V
C190 4.7uF;0603

R98 0R;0402;1%

PGOOD5 {SYNTH_+3.3V}

FPGA Power

C127 4.7uF;0603
C128 4.7uF;0603
C133 4.7uF;0603
C122 470nF;0402
C114 4.7uF;0603
C123 4.7uF;0603
C115 470nF;0402
C139 470nF;0402
C134 4.7uF;0603

U6C — FPGA Supply

XC6SLX16-2CSG225C

Power Good Indicators

PGOOD[1-5]

PGOOD1 {D_+3.3V}
PGOOD2 {AMP1_+3V}
PGOOD3 {A_+4.75V}
PGOOD4 {CLK_+3.3V}
PGOOD5 {SYNTH_+3.3V}

PCB Mounting Holes

H2 H4 H3 H1

Power Requirements (*TBC)

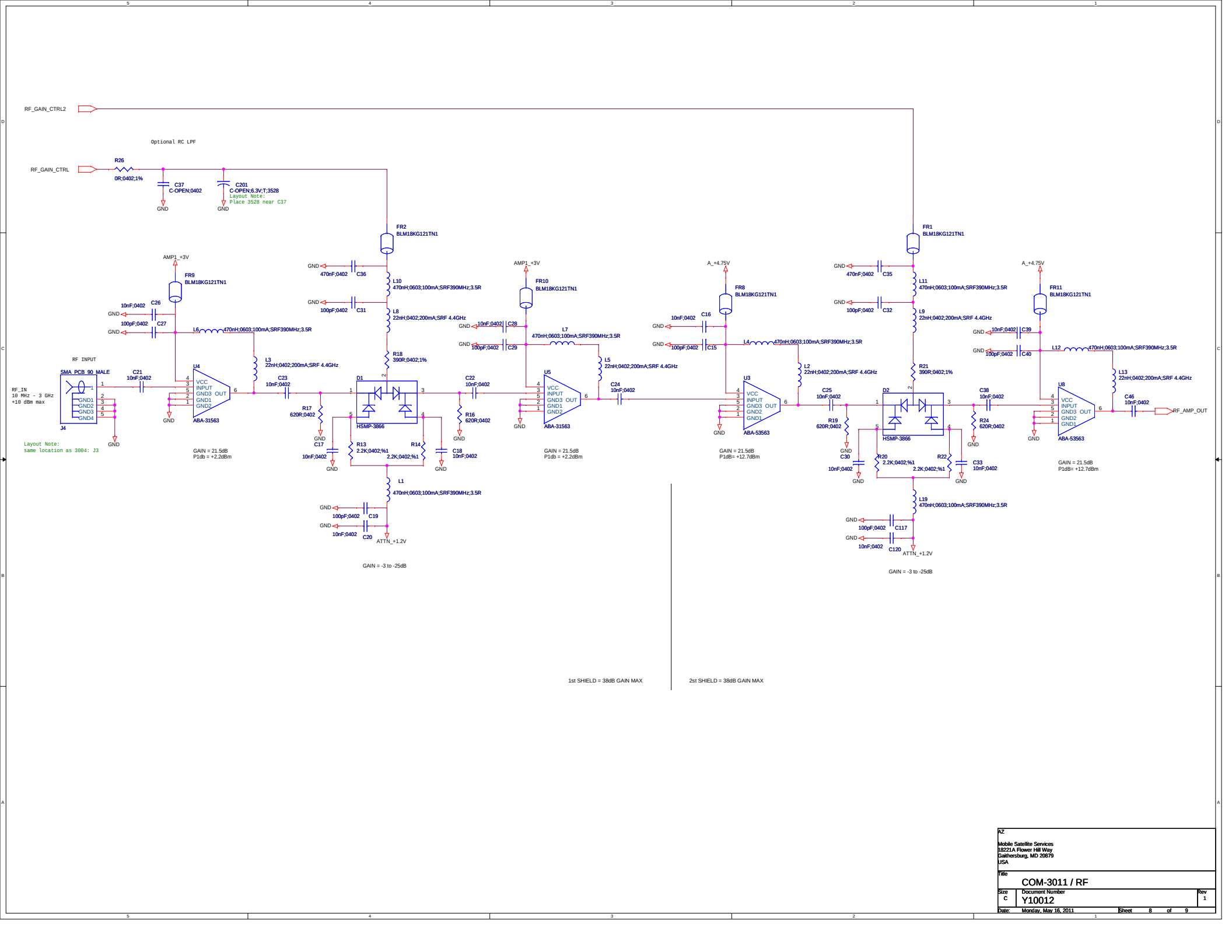
COMP	V	mA
RF AMP1	+3.0	36
RF AMP2	+4.75	215
FPGA	+3.3	100*
MICRO	+3.3	90*
ADC	+3.3	50
FPGA	+1.2	1500

AK
Mobile Satellite Services
18221A Flower Hill Way
Gaithersburg, MD 20879
USA

Title: COM-3011 / POWER

Size: B | Document Number: Y10012 | Rev: 1

Date: Monday, May 16, 2011 | Sheet 7 of 9



AZ		
Mobile Satellite Services 18221A Flower Hill Way Gaithersburg, MD 20879 USA		
Title	COM-3011 / RF	
Size: C	Document Number: Y10012	Rev: 1
Date: Monday, May 16, 2011	Sheet 8 of 9	

EXTERNAL FREQUENCY REFERENCE

Layout Note:
SMA edge location should be
the same with COM4410 SMA location

10/20 MHz frequency reference.
0.6Vpp min, 3.3Vpp max

J8
SMA_EDGE_FEMALE
GND1 GND2 GND3 GND4
C90 470nF;0402
R52 10K;0402;1%
R54 12.4K;0402;1%
D3 TZM5227B
3.6V Zener: Prevent over/under-voltage damage to NC7SZ04 at analog inputs.
C83 470nF;0402
U14 NC7SZ04P5X
R47 0R;0402;1%
C79 470nF;0402
U12 NC7SZ04P5X
C72 4.7uF;0603
C66 470nF;0402
C63 C-OPEN;0402
SYNTH_CTRL[0-3]
SYNTH_CTRL0 {CLK} R41 10R;0402;1% 1
SYNTH_CTRL1 {DATA} R37 10R;0402;1% 2
SYNTH_CTRL2 {LE} R35 10R;0402;1% 3
SYNTH_CTRL3 {LD} R46 10R;0402;1% 25
SYNTH_PLL_LOCK {MUXOUT} R44 10R;0402;1% 30
Layout note:
Route the sensitive 20MHz_REF & 20MHz_REF_IN traces away from noise sources
20MHz_REF
C74 10nF;0402
20MHz_REF_IN
C76 C-OPEN;0402
R48 1M;0402;1%
R49 499R;0402;1%
Y2 20MHz CSA309
C183 33pF;0402
C188 22pF;0402
Layout note:
Crystal uses "laydown" footprint
No traces under component
U10 NC7SZ04P5X
C68 470nF;0402
R36 33R;0402;1%
CLK_REF
TP3 TP_SMALL
CLK REF testpoint
R33 0R;0402;1%
Layout note:
Label Testpoints
SYNTH_PLL_LOCK {MUXOUT} 1
TP2 TP_SMALL
PLL LOCK testpoint
FR14 BLM18KG121TN1
R90 0R;0402;1%
C182 4.7uF;0603
C87 10pF;0402
C84 470nF;0402
U11 ADF4350BCPZ
V_VCO1 V_VCO2 AVDD VP DVDD SDVDD CE CPGND AGND AGND_VCO1 AGND_VCO2 AGND_VCO3 EXPAD DGND SDGND
CLK DATA LE LD MUXOUT REF_IN RSET PDBRF
RF_OUTB+ RF_OUTB- RF_OUTA- RF_OUTA+ VTUNE CPOUT SW VREF VCOM TEMP
Frequency Synthesizer
R51 4.7K;0402;1%
SYNTH_ENABLE
R96 R-OPEN;0402
R45 R-OPEN;0402
L17 L14 L16 L15
470nH;0603;100mA;SRF390MHz;3.5R
22nH;0402;200mA;SRF 4.4GHz
21mA
C78 10nF;0402
C73 10nF;0402
LOP
LON
Layout note:
RF_OUT/LO traces are
100 Ohm diff. impedance matched
R97 820R;0402;1%
C86 680pF;0402
Fast Lock Mode
R94 0R;0402;1%
C62 1.5nF;0402
C173 22nF;0402
R91 113R;0402;1%
R95 340R;0402;1%
C175 C58 C59 C65 C69
C181 C60 C61 C77 C51 C178 C67
C186 C187 C184 C185 C85 C88
10pF;0402
470nF;0402
4.7uF;0603
SYNTHA_+3.3V
SYNTH_+3.3V
CLK_+3.3V
D_GND
GND

AK & AZ
Mobile Satellite Services
18221A Flower Hill Way
Gaithersburg, MD 20879
USA

Title: COM-3011 / SYNTHESIZER

Size	Document Number	Rev
B	Y10012	1

Date: Monday, May 16, 2011 Sheet 9 of 9