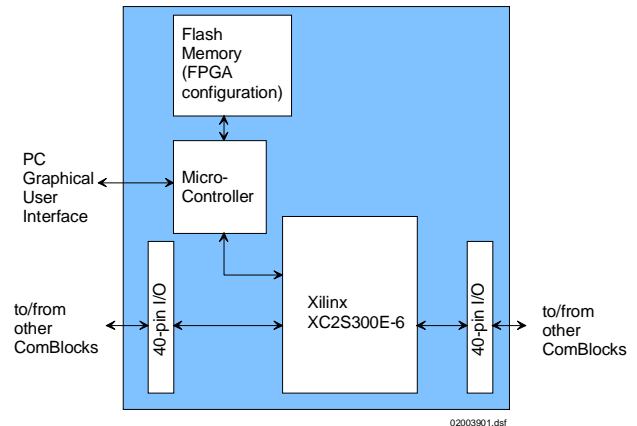


## COM-8000 FPGA / VHDL DEVELOPMENT PLATFORM & SODIMM SOCKET

### Key Features

- Develop custom signal processing applications on FPGA in VHDL language using this generic development platform.
- Xilinx Spartan-IIe XC2S300E-6 FPGA features 93,000 system gates and 64Kbit of dual port memory.
- The FPGA is suitable for synchronous signal processing at 80 MHz.
- SODIMM socket for SDRAM or other modules.
- Modules can be stacked for large VHDL design development.
- FPGA configuration remains in non-volatile flash memory and is automatically reloaded at power up.
- Graphical User Interface is used for remote monitoring and control over simple serial link. This includes loading FPGA configuration file into flash. No special cable nor serial EPROM is needed.
- This module is interface compatible with other pre-programmed ComBlock modules.
- Microprocessor automatically configures FPGA at power up.
- 40 MHz on-board oscillator or external clock selection. Use FPGA DLL to double the clock speed for 80 MHz processing.
- Single 5V supply with reverse voltage and overvoltage protection. Connectorized 3"x3" module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right).

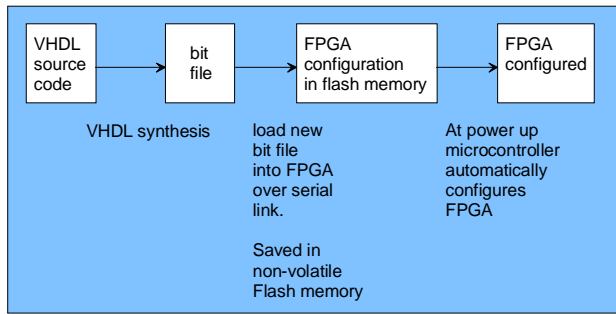


**Block Diagram**

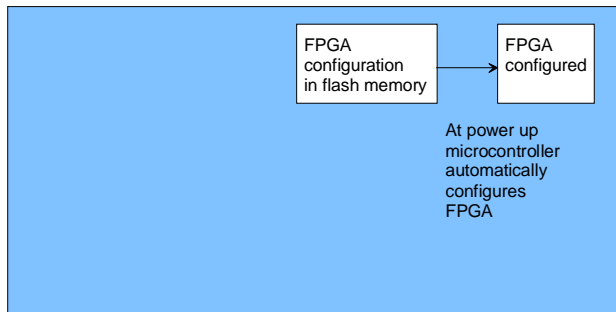


For the latest data sheet, please refer to the **ComBlock** web site: [www.comblock.com/download/com8000.pdf](http://www.comblock.com/download/com8000.pdf). These specifications are subject to change without notice.

## Application Development Process



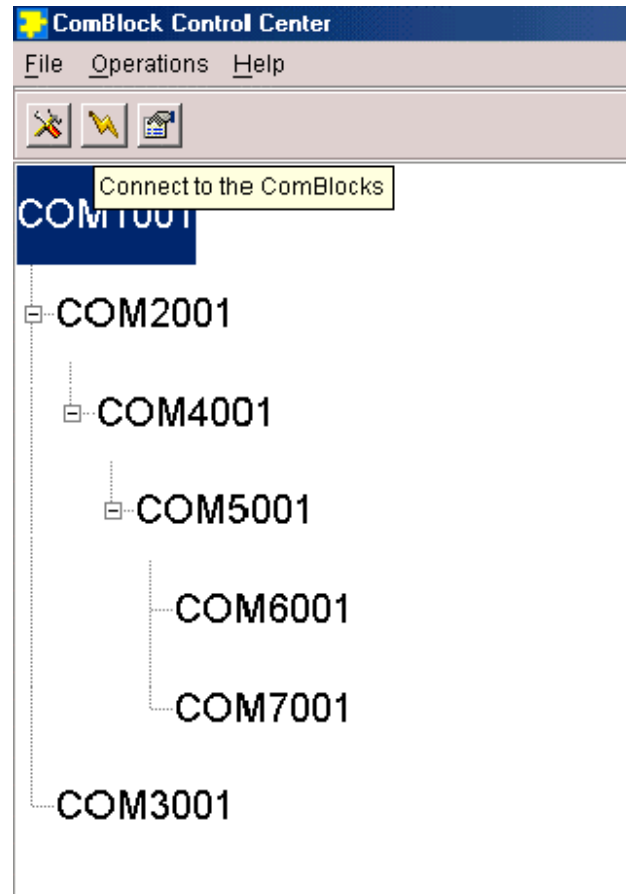
*Development environment.*



*Run-time environment..*

## Graphical User Interface

When activated, the GUI enumerates the ComBlock modules within the assembly. The modules are identified by their name in a tree-like structure. Each module can be configured and monitored remotely.



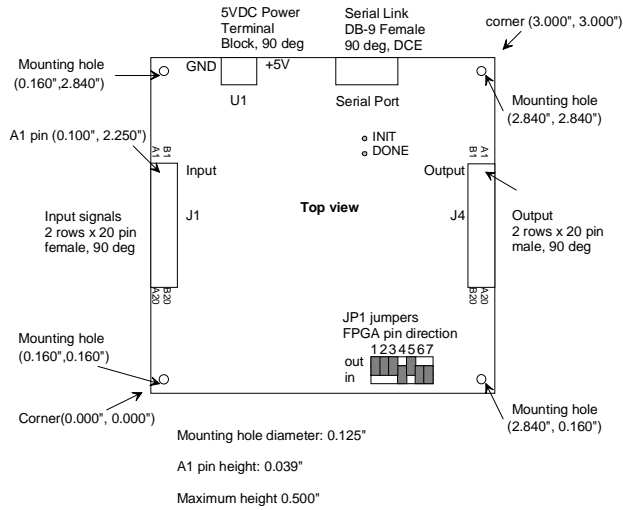
The ComBlock Control Center software is provided with all ComBlock modules. The user's manual can be found at

[www.comblock.com/download/ccchelp.pdf](http://www.comblock.com/download/ccchelp.pdf)

## Electrical Interface

| Interfaces                             | Definition  |
|--|---|
| J1(27:2)                               | J1 connector (left)<br>J1(27:21) shares FPGA pins with J4(26:21) & J4(19). This input/output selection is selected by jumpers.  |
| J4(26:1)                               | J4 connector (right)  |
| <b>Serial Monitoring &amp; Control</b> | DB9 connector.<br>115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.   |
| <b>Power Interface</b>                 | 4.75 – 5.25VDC. Terminal block.<br>Power consumption is approximately proportional to the CLK frequency.<br>The maximum power consumption at 80 MHz is typically less than 600mA. |

## Mechanical Interface



## Schematics

The board schematics are available on-line at [www.comblock.com/download/com\\_8001schematics.pdf](http://www.comblock.com/download/com_8001schematics.pdf).

## VHDL code template

A VHDL project template is available on-line at TBD. It includes a VHDL source code for a SDRAM driver, the VHDL top-level template and the Xilinx constraint file (.ucf).

## I/Os

**Important: The I/O signals connected directly to the FPGA are NOT 5V tolerant!**

## Shared FPGA pins

Due to the limited number of I/O pins in the FPGA, seven pins are shared between the J1 input connector and the J4 output connector. Selection is done by using the JP1 jumper as illustrated below:

| FPGA pin | J1 pin | J4 pin |
|----------|--------|--------|
| 201      | J1(21) | J4(19) |
| 200      | J1(22) | J4(21) |
| 203      | J1(23) | J4(22) |
| 202      | J1(24) | J4(23) |
| 205      | J1(25) | J4(24) |
| 204      | J1(26) | J4(25) |
| 206      | J1(27) | J4(26) |

## Test Points

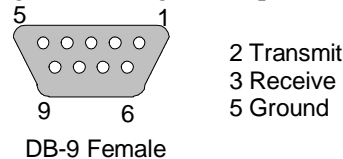
Proper FPGA configuration can be verified by checking that the DONE test point is high. It typically takes 5 seconds after power up for the FPGA configuration to be complete.

When connecting the INIT test point to ground, the FPGA is prevented from configuring.

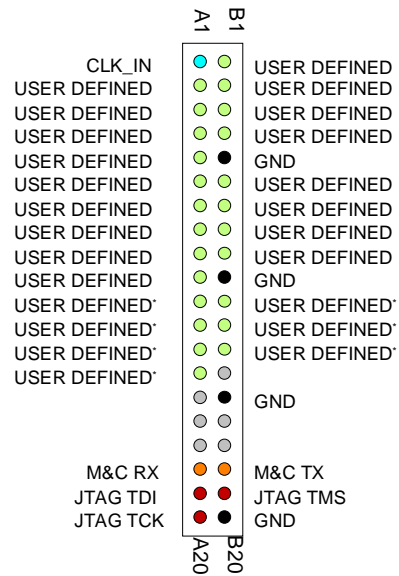
## Pinout

### Serial Link

The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



### (Input) Connector J1



(\* Shared FPGA pin: Input / Output is jumper selectable.

Note: although the J1 connector is generally referred to as 'Input', individual user-defined pins can be configured as 'IN', 'OUT', or 'INOUT' in the user VHDL source code.

