#### Com Block **Rapid Prototyping Communication Modules** BASEBAND BASEBAND MODULATOR DIGITAL RF / ANALOG DEMODULATOR ERROR FEC FRAME ENCODING CORRECTION ORMATTING TO ANALOG / RF TO DIGITAL FRAME FORMATTING RECEIVER BASEBAND CHANNEL PERFORMANCES IMPAIREMENTS INTERFACE 2 MEASUREMENT

# Rapid Prototyping

**ComBlock** is an innovative approach to developing communication equipment. Low-cost building blocks pre-programmed with essential communication processing functions can be daisy-chained to form complex communication equipment.

The **ComBlock** architecture is aimed at rapid prototyping, developing software-defined radios and building cost-effective low-volume semi-custom equipment.

The layered organization of communication systems is reflected in the **ComBlock** modules available: the **ComBlock** family includes network, digital, analog and radio frequency functions. Technologies span FPGAs, ARM processors, analog and RF, all connecting seamlessly.

**ComBlocks** can be assembled in a three dimensional structure for maximum volume efficiency.

A single LAN, USB, CardBus or serial connection allows remote monitoring and control of the entire assembly from the ComBlock control center software (included), irrespective of the number of constituent modules.

New FPGA software versions can be downloaded into the modules from the ComBlock control center.



Most modules are in-stock and typically ship within 24 – 48 hours.



3"x3" low-power modem development board

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### FPGA Development Platforms

In addition to the off-the-shelf pre-programmed modules, users can develop custom applications by using interface compatible FPGA development modules (COM-1800, 1700, 1500, 3011, 1400, 1300, 1200) with large parallel computation capabilities. Multiple **FPGA** configurations (personalities) can be programmed into the board Flash memory using the supplied ComBlock control center software. The FPGA is configured automatically at power up.

For even larger FPGA projects, several modules can be concatenated.

FPGA modules are best suited for recursive highlyparallel time-critical signal processing such as highspeed modulation or demodulation.

# ARM Development Platforms

32-bit ARM processors provide additional sequential computation capabilities in several modules (COM-1700, 1500, 3011, 3505). These modules complement FPGA-based modules by providing flexible, memory-intensive processing.

# Path to Production

Project evolution from prototyping to larger production runs is made easy by the availability of reasonably-priced VHDL source code. Price and availability for the most common VHDL IP cores are listed at

www.comblock.com/product\_list\_IP.html

### Modularity

To maximize interoperability among **ComBlocks**, the interfaces are restricted to four main connector types:

- 98-pin PCI express
- 40-pin headers (standard 2mm, 2 rows \* 20 positions)
- SMA
- UMCC (ultra miniature coaxial)

Likewise, for maximum interoperability, baseband signals are generally represented as one of two simple 'natural' interfaces:

- 2 \* 10/12/14-bit complex (In-phase and Quadrature) baseband interface, or - analog baseband (I & Q) interface and gain controls.

These simple 'natural' interfaces maximize the number of possible combinations between RF and digital signal processing modules and facilitate the interface with user-supplied (i.e. non-ComBlock) components.

For example, a digital demodulator can be connected to many interchangeable RF receivers, depending on the frequency band of interest, as illustrated below:



# **ComBlock Family**

#### Analog / IF / RF Front-End

Module	Definition	
<u>COM-3506</u>	[400 MHz – 3 GHz] customizable	
	transceiver	
<u>COM-1700</u>	Baseband, 70 MHz or 140 MHz	
	receiver.	
	SDR development platform	
<u>COM-3505</u>	Dual-ban 2.4/5 GHz 2x2 MIMO	
	transceiver.	
<u>COM-3504</u>	Dual Analog <-> Digital	
	conversions, including	
	dual 16-bit 250 MS/s DACs	
	dual 12-bit 150 MS/s ADCs	
<u>COM-2001</u>	Dual Digital-to-Analog conversion	
	and anti-aliasing filtering, up to 125	
	Msamples/s.	
<u>COM-2802</u>	Synchronized 8-channel 900	
	Msamples/s digital to analog	
	conversion.	
<u>COM-3010</u>	[925 – 2175 MHz] receiver.	
	LNB compatible.	
<u>COM-3011</u>	[20 MHz – 3 GHz] receiver.	
	SDR development platform.	
<u>COM-3007</u>	[2.3 – 2.8GHz] receiver. A/D	
	conversion up to 105 Msamples/s.	
<u>COM-3008</u>	[0 – 200 MHz] receiver.	
	10-bit 210 Msamples/s A/D	
	converters, AGC and low phase-	
	noise synthesized sampling clock.	
	Well suited for IF undersampling as	
	well as baseband sampling.	
<u>COM-3009</u>	Similar to COM-3008 but with 12-	

	bit precision, 105 Msamples/s
<u>COM-3501</u>	1W UHF Transceiver [225-400
	MHz] for two-way half-duplex
	communications
<u>COM-4410</u>	[70 MHz – 2.2GHz] 4-channel
	quadrature modulators
COM-40xx	Radio-Frequency modulators in-
	cluding low-phase noise frequency
	synthesizer, direct I/Q modulation,
	optional output power measure-
	ment.
<u>COM-4001</u>	Dual-band 915 MHz and 2.4 GHz
	modulator
<u>COM-4003</u>	L-band 1500 - 1740 MHz
	modulator
<u>COM-4005</u>	Cellular band [800 - 1000 MHz]
	modulator
<u>COM-4006</u>	PCS frequency band [1850 - 2050
	MHz] modulator
<u>COM-4008</u>	L-band 850 - 1600 MHz modulator
<u>COM-4101</u>	RF Transmit Redundancy module:
	Software controlled A/B swith
	directs RF to one of two paths.
	10MHz – 1.5 GHz, 17 dB gain,
	$P_{1dB} = 9.5 \text{ dB}$
<u>COM-4103</u>	L/S-band 10W power amplifier +
	LNA

#### Modulators

Module	Definition
<u>COM-1402</u>	PSK/QAM/APSK digital modulator
	up to 22 MSymbols/s. Includes
<u></u>	pseudo-random bit stream
	generator. USB 2.0 data interface.
<u>COM-1519</u>	Direct-sequence spread-spectrum
	digital modulator. Up to 60
<u></u>	Mchip/s.
	Spreading codes: Gold sequences,
	LFSR sequences, Barker codes, or
	GPS C/A codes.
<u>COM-1028</u>	FSK/MSK/GFSK/GMSK digital
	modulator. 2-,4-,8-ary.
III ***	Programmable data rates (up to 30
	Mbit/s), modulation index, BT
	product (0.3 and 0.5).

# Demodulators, Modems

Module	Definition
<u>COM-1518</u> NEW	Direct Sequence Spread-Spectrum
	digital demodulator. Up to 60
11 000 00	Mchip/s. Fast parallel acquisition.
	Maximum processing gain: 33 dB.
	Spreading factor: 3 to 2047
	Maximal code period: 65535
<u>COM-1505</u> NEW	Integrated PSK modem, including
	PSK modulation, demodulation,
<u></u>	convolutional error correction
	encoding and decoding, V.35
	scrambling, HDLC framing, TCP-
	IP network interface and USB 2.0
	interface
<u>COM-1202</u>	PSK/QAM/APSK digital/analog
	modulator and demodulator up to
<u></u>	22 MSymbols/s. Includes built-in
	BER measurement, and pseudo-
	random bit stream generator. USB
	2.0 data interface.
<u>COM-1203</u>	Same as above plus 10/100 Mbits/s
	LAN/TCP-IP interface.
<u> </u>	
<u>COM-1027</u>	FSK/MSK/GFSK/GMSK digital
	demodulator. 2-,4-,8-ary.
<u>COM-1008</u>	Variable decimation: 1:1024.
	AGC control. Pilot tone detection
	for frequency calibration. Used as
	pre-processing for low-data rate
	demodulators to prevent aliasing.

# **Error Correction**

Module	Definition
<u>COM-1510SOFT</u>	Block error correction codec, 100-
	250 Mbits/s. Convolutional
	encoding, Viterbi decoding.
	K=5,6,7,9.
	2 to 5 parity bits
	GMR-1 3G compatible
	(IP, VHDL source code)
COM-1209ASOFT	1Gbit/s BCH encoder/decoder.
	DVB-S2 standard.
	(IP, VHDL source code)
<u>COM-1509</u>	Error correction codec, 120 Mbits/s.
	Convolutional encoding, Viterbi
	decoding. K=5,7,9.
	V.35 scrambling.
	HDLC framing.
	K = 5, rate $1/7$
	K = 7, rates 1/2, 2/3, 3/4, 5/6, 7/8
	K = 9, rates 1/3, 1/2, 2/3
<u>COM-7002</u>	Turbo code encoder / decoder.
	Includes unique word frame
	synchronization, interleaving,
	scrambling and CRC.
<u>COM-1006</u>	Reed-Solomon Encoder
	DVB standard, Intelsat standard,
	other commonly used RS codes.

# Network / Baseband Interfaces

Module	Definition
<u>COM-5401</u>	4-port 10/100/1000 MBps Ethernet
	Transceivers for FPGA-based
	ComBlock modules (COM-1600,
	COM-1500). 4 RJ-45 ports.
<u>COM-5102</u>	1-port Gigabit Ethernet
	(10/100/1000) + HDMI video in/out
	for FPGA-based ComBlock
	modules (COM-1500). 1 RJ-45
	ports, 2 HDMI ports.
<u>COM-5003</u>	TCP-IP / USB Gateway.
	Connects ComBlock assemblies to a
	host computer over USB 2.0 or
	LAN TCP-IP (10Base-T/100Base-
	Tx). Supports 3 concurrent TCP-IP
	sockets for high-speed data (2) and
	monitoring and control (1).
	Maximum sustained throughput 53
	Mbit/s over TCP-IP, 86 Mbit/s over
	USB 2.0.
<u>COM-5404</u>	IP Router.
	Typical application: UDP video
	streaming to/from a synchronous
	data link.
<u>COM-5101</u>	Signal/Power conditioning interface
	module. Supports 4 full-duplex
	RS422 interface signals. Includes

DC/DC	converters	for	6-26	V
supply. A	all signals cor	nveyed	over	a
single DE	325 connector			

# Signal Generators, Test Modules

Module	Definition
<u>COM-1524</u>	Real-time digital channel simulator,
	featuring multipath fading, white
<u></u>	Gaussian noise, frequency trans-lation
	and long propagation
	delay.
<u>COM-1232</u>	Channel emulator with analog
	input/output. 64 MSamples/s. Up to 40
<u></u>	paths. Typical applications:
	Power line channel emulator
	Wireless channel emulator
<u>COM-1005</u>	Bit Error Rate measurement module.
<u>COM-8001</u>	Arbitrary waveform generator.
	256 MB or 1GB SDRAM,
<b>11</b> •••	Variable sampling rate and precision
	from 1 to 20 bits and up to 40
	Msamples/s.
<u>COM-8002</u>	High-speed data acquisition.
	256 MB DRAM, 1 Gbit/s throughput, 50
<b>11</b> •••	MHz sampling rate. Variable sample
	precision from 1 to 20 bits.

## Scrambling / Stream Formatting

Module	Definition
<u>COM-1014</u>	Standard Triple Data Encryption
	Algorithm (TDEA). Can be used for
	encryption or decryption.
	Maximum data rate 140 Mbit/s.
<u>COM-1016</u>	Bit Interleaver / Deinterleaver
	8 branches, 1024 depth cell.
	20 Mbps max.
<u>COM-8003</u>	Signal Diversity Combiner
<u>COM-8004</u>	Signal Diversity Splitter

# Connectivity

Module	Definition
<u>COM-9001</u>	Vertical extension connector
<u>COM-9002</u>	Horizontal extension connector
<u>COM-9003</u>	8:1 multiplexing connector
<u>COM-9004</u>	8:1 demultiplexing connector
COM-9105 <sup>1</sup>	98-pin to 98-pin connector
COM-9107 <sup>1</sup>	98-pin to 40-pin male connector
COM-9108 <sup>1</sup>	40-pin female to 98-pin connector
COM-9112 <sup>1</sup>	98-pin to 40-pin female connector
COM-9109 <sup>1</sup>	98-pin to two 40-pin female connectors
	(for use with COM-3505)
COM-9113	2 40-pin female to 98-pin male, for
	connecting two COM-30xx receivers to
	a FPGA module.

<sup>1</sup> Included with the relevant ComBlock modules. Please let us know your connectivity plans so that we can supply the appropriate module-to-module adapter(s).

Y03007R4	Card-edge adapter for ARM or Atmel micro programming through JTAG or DB-9 serial
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#### **User Interface**

Module	Definition
<u>COM-6001</u>	LEDs + dual 7-segment display

#### **FPGA / ARM Development Platforms**

Module	Definition
<u>COM-1800</u>	FPGA + ARM + GbE + DDR3
	SODIMM socket
<u> </u>	Development platform.
	Based on Xilinx Artix 7-100T
<u>COM-1700</u>	FPGA + ARM + GbE + USB2 +
	NAND + dual ADCs + dual DACs
<u> </u>	Development platform.
	Optimized for low-power.
	Based on Xilinx <b>Spartan-6</b>
	LX45L1
<u>COM-1500</u>	FPGA + ARM + DDR2 SODIMM
	socket + USB2+ NAND
<u> </u>	development platform. Powerful
	digital signal processing hardware
	comprising
	32-bit ARM processor @120 MHz
	+ Spartan-6 LA45 or LA150
	FPGA+ DDR2 SODIVIN socket for
	Large 64-bit wide memory module
	+ IGOR NAND hash memory + USP 2.0
COM-3011	103B 2.0
<u>COM-5011</u>	EPGA + APM
<u>п</u>	Software-defined ratio development
	platform comprising Xilinx
	Snartan-6 LX16 FPGA +
	32-bit ARM processor @120 MHz
	+ USB 2.0
<u>COM-1200</u>	FPGA development platform,
a fila	Analog front-end & USB 2.0. Based
III III 😽	on the Spartan-3 XC3S2000.
	Analog front-end includes dual
	high-speed 10-bit ADC, dual high-
	speed 12-bit DAC and multiple
	lower speed DACs and ADCs.
	FPGA configuration remains in
	non-volatile flash memory and is
	automatically reloaded at power up.
	Remote monitoring and control
	from the ComBlock control center.
<u>COM-1300</u>	FPGA development platform
- the	Spartan-3 XC3S400. & CardBus /
<u>III :::</u> 👐	PCMCIA Interface.

# Ease of Assembly

Complex communication systems can be created in three easy steps:

1. Connect +5V DC power to each **ComBlock** module.



2. Connect the monitoring and control link between one of the **ComBlock** modules within the assembly and the host computer. This connection is not mandatory at run-time as each **ComBlock** module retains its configuration.



Step 3: Plug in other **ComBlock** modules.



The assembly is now ready to run.

# **Conformal Assemblies**

**ComBlock** modules can be assembled in a variety of two-dimensional or three dimensional shapes to fit within standard size chassis or enclosures.













# Ease of Operation

**ComBlock** assemblies can be controlled and monitored over a single connection with a PC. Five connection types are supported by the ComBlock Control Center graphical user interface:

- Network: TCP/IP over a 10/100/1000 Mbps LAN (RJ-45 connector)
- USB 2.0 (high-speed)
- PCMCIA/CardBus
- 115.2 Kbaud/s asynchronous serial link (DB9 connector)
- Simulated connection with a module

The **ComBlock** Control Center software provides a simple user-friendly method for monitoring and control in four easy steps:

1. Connect with the **ComBlock** assembly.

<b>Com</b> File Ope	Block Control Center erations Functions Help
× ×	er 🎆 0 🖄 💵 🚇
Comm	unication Setup
0	Com Port
•	LAN/IP IP-address: 172, 16, 1, 128 IP Port Scan
O	USB comblock_usb_0 v
O	-CardBus
0	ComBlock Simulation
	Ok Cancel



3. Automatically detect the constituent modules of the assembly.

ComBlock Control Center	
File Operations Functions Help	
* 🔌 🖻 🐝 🕕 🐘 🕮 🚇	

COM5003 TCP-IP / USB GATEWAY

COM1019 Direct Sequence Spread-Spectrum Modulator

COM4004 70 MHz IF Modulator

- 4. Download firmware when new versions are available.
- 5. Monitor and control each module.

👎 COM4004 70 MHz IF Modulator Basic Settings 🛛 🛛 🔀	
IF Center Frequency: 69999999 Hz	
Gain Control: 128	
10 MHz External Frequency Reference	
Unmodulated Test Mode	
V Output On	
Apply Ok Advan Cancel	

The actual configuration resides in each **ComBlock** in non-volatile memory. It is automatically loaded at power up. Thus, remote configuration is not required once the **ComBlocks** are configured.

Custom monitoring & control applications can also be developed. The messages and protocols for communicating with **ComBlocks** are described in an <u>API document.</u>

#### ComScope

Most FPGA-based digital **ComBlock** modules are equipped with the **ComScope** data capture capability to help users visualize otherwise hidden digital signals.

These modules are identified with the **main** icon.

Internal digital signals, whether binary or digital representation of analog signals, can be stored in realtime into internal memory, then exported to a host computer for plotting, storage and further processing.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope Window Sample: showing GMSK demodulated phase (blue) and reconstructed unfiltered symbols (red).



### Multiple Personalities and Dynamic Reconfiguration

FPGA-based digital ComBlock modules are capable of **multiple personalities** and **dynamic reconfiguration**, whereby the FPGA can embody, on demand, one of multiple personalities stored in non-volatile flash memory.

Reconfiguration is ordered by a user over the selected communication link between user and ComBlock assembly: serial, LAN, PCMCIA, or USB, whichever is applicable.

Typical FPGA reconfiguration time is between 0.1 and 4 seconds, depending on the ComBlock, as listed in the specifications.

FPGA configuration data can be programmed into Flash memory one at a time, without affecting the other FPGA configurations already stored within the Flash memory.

Dynamic reconfiguration of the FPGA does not require any special VHDL programming. All ancillary tools are supplied with the ComBlock.

ComBlock hardware platforms supporting the dynamic reconfiguration are identified with the  $f^{a}$ 



User can select the default personality after reset/power-up.

#### Application Example: Spread-Spectrum L-band Modulator

Using five modules, one can easily assemble a variable data rate spread-spectrum L-band modulator.



The user forwards data to be transmitted over the LAN to a TCP-IP socket, or alternatively through a USB 2.0 connection between PC and COM-1509.

The data to be transmitted is encoded by a convolutional error correction code (COM-1509). The same module can also scramble the data and insert an HDLC-like frame structure prior to convolutional encoding.

The resulting data stream undergoes direct-sequence spread-spectrum (digital) modulation in the COM-1519 module.

The signal is then converted to analog baseband, low-pass filtered to reject spurious spectral lines and out-of-band signals. (COM-2001)

The last module (COM-4008) synthesizes a lowphase noise carrier. High frequency stability can be obtained by locking the carrier frequency to an external ultra-stable 10 MHz reference clock. The carrier frequency is user-selectable over the range 850 MHz to 1.6 GHz.

In order to keep the RF modulated signal at a fixed power level, an accurate RF power measurement is performed in the last stage. The user can control the transmitted power accurately over at least 20 dBs. Several test modes are included in this assembly, including transmitting a known 2047-bit pseudo-random sequence.

### Mechanical Interface Example

#### COM-15xx module



Maximum height 0.500"

# **Ordering Information**

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