

CREATING A FPGA CONFIGURATION FILE (.MCS) USING XILINX ISE 7.1

Following are the instructions to be followed to obtain a mcs file from a Xilinx ISE project (to program a [ComBlock FPGA development platform](#) for example). Please note that a newer document is available [here](#).

1.

The screenshot shows the Xilinx ISE 7.1 Project Navigator interface. The top window is titled 'Xilinx - Project Navigator - C:\DRIVERS\USB\WHDL\com1200del\com1200template_004b\com1200B.isc - [Design Summary]'. The 'Sources in Project' window on the left shows a project structure for 'com1200-behavioral' with various source files like 'com1200_1-behavioral.vhd', 'com1200_2-behavioral.vhd', 'com1200_3-behavioral.vhd', 'comscope-behavioral.vhd', 'capture_8_bit_words-behavioral.vhd', 'decimate-behavioral.vhd', and 'usb20'. The 'Processes for Source: "com1200-behavioral"' window on the right shows a list of processes, with 'Generate Programming File' selected and 'Generate PROM, ACE, or JTAG File' highlighted. The right-hand pane displays the 'Design Overview for com1200' and 'Performance Summary'.

Design Overview for com1200

Property	Value
Project Name:	c:\drivers\usb\whdl\com1200del\com1200template_004b\com1200B.isc
Target Device:	xc3s2000
Report Generated:	Wednesday 05/31/06 at 10:47
Printable Summary (View as HTML):	com1200_summary.html

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops:	1,025	40,960	2%	
Number of 4 input LUTs:	1,972	40,960	4%	
Logic Distribution:				
Number of occupied Slices:	1,339	20,480	6%	
Number of Slices containing only related logic:	1,339	1,339	100%	
Number of Slices containing unrelated logic:	0	1,339	0%	
Total Number 4 input LUTs:	2,183	40,960	5%	
Number used as logic:	1,972			
Number used as a route-thru:	211			
Number of bonded IOBs:	136	489	27%	
Number of Block RAMs:	6	40	15%	
Number of GCLKs:	7	8	87%	
Number of DCMs:	3	4	75%	

Performance Summary

Property	Value
Final Timing Score:	0
Number of Unrouted Signals:	All signals are completely routed.
Number of Failing Constraints:	0

Failing Constraints

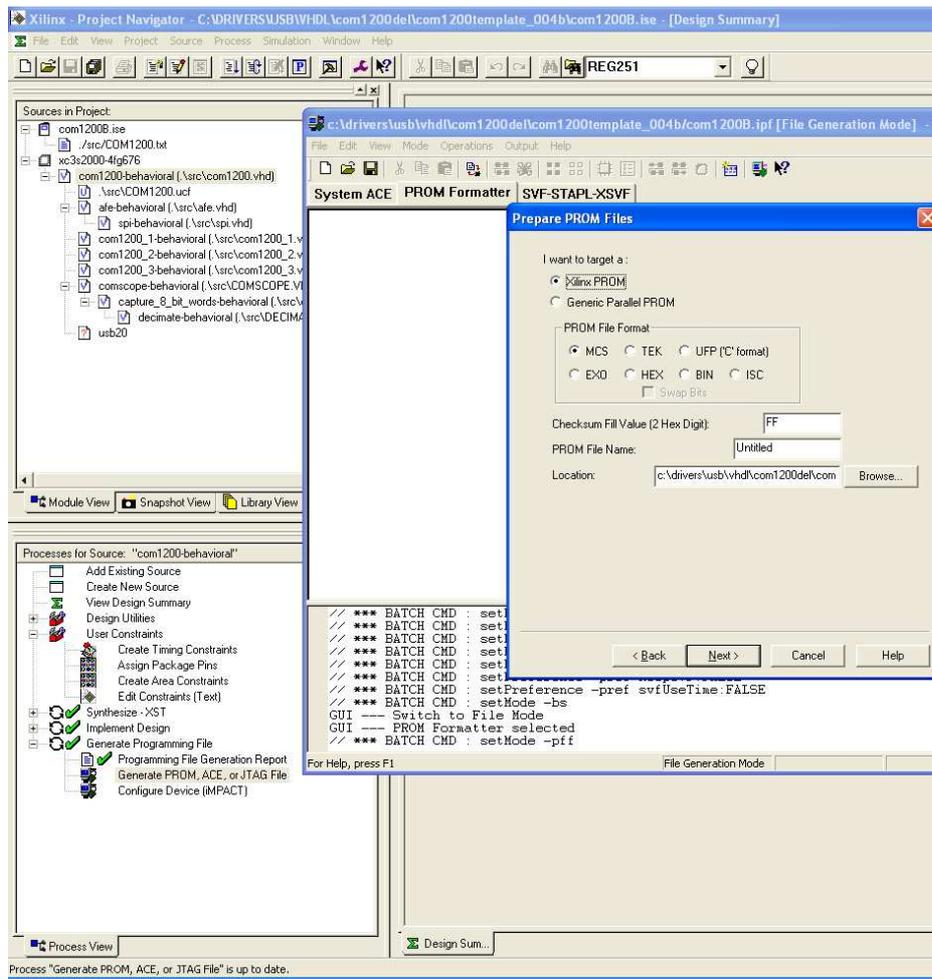
Constraint(s)	Requested	Actual	Logic Levels
All Constraints Met			

Detailed Reports

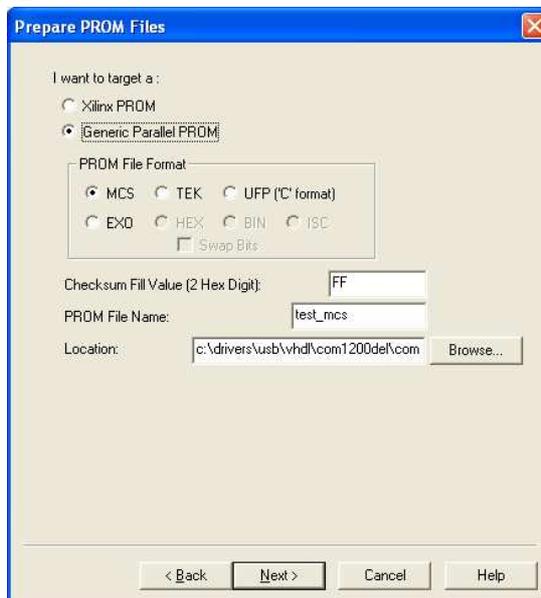
Report Name	Status	Last Date Modified
Synthesis Report	Current	Wednesday 05/31/06 at 10:45
Translation Report	Current	Wednesday 05/31/06 at 10:45
Map Report	Current	Wednesday 05/31/06 at 10:45
Pad Report	Current	Wednesday 05/31/06 at 10:46
Place and Route Report	Current	Wednesday 05/31/06 at 10:46
Post Place and Route Static Timing Report	Current	Wednesday 05/31/06 at 10:47
Bitgen Report	Current	Wednesday 05/31/06 at 10:47

From the Processes window of the Xilinx ISE run "Generate PROM, ACE or JTAG file" under the Generate Programming File process.

This will bring up iMPACT in a new window.

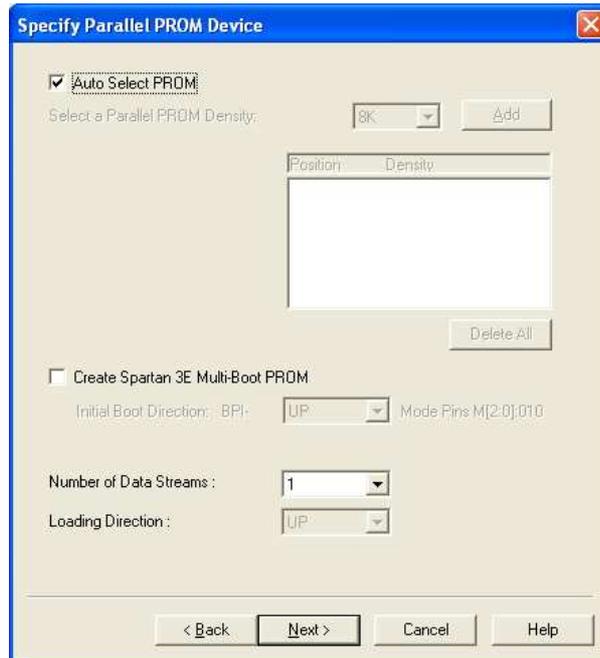


2. On the 1st screen:



Target: Generic Parallel PROM
 PROM file format: MCS
 Checksum: FF (unchanged)
 PROM file name: user defined
 Location: user defined
 Click next.

3.



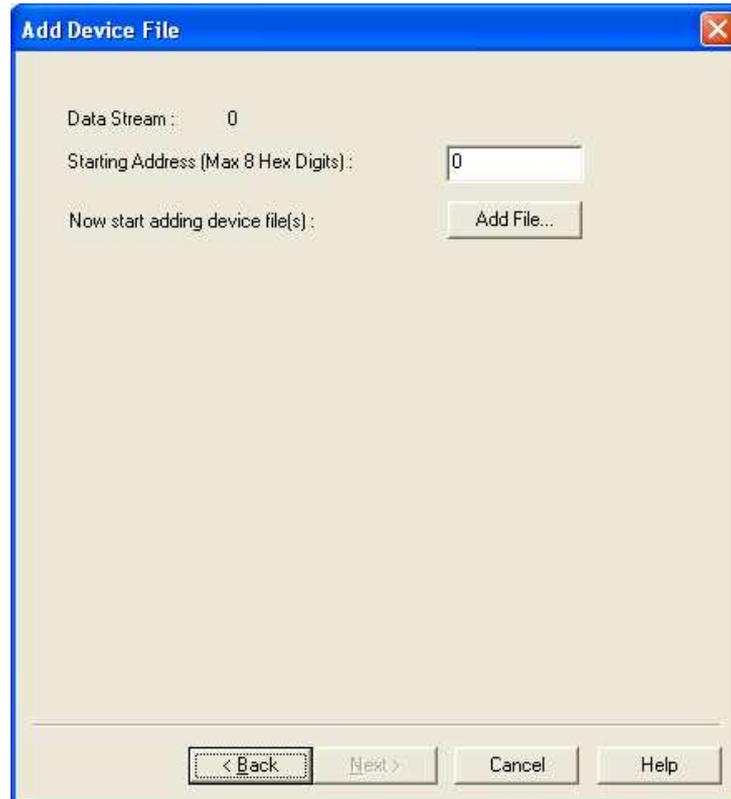
Select "Auto select PROM" and click next.

4.

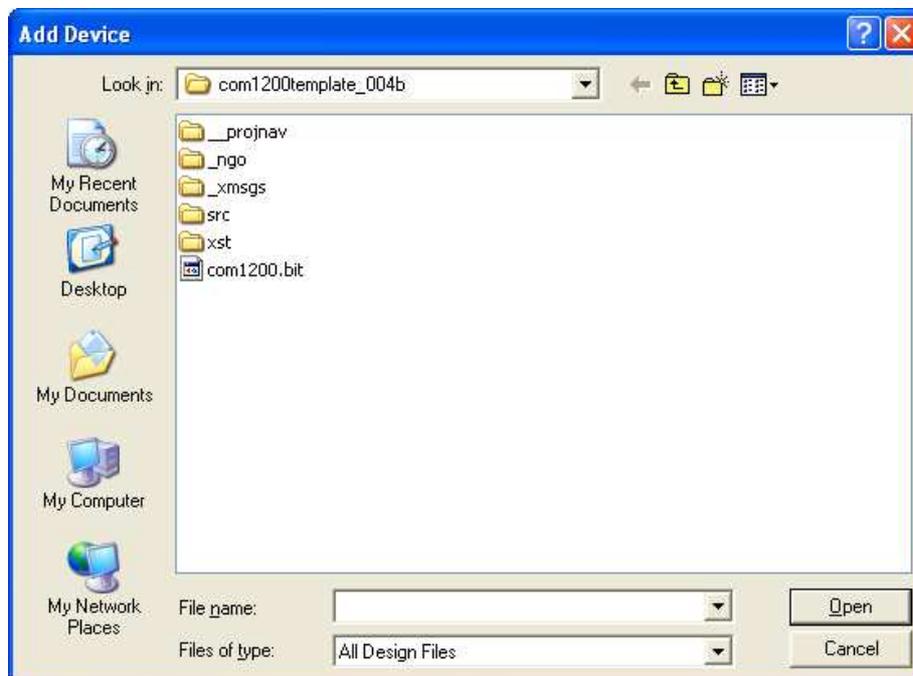


In the File Generation Summary screen, just click "Next".

5.



In the Add Device File Click on “Add File” to select the appropriate bit file.



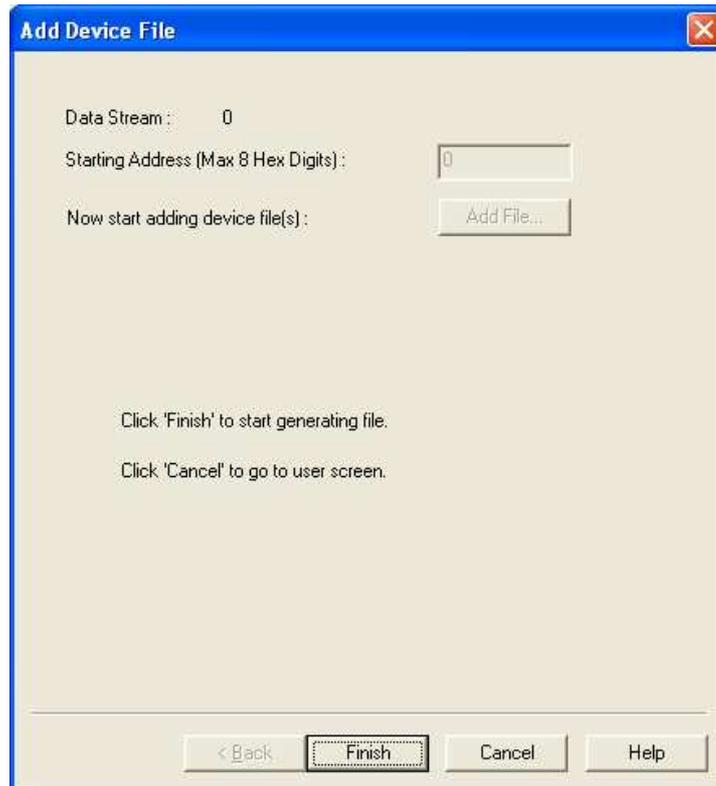
Select the bit file and click “Open”

6.



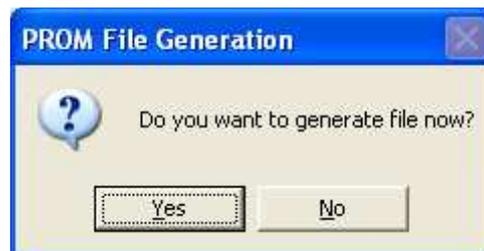
Answer “No” to the above question.

7.



Click on “Finish” in the next screen that appears.

8.



Select “Yes” in the above screen. At this point the impact window will become inactive. Once it is activated again, it shows the successful creation of a PROM file in .mcs format in the directory specified by the user.

