

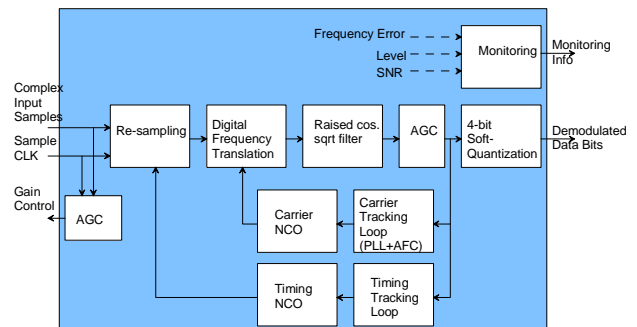
## COM-1001 BPSK/QPSK/OQPSK DEMODULATOR

### Key Features

- Digital BPSK/QPSK/OQPSK Demodulator.
- Variable data rates up to 20 Mbps (QPSK) / 10 Mbps (BPSK).
- Differential / non-differential decoding.
- Includes raised cosine square root filter with 20%, 25%, or 40% rolloff options.
- Demodulation losses less than 0.5 dB with respect to theory at  $E_b/N_o = 1$  dB.
- Demodulation threshold  $< -2$  dB  $E_b/N_o$ .
- Automatic frequency acquisition range up to  $\pm 50\%$  of the symbol rate.
- 4-bit soft-quantized demodulated bits.
- Extensive monitoring:
  - Carrier lock
  - Frequency error
  - AGC gain
  - SNR estimate
- Connectorized 3" x 3" module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom). Single 5V supply. Interfaces with 5V and 3.3V logic.

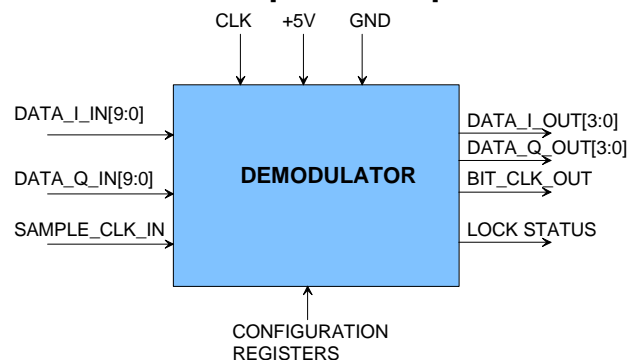


### Block Diagram



### Electrical Interface

#### Demodulator Inputs / Outputs



For the latest data sheet, please refer to the **ComBlock** web site: [www.comblock.com/download/com1001.pdf](http://www.comblock.com/download/com1001.pdf). These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to [www.comblock.com/product\\_list.htm](http://www.comblock.com/product_list.htm).

Input Module Interface	Definition
DATA_I_IN[9:0]	Modulated input signal, real axis. 10-bit precision. Format: 2's complement or unsigned. Unused LSBs are pulled low.
DATA_Q_IN[9:0]	Modulated input signal, imaginary axis. 10-bit precision. Same format as DATA_I_IN. Unused LSBs are pulled low.
SAMPLE_CLK_IN	Input signal sampling clock $f_s$ . One CLK-wide pulse. Read the input signal at the rising edge of CLK when SAMPLE_CLK_IN = '1'. Signal is pulled-up.
AGC_OUT	Output. When this demodulator is connected directly to an analog receiver, it generates a pulse-width modulated signal to control the analog gain prior to A/D conversion. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3V is the minimum gain.
CLK_IN	Input reference clock for synchronous I/O and processing. Yields internal CLK clock. Maximum frequency $f_{clk}$ is 40 MHz.

Two basic types of output connections are available for user selection:

- direct connection between demodulator and data destination.
- Shared data bus connecting multiple demodulators to a single data destination (for signal diversity combining)

Output Module Interface	Definition
Direct connection between two ComBlocks, REG7(3) = '0'	
DATA_I_OUT[3:0]	4-bit soft-quantized demodulated bits, real axis. Unsigned representation: 0000 for maximum amplitude '0', 1111 for maximum amplitude '1'. When the serial output mode is selected, I and Q samples are transmitted one after another on this interface. I is transmitted

	before Q.
DATA_Q_OUT[3:0]	4-bit soft-quantized demodulated bits, imaginary axis. Same format as DATA_I_OUT. When the serial output mode is selected, this interface is unused.
BIT_CLK_OUT	Demodulated bit clock. One CLK-wide pulse. Read the output signal at the rising edge of CLK when BIT_CLK_OUT = '1'.
CARRIER_LOCK	'1' when the demodulator is locked, '0' otherwise.
CLK_OUT	Output reference clock $f_{clk}$ . Typically 40 MHz.

Output Module Interface	Definition
Direct connection between two ComBlocks, REG7(3) = '0'	
DATA_I_OUT[3:0]	4-bit soft-quantized demodulated bits, real axis. Unsigned representation: 0000 for maximum amplitude '0', 1111 for maximum amplitude '1'. When the serial output mode is selected, I and Q samples are transmitted one after another on this interface. I is transmitted before Q.
DATA_Q_OUT[3:0]	4-bit soft-quantized demodulated bits, imaginary axis. Same format as DATA_I_OUT. When the serial output mode is selected, this interface is unused.
BIT_CLK_OUT	Demodulated bit clock. One CLK-wide pulse. Read the output signal at the rising edge of CLK when BIT_CLK_OUT = '1'.
RX_LOCK	'1' when the demodulator is locked, '0' otherwise. The lock status is based on the carrier lock.
CLK_OUT	output reference clock $f_{clk}$

<b>Serial Monitoring &amp; Control</b>	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
<b>Power Interface</b>	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency.

	The maximum power consumption at 40 MHz is 300mA.
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## Configuration

Complete assemblies can be monitored and controlled centrally over a single serial (included), LAN/TCP-IP, USB 2.0 or PCMCIA/CardBus connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

Most processing is done at the sampling rate /  
 $f_{\text{sample\_clk}} = 4 * \text{symbol rate}$ .

Parameters	Configuration
Nominal symbol rate x 4 (fsymbol rate x 4)	24-bit integer expressed as $f_{\text{symbol rate}} \times 4 * 2^{23} / f_s$ , where $f_s$ is the input sampling rate as determined by the SAMPLE_CLK_IN input signal. Alternatively, the user can select to ignore the external sampling clock and use the processing clock $f_{\text{clk}}$ instead (see REG7 bit 6 control). In the latter case, $f_s = f_{\text{clk}}$ .  Use of the COM-1001 at symbol rates below 100 Ksymbols/s is possible but can be complex because of effects such as of phase noise, frequency acquisition, oscillator stability, microphonics, etc.  REG0 = bit 7-0 REG1 = bit 15 – 8 REG2 = bit 23 – 16
Nominal carrier center frequency ( $f_c$ )	24-bit signed integer (2's complement) expressed as $f_c * 2^{24} / f_{\text{symbol rate}} \times 4$ . This field is typically used for fine frequency tuning (coarse frequency tuning being implemented at the RF front-end). Maximum range to avoid aliasing is +/- 1.5*fsymbol rate. REG3 = bit 7 – 0 REG4 = bit 15 – 8 REG5 = bit 23 - 16
Input sample format	0 = 2's complement 1 = unsigned REG6 bit 1
Carrier frequency tracking loop gain	0 = nominal 1 = 2x loop gain 2 = 4x loop gain 3 = 8x loop gain

	The loop gain can be changed dynamically to ease the transition between acquisition and tracking. A higher loop gain can be used to increase acquisition range or to minimize cycle slips at low data rate. A lower loop gain minimizes demodulation losses. REG6 bits 3-2
Extended frequency acquisition enable	Enable the extended frequency acquisition over +/- 50% of the symbol rate. When disabled, the receiver only means of carrier acquisition is the carrier frequency tracking loop which is inherently limited to approximately 1% of the symbol rate. A larger frequency acquisition can be achieved than with the Costas carrier tracking loop or the AFC, but the acquisition time is slower. The extended frequency acquisition mode should only be used during acquisition as it interferes with the AFC and Costas Loop operation. 0 = disabled. 1 = enabled. REG6 bit 4
Spectrum inversion	Invert Q bit. 0 = off 1 = on REG6 bit 5
Differential decoding	0 = off 1 = on REG6 bit 6
Output sample format	00 = I/Q parallel 01 = I/Q serial, I before Q (never use with BPSK as there is no information data on the Q channel) REG7 bits 1-0
AFC enable	The automatic frequency control circuit extends the frequency acquisition over +/- 10% of the symbol rate. When disabled, the receiver only means of carrier acquisition is the carrier frequency tracking loop which is inherently limited to approximately 1% of the symbol rate. The AFC should only be used during acquisition as it interferes with the Costas Loop operation. 0 = AFC disabled. Carrier tracking loop only 1 = AFC enabled. REG7 bit 2
Point-to-point vs shared bus output	Controls whether the output connection is point-to-point or multipoint-to-point over a shared data bus (via a COM-9003 multiplexing connector for example). The J3 output connector pinout is affected by this control bit. 0 = direct connection. Point to point.

	1 = shared data bus. REG7 bit 3
Modulation	00 = BPSK 01 = QPSK 10 = OQPSK (I channel is delayed by ½ a symbol w.r.t. the Q channel) REG7 bit 5 – 4
Force sampling rate $f_s = f_{clk}$	Ignore external SAMPLE_CLK_IN sampling clock and force internal resampling $f_s$ to $f_{clk}$ . 0 = $f_s$ sampling clock based on external sampling signal SAMPLE_CLK_IN. 1 = ignore external sampling clock. $f_s = f_{clk}$ (typically 40 MHz) REG7 bit 6
Force (Re-) acquisition	A one-time write of '1' forces the carrier loops (carrier PLL, AFC) back into acquisition mode. This can be used to get out of any potential false lock condition. There is no need to clear this bit. REG7 bit 7
Bus address	Unique 4-bit address identifying this module on the output bus (if the output bus is enabled in REG7 bit 3). Ignore otherwise. This module acts as bus slave: it performs the read transaction requested by the bus master if and only if the bus address matches its own address defined here. This address must be unique among modules connected to the same bus in order to avoid conflicts. REG8 bits 3-0

## Monitoring

Monitoring registers are read-only.

Parameters	Monitoring
Carrier frequency offset	Residual frequency offset with respect to the nominal carrier frequency. 24-bit signed integer (2's complement) expressed as $f_{c\delta} * 2^{24} / f_{symbol\ rate} * 4$ SREG8 = bit 7 – 0 SREG9 = bit 15 – 8 SREG10 = bit 23 – 16
AGC gain	Digital AGC gain settings 8 bit unsigned SREG11 bit 7-0.
NSR	Noise to signal ratio. Variance of the 4-bit soft-quantized demodulated samples at the optimum sampling instant averaged over 4096 symbols. Non-linear scale. Approximates 1/SNR. A few reference points: NSR = 24 -> SNR = 8.6 dB NSR = 34 -> SNR = 5.6 dB

	8 bit unsigned. SREG12 bits 7 – 0
Lock status	SREG13 bit 0 0 = unlocked 1 = locked
I sample	I sample after digital AGC. Format: 8-bit 2's complement. This monitoring point can be used in conjunction with the Q sample to plot a scatter diagram. SREG14 bits 7-0
Q sample	I sample after digital AGC. Format: 8-bit 2's complement. This monitoring point can be used in conjunction with the Q sample to plot a scatter diagram. SREG15 bits 7-0
Option o / Version v	Returns '1001ov' when prompted for option o and version v numbers.

### Default configuration at manufacturing:

REG0 = 0x00  
REG1 = 0x00  
REG2 = 0x40  
REG3 = 0x00  
REG4 = 0x00  
REG5 = 0x00  
REG6 = 0x82  
REG7 = 0x00

### Configuration example:

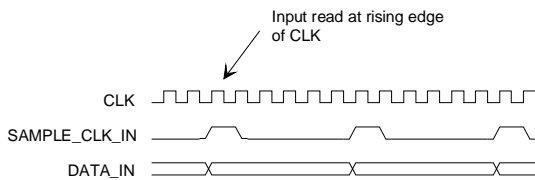
REG0 = 0x52  
REG1 = 0xB8  
REG2 = 0x7E  
REG3 = 0x00  
REG4 = 0x00  
REG5 = 0x00  
REG6 = 0x80  
REG7 = 0x11  
configures the demodulator as follows:  
symbol rate x 4 = 39.6 MHz  
offset carrier = 0 Hz  
2's complement input format  
nominal loop gain  
no spectrum inversion  
no differential decoding  
serial output  
QPSK

## Timing

The I/O signals are synchronous with the rising edge of the reference clock CLK (i.e. all signals transitions always occur after the rising edge of the reference clock CLK). The maximum CLK frequency is 40 MHz.

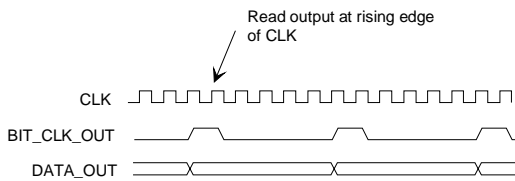
The maximum demodulated data rate is equal to half of the reference clock frequency.

## Input



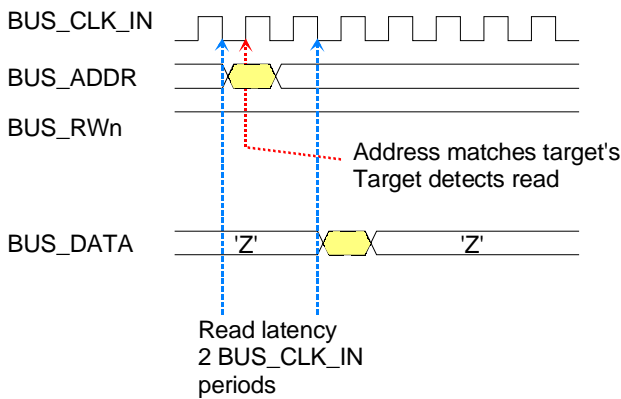
## Output

(Point to point connection, REG7 bit3 = '0')



## Output

(Shared bus, REG7 bit3 = '1')



## Test Points

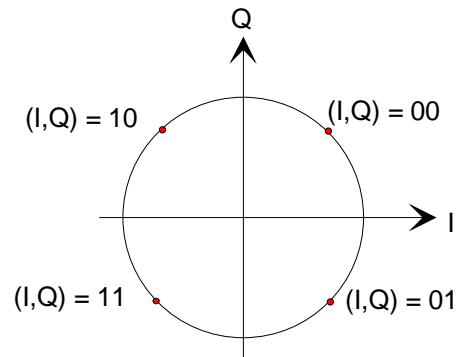
Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
TP1	Carrier lock. Lock status is based on the rms phase error. This test point can be ambiguous as a 'no input signal' condition may yield be confused as carrier lock. Use in conjunction with bit transition (TP7) to remove any ambiguity.
TP2	Frequency acquisition in progress
TP3	Recovered carrier
TP4	Recovered timing (2*symbol rate)
TP5	Demodulated bit, I-channel DATA_I_OUT(3)
TP6	Demodulated bit, Q-channel DATA_Q_OUT(3)
TP7	Bit transitions. '1' if at least symbol transition within any 1023 symbol window.
TP10	Input samples saturation detector. Helpful in identifying possible saturation at the external A/D converters.

## Implementation

### Phase Map (QPSK)

The nominal phase map follows Gray encoding as illustrated below:



As with all QPSK demodulators, there is a phase ambiguity of  $n \cdot 90$  deg in the demodulated output. The phase ambiguity is not resolved in this module. It is typically resolved either through the use of a unique word periodically inserted in the data stream (for example when using Turbo code or Reed-Solomon block code) or through bit error rate detection in Viterbi decoder.

## Differential Decoding (QPSK)

In low data rate applications where the phase noise can affect the bit error rate performances, it can be advisable to use differential QPSK. The phase difference between two successive symbols conveys the information symbol.

0 deg = "00"  
 90 deg = "01"  
 180 deg = "10"  
 270 deg = "11".

This implementation is not strictly that of a DPSK demodulator in the sense that the receiver still tracks the carrier phase and frequency using a Costas loop.

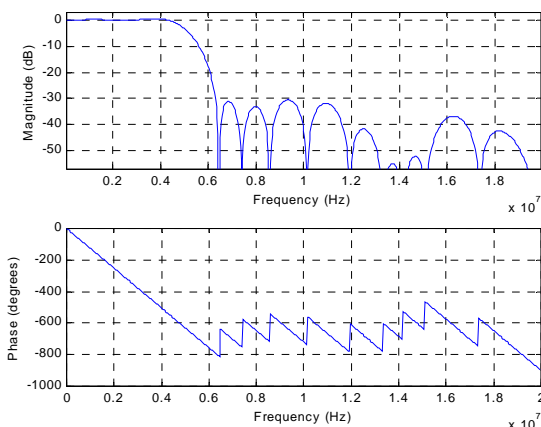
## Filter Response

This module is configured at installation with a 20% rolloff filter. The filter rolloff can be selected among 20%, 25% and 40%. Changing the rolloff selection requires re-loading the firmware using the ComBlock control center.

The three firmware versions can be downloaded from [www.comblock.com/download](http://www.comblock.com/download).

COM-1001-A QPSK demodulator 20% rolloff  
 COM-1001-B QPSK demodulator 25% rolloff  
 COM-1001-E QPSK demodulator 40% rolloff

## Filter Response (20% rolloff)



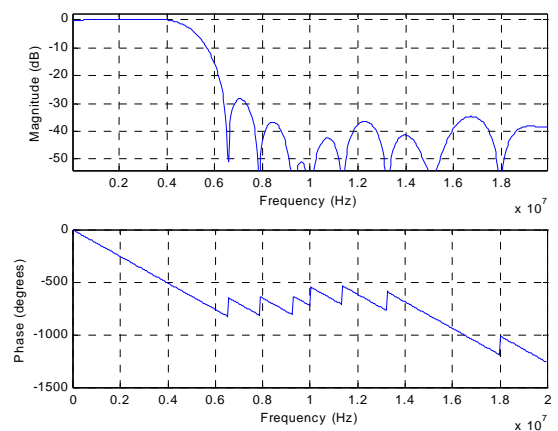
*(filter response normalized for 4\*symbol rate = 40 MHz)*

The raised cosine square root filter with 20% rolloff is a 29-tap FIR filter with the following impulse response:

Coeff(0) = -8/1024  
 Coeff(1) = -16/1024  
 Coeff(2) = -8/1024

Coeff(3) = 8/1024  
 Coeff(4) = 24/1024  
 Coeff(5) = 24/1024  
 Coeff(6) = 12/1024  
 Coeff(7) = -16/1024  
 Coeff(8) = -48/1024  
 Coeff(9) = -52/1024  
 Coeff(10) = -16/1024  
 Coeff(11) = 64/1024  
 Coeff(12) = 160/1024  
 Coeff(13) = 240/1024  
 Coeff(14) = 272/1024  
 Coeff(j=15:28) = coeff(28-j);

## Filter Response (25% rolloff)

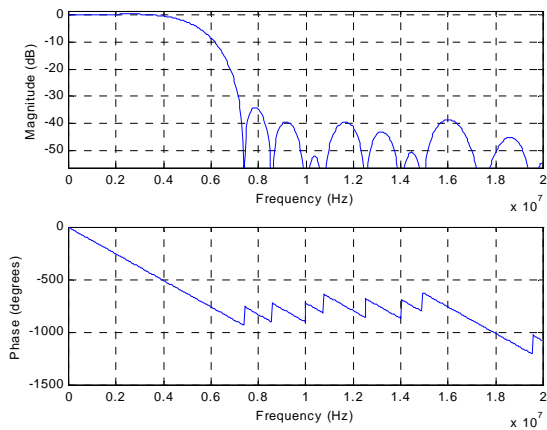


*(filter response normalized for 4\*symbol rate = 40 MHz)*

The raised cosine square root filter with 25% rolloff is a 29-tap FIR filter with the following impulse response:

Coeff(0) = -4/1024  
 Coeff(1) = -12/1024  
 Coeff(2) = -8/1024  
 Coeff(3) = 2/1024  
 Coeff(4) = 16/1024  
 Coeff(5) = 24/1024  
 Coeff(6) = 12/1024  
 Coeff(7) = -16/1024  
 Coeff(8) = -48/1024  
 Coeff(9) = -48/1024  
 Coeff(10) = -16/1024  
 Coeff(11) = 64/1024  
 Coeff(12) = 160/1024  
 Coeff(13) = 240/1024  
 Coeff(14) = 272/1024  
 Coeff(j=15:28) = coeff(28-j);

## Filter Response (40% rolloff)



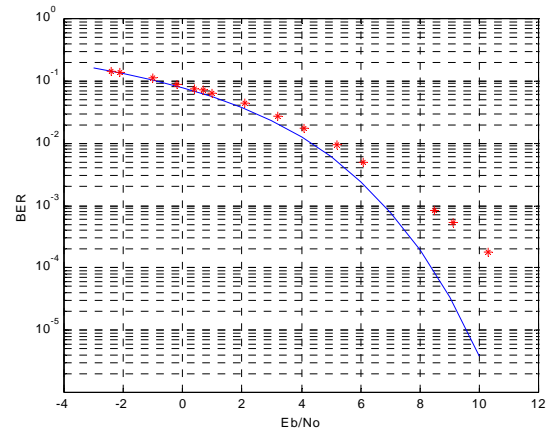
(filter response normalized for 4\*symbol rate = 40 MHz)

The raised cosine square root filter with 40% rolloff is a 29-tap FIR filter with the following impulse response:

- Coeff(0) = 4/1024
- Coeff(1) = 1/1024
- Coeff(2) = -4/1024
- Coeff(3) = -4/1024
- Coeff(4) = 2/1024
- Coeff(5) = 12/1024
- Coeff(6) = 14/1024
- Coeff(7) = -2/1024
- Coeff(8) = -30/1024
- Coeff(9) = -48/1024
- Coeff(10) = -24/1024
- Coeff(11) = 48/1024
- Coeff(12) = 152/1024
- Coeff(13) = 248/1024
- Coeff(14) = 284/1024
- Coeff(j=15:28) = coeff(28-j);

## Bit Error Rate Performances

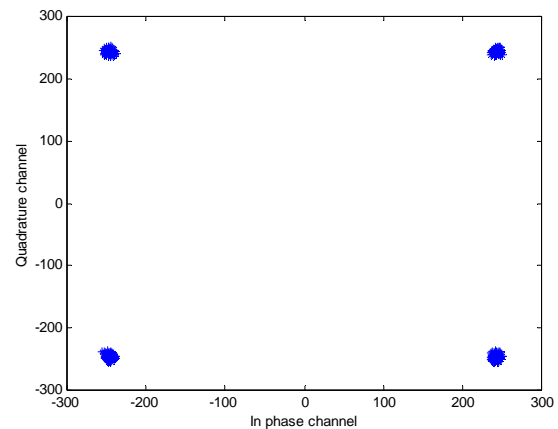
The demodulator bit-error-rate performances are within 0.5 dB from the theoretical performances  $\frac{1}{2} * \text{erfc}(E_b/N_o)$  of QPSK demodulators at  $E_b/N_o$ , of 1 dB Actual measurements taken by using the COM-1001-E digital demodulator, the COM-1002-E digital modulator and the COM-1023 noise generator are shown below:



### BER performance

The demodulator threshold is better than -2 dB  $E_b/N_o$ , during digital back to back tests.

The demodulated QPSK bits (also captured with back to back digital modulator-demodulator) . It shows that the intersymbol interferences are negligible.



## Frequency Acquisition & Tracking

The demodulator comprises three frequency acquisition and tracking processes:

- a phase locked loop (PLL), also known as 'Costas Loop'.
- an Automatic Frequency Control (AFC) loop.
- an extended frequency acquisition circuit.

The AFC is to quickly detect and compensate for carrier *frequency* offsets, generally around the time of the initial acquisition. The PLL is to detect and compensate for carrier *phase* errors.

The PLL is a second order loop. It can track the center frequency over a range of  $\pm 1.5 \times$  symbol rate. The digital implementation of the Costas PLL has a small frequency acquisition range of about  $\pm 1\%$  of the modulation symbol rate.

The main purpose of the AFC is to increase the frequency acquisition window to about  $\pm 10\%$  of the modulation symbol rate (typical). Once the AFC ‘zooms in’, the AFC must be disabled (see REG7 bit2).

The extended frequency acquisition circuit extends the frequency acquisition range to about  $\pm 50\%$  of the modulation symbol rate (typical). The algorithm relies on the spectrum symmetry: it is thus important to ensure bit randomness at the transmitter for a symmetrical spectrum. This loop is significantly slower than the AFC. It can be enabled or disabled by means of control register REG6 bit 4.

If the unknown received carrier frequency uncertainty is larger, the user must program some search algorithm using the nominal center frequency control registers (REG3/4/5).

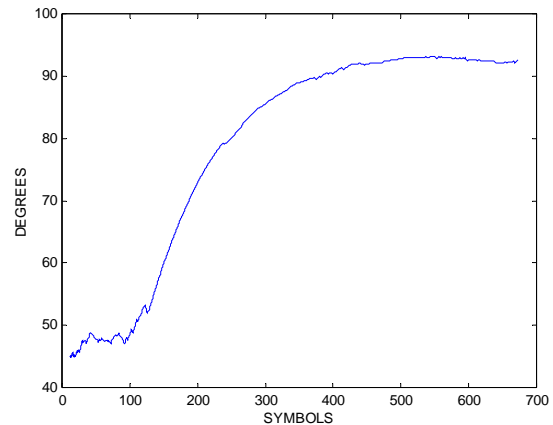
For high data rates ( $> 100$  Kbps), carrier phase noise is generally negligible. For lower data rates, it may be necessary to adjust the carrier tracking loop gain as a tradeoff between carrier phase noise (originating at the modulator, up-converter, down-converter, etc) and thermal noise. To this effect, the user is given control of the loop gain over a range of x1, x2, x4 and x8.

The higher loop gain can also be used temporarily during acquisition to increase the frequency acquisition window from approximately 1% to 3% of the symbol rate. However, use of the AFC is preferred because of the faster acquisition time and larger acquisition range.

In some conditions, such as no input signal, the AFC and PLL loops can drift out and inhibit (re-)acquisition. It is possible for the user to reset the accumulators within the AFC and PLL loops by writing a ‘1’ in REG7 bit7.

The Costas loop nominal settings are selected to keep the BER degradations small (within 0.5 dB from theory) at the threshold SNR. The resulting frequency acquisition range is about 1% of the symbol rate. The acquisition time is typically 500 symbols as shown below.

The carrier tracking loop’s response to a (worst case) 45 degrees phase error step at the input is shown below.



*NCO phase response to a 45 deg. input phase error step. Nominal loop gain. Noiseless.*

## **Input Interpolation**

This module provides fine selection of symbol rates, as long as the input sampling rate is between x4 and x8 the symbol rate. For higher ratios between input sampling rate / symbol rate, the COM-1008 variable decimation filter is recommended to prevent aliasing.

## **AGC**

The COM-1001 comprises two AGC circuits, one at the front-end operating jointly with a front-end analog receiver, the other fully digital after channel filtering.

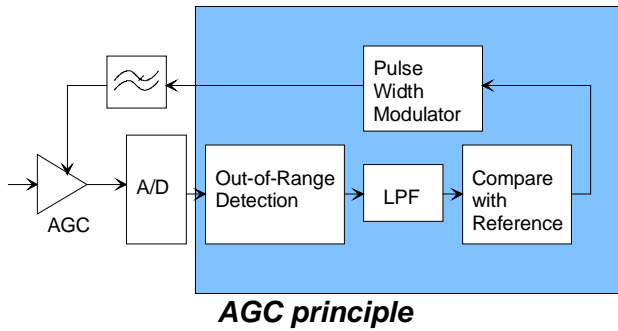
### **Front-End AGC**

The purpose of this front-end AGC is to prevent saturation at the external A/D converter(s) while making full use of the 10-bit A/D converter dynamic range. The principle of operations is outlined below:

- (a) out-of-range at the A/D converter is detected. An out-of-range condition occurs if the quantized A/D samples are equal to either “1111111111” or “0000000000”.
- (b) The AGC will adjust the analog circuitry gain so that out-of-range conditions do not occur more than 1 in 64 samples in the average.



(c) The resulting gain control signal is a pulse-width modulated (PWM) signal with 10-bit precision.



The analog circuit shall filter this 3.3V low-voltage TTL PWM signal with a low-pass filter prior to controlling the analog gain. The PWM is randomized and its spectral distribution shifted to the higher frequencies so as facilitate the analog low-pass filter design.

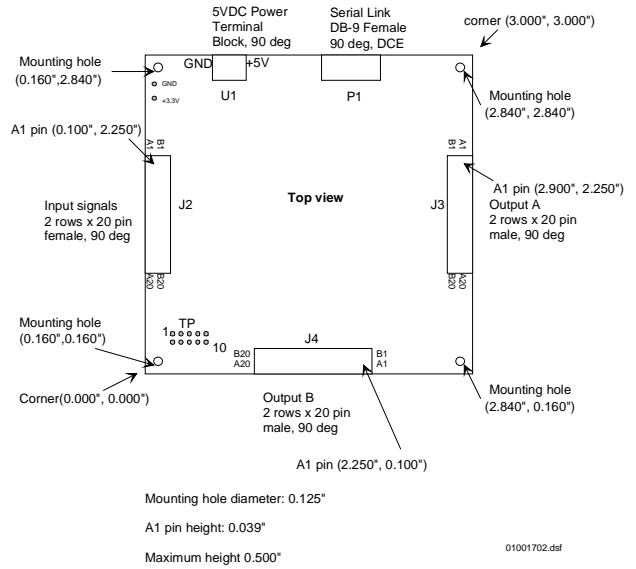
The AGC loop bandwidth is typically 1 Hz when used in conjunction with COM-30xx receivers and a 40 MHz input clock. The loop response time is assymetrical: it responds faster to a saturation condition than to a 'low signal' condition.

The gain control signal will increase if too many out-of-range conditions occur.

## Digital AGC

A digital AGC provides 18 dB (3 bits) of dynamic range for signals following the raised cosine filter.

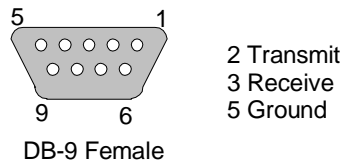
## Mechanical Interface



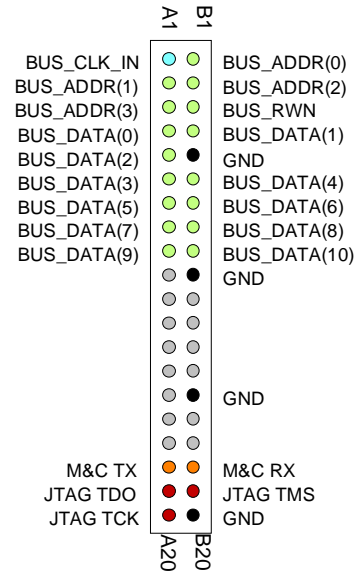
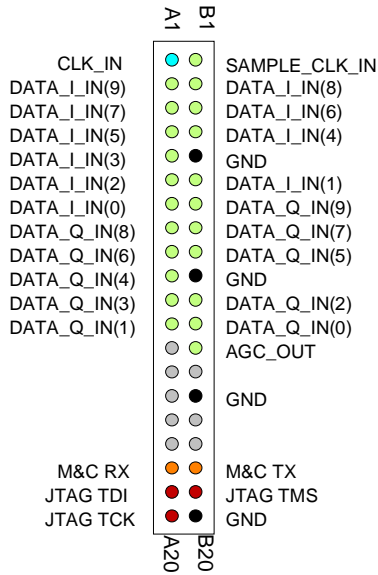
## Pinout

### Serial Link P1

The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.

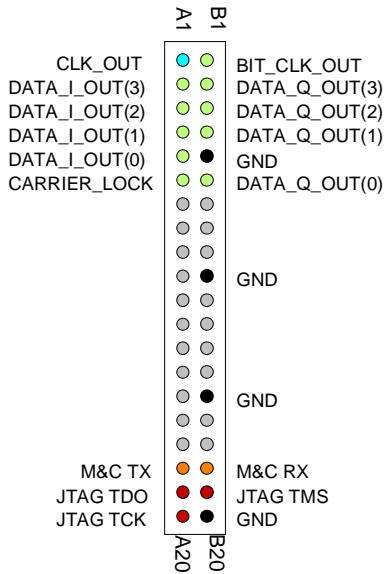


## Input Connector J2



This connector is used for multipoint-to-point connection over a shared data bus when control register REG7(3) = '1'. COM-1001 is a bus slave. It always listens to BUS\_CLK\_IN, BUS\_ADDR, BUS\_RWN. The bus interface is only via the J3 connector, the J4 connector being disabled.

## Output Connectors J3, J4



This connector is used for point-to-point (i.e. direct) connection between two ComBlocks when control register REG7(3) = '0'.

## I/O Compatibility List

(not an exhaustive list)

Input	Output
<a href="#">COM-1002</a> BPSK/QPSK/OQPSK modulator (digital back to back)	<a href="#">COM-1005</a> Bit Error Rate Measurement
<a href="#">COM-300x</a> RF receivers	<a href="#">COM-7001</a> Turbo Code decoder
<a href="#">COM-1008</a> Variable decimation	<a href="#">COM-1009</a> Convolutional decoder K=5, 7
<a href="#">COM-1023</a> BER generator, AWGN generator	<a href="#">COM-8003</a> Signal diversity combiner
<a href="#">COM-1024</a> Multi-path generator	<a href="#">COM-5003</a> TCP-IP / USB Gateway

## Configuration Management

This specification is to be used in conjunction with VHDL software revision 28.

## ComBlock Ordering Information

COM-1001     Digital BPSK/QPSK/OQPSK  
demodulator

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