COM-1002
BPSK/QPSK/OQPSK MODULATOR

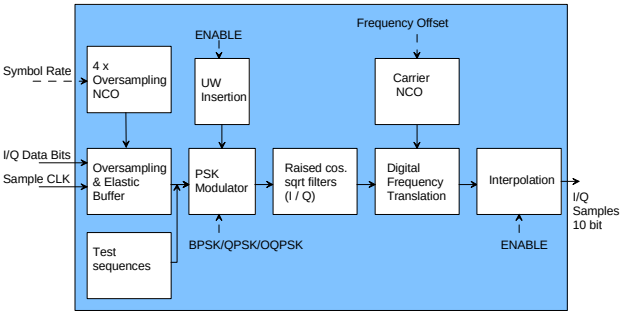
Key Features

- BPSK/QPSK/OQPSK modulator.
- Programmable data rates up to 20 Mbps (QPSK) and 10 Mbps (BPSK) by steps of at most 3bps.
- Includes raised cosine square root filter with 20%, 25%, or 40% rolloff options.
- Differential and non-differential encoding.
- Synchronization sequence (unique word) insertion to facilitate demodulator acquisition.
- Internal generation of pseudo-random bit stream and unmodulated carrier for test purposes.
- Built-in channel impairments generation:
  - frequency offset (Doppler)
- On-board or external clock selection.
- Single 5V supply
- Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom). Interfaces with 5V and 3.3V logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1002.pdf.
These specifications are subject to change without notice.

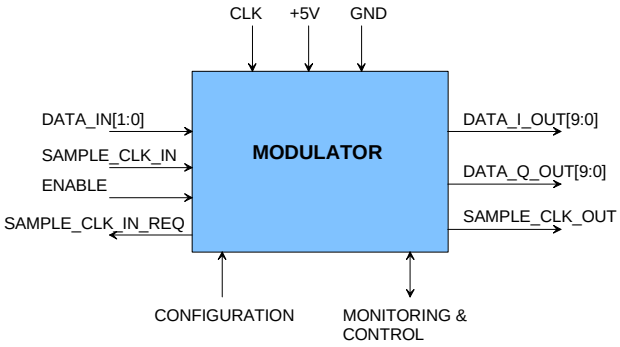
For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

Block Diagram



Electrical Interface

Modulator Inputs / Outputs



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Two basic types of input connections are available for user selection:

- direct connection between data source and modulator.
- single data source to multiple modulators over a shared bus.

Input Module Interface Direct connection between two ComBlocks, REG9(4) = '0'	**Definition**
DATA_IN[1:0]	Input data stream. In 1-bit serial mode, use DATA_IN[0] only. In 2-bit parallel mode, DATA_IN[0] is the I data bit DATA_IN[1] is the Q data bit The Q data bit is ignored in BPSK mode.
SAMPLE_CLK_IN	Input symbol clock. One CLK-wide pulse. Read the input signals at the rising edge of CLK when SAMPLE_CLK_IN = '1'.
ENABLE	Modulator enable input. Internally pulled high. Qualifies the SAMPLE_CLK_IN signal. Used for burst-mode transmission. In continuous mode, keep at '1'.
SAMPLE_CLK_IN_REQ	One CLK-wide pulse. Requests a sample from the module upstream. For flow-control purposes.
CLK_IN	Input reference clock for synchronous I/O and processing. Yields internal CLK clock. Typically $\mathbf{f_{clk}}$ = 40 MHz.

Input Module Interface Bus connection, REG9(4) = '1'	**Definition**
BUS_CLK_IN	40 MHz input reference clock for use on the synchronous bus.
BUS_ADDR[3:0]	Bus address. Input (since this module is a bus slave). Designates which slave module is targeted for this read or write transaction.
	All 1's indicates that the write data is to be broadcasted to all receiving slave modules. Read at the rising edge of BUS_CLK_IN
BUS_RWN	Read/Write#. Input (since this module is a bus slave). Indicates whether a read (1) or write (0) transaction is conducted. Read at the rising edge of BUS_CLK_IN. Read and Write refer to the bus master's perspective.
BUS_DATA[15:0]	Bi-directional data bus. Input when BUS_RWN='0'. Output when BUS_RWN='1'. Read data latency is 2 clock periods after the read command. Functional definition during write: • bit 0 SAMPLE_CLK_IN. '1' when DATA_IN is available • bit 1 DATA_IN data stream to modulator. • bits(15:2) undefined Functional definition during read: • bit 0 SAMPLE_CLK_IN_REQ requests data from the source. Used for flow control. • bits(15:1) undefined

Two basic types of output connections are available for user selection:

- connection to dual 10-bit DACs, parallel I and Q samples, output sampling clock.
- connection to dual 14-bit DACs, multiplexed I and Q samples, input sampling clock.

Output Module Interface (Output data pushed out) Parallel 10-bit I & Q samples. REG9(2) ='0'	**Definition**
DATA_I_OUT[9:0]	Modulated output signal, real axis. 10-bit precision. Format: 2's complement or unsigned, selected by configuration bit 1.
DATA_Q_OUT[9:0]	Modulated output signal, imaginary axis. 10-bit

	precision. Same format as DATA_I_OUT.
SAMPLE_CLK_OUT	Output signal sampling clock. Read the output signal at the rising edge of CLK when SAMPLE_CLK_OUT = '1'. Sampling rate is either 4 x symbol rate or fclk (interpolation off/on configuration bit 7). SAMPLE_CLK_OUT can stay high when output samples are transmitted in successive CLK periods.
DAC_CLK_OUT	Output sampling clock for Digital to Analog Converters. DAC reads the output sample at the rising edge.
CLK_OUT	Output reference clock. Same as CLK internal processing clock. Typically 40 MHz.

Output Module Interface (Output data pulled) REG9(2) ='1'	**Definition**
SAMPLE_CLK_REQ_IN	Input. 100 MHz clock requesting output samples.
DATA_OUT[13:0]	Output. Quadrature baseband samples, 14-bit precision, 2's complement format. Bit 13 is the most significant bit. The in-phase (I) and quadrature (Q) samples alternate. Output samples are synchronous with the falling edge of SAMPLE_CLK_REQ_IN.
TX_ENABLE	Output. Transmit enable. Active high. The first sample after TX_ENABLE becomes active is an in-phase (I) sample.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 650mA.

Configuration

Complete ComBlock assemblies can monitored and controlled centrally over a single serial, LAN/TCP-IP, USB 2.0, or PCMCIA/CardBus connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

Most processing is done at the sampling rate / f_{sample_clk} = 4 * symbol rate.

In the definition below, a few control register bits may be undefined to maintain backward compatibility with previous versions. They can be ignored by the user when using the latest firmware release.

Parameters	**Configuration**
Symbol rate x 4 (f_{sample_clk})	24-bit unsigned integer expressed as fsymbol rate x 4 * 2^{24} / f_{clk}. f_{clk} is typically 40 MHz. REG0 = bit 7-0 (LSB) REG1 = bit 15 – 8 REG2 = bit 23 – 16 (MSB)
Offset carrier frequency	24-bit signed integer (2's complement representation) expressed as fc * 2^{24} / f_{sample_clk}. f_{sample_clk} is defined by REG0,1,2. REG3 = bit 7 – 0 REG4 = bit 15 – 8 REG5 = bit 23 - 16
Signal gain	Signal level. 8-bit unsigned integer. Maximum level 255, Minimum level 0. When the maximal level (255) is selected, the peak-to-peak dynamic range is +/- 371 out of a +/-512 (10-bit) range and the standard deviation is 249. REG6 = bit 7-0
Reserved	0x00 REG7
Internal / External clock selection	Clock is 'internal' when this module is the first in the transmission chain and when using the internally generated test sequences (see Test mode below). In all other cases, clock selection is 'external'. 0 = internal clock 1 = external clock REG8 bit 0
Output sample format	0 = 2's complement 1 = unsigned See also REG9 bit 2 for additional settings. REG8 bit 1

Modulation	00 = BPSK 01 = QPSK 10 = OQPSK (Q channel is delayed by ½ a symbol w.r.t. the I channel) REG8 bit 3 – 2
Test mode	00 = disabled 01 = internal generation of 2047-bit periodic pseudo-random bit sequence as modulator input. (overrides external input bit stream). 10 = unmodulated carrier. (overrides external input bit stream) REG8 bit 5 – 4
Spectrum inversion	Invert Q bit. 0 = off 1 = on REG8 bit 6
Interpolation	Interpolation to maximum clock rate. 0 = off 1 = on REG8 bit 7
Differential encoding	0 = off 1 = on REG9 bit 0
Input format	0 = 1-bit serial 1 = 2-bit parallel REG9 bit 1
Output data flow	0 = output data is pushed to the next module (for example to COM-2001, or COM-1001) 1 = output data is pulled by next module (for example by the COM-4004) REG9 bit 2
Tx unique word	0 = off 1 = on REG9 bit 3
Input bus enabled	Controls whether the input connection is point-to-point or point-to-multipoint over a data bus (via a COM-9004 demultiplexing connector for example). The J2 input connector pinout is affected by this control bit. 0 = direct connection. Point to point. 1 = input data bus enabled. REG9 bit 4
Bus address	Unique 4-bit address identifying this module on the input bus (if the input bus is enabled in REG9 bit 4). Ignore otherwise. This module acts as bus slave: it performs the read/write transaction requested by the bus master if and only if the bus address matches its own address defined here. This address must be unique among modules connected to the same bus in order to avoid conflicts. REG10 bits 3-0

Writing to REG9 resets the output interface. When interfacing with the COM-4004 70 MHz modulator, any configuration change in the COM-4004 should be followed by an interface reset.

Configuration example 1:

REG0 = 0x99
REG1 = 0x99
REG2 = 0x19
REG3 = 0xD7
REG4 = 0xA3
REG5 = 0x00
REG6 = 0xFF
REG7 = 0x00
REG8 = 0xA2
REG9 = 0x00
configures the modulator as follows:
symbol rate x 4 = 4 MHz
offset carrier = 10 KHz
signal gain = 255 (maximum)
internal clock
unsigned output format
BPSK
no spectrum inversion
interpolation on
output data is pushed to the next module

With this configuration, the modulator will synthesize an unmodulated 10 KHz sinewave on the I-channel port, in unsigned format for direct connection to the A/D converter module.

Configuration example 2:

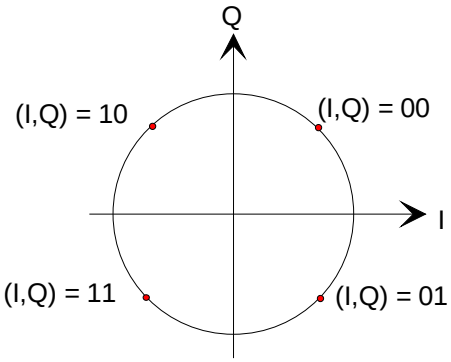
REG0 = 0xFF
REG1 = 0xFF
REG2 = 0xFF
REG3 = 0xFF
REG4 = 0xFF
REG5 = 0xFF
REG6 = 0xFF
REG7 = 0xFF
REG8 = 0x94
REG9 = 0x00
configures the modulator as follows:
symbol rate x 4 = 39999997.6 Hz
offset carrier = -2.38 Hz
signal gain = 255 (maximum)
internal clock
2's complement output format
QPSK
test pattern 2047-bit pseudo-random sequence
no spectrum inversion

interpolation on
Not differentially encoded.

Operation

Phase mapping

The nominal phase map follows Gray encoding as illustrated below:



REG8(6) causes a spectrum inversion by changing the Q sign.

Configuration Files

In order to provide for configuration flexibility without unduly increasing the hardware complexity, some features require uploading different firmware into the ComBlock using the ComBlock control center.

- Channel filter (raised cosine square root) rolloff: 20%, 25% and 40%.

All firmware versions can be downloaded from www.comblock.com/download.

COM-1002-A
BPSK/QPSK/OQKSK modulator 20% rolloff.

COM-1002-B
BPSK/QPSK/OQKSK modulator 25% rolloff.

COM-1002-E
BPSK/QPSK/OQKSK modulator 40%.

Differential Encoding

In low data rate applications where phase noise may become a problem, link performances can be improved by using differential encoding. At the encoder, the symbol information transforms into a phase shift, not an absolute phase. For QPSK, the phase shift is as follows:
The symbol 00 is mapped into +0 deg
The symbol 01 is mapped into +90 deg
The symbol 10 is mapped into +180 deg
The symbol 11 is mapped into +270 deg

For BPSK, the phase shift is as follows:
The bit 0 is mapped into +0 deg
The bit 1 is mapped into +180 deg

Unique Word

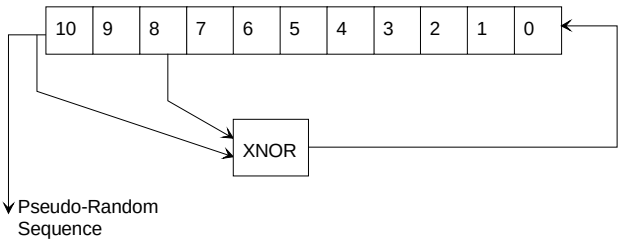
A unique word can be inserted periodically every 2048 data symbols to facilitate fast acquisition at the demodulator. This feature should only be enabled when used in conjunction with a compatible demodulator (i.e. designed to recognize this specific unique word and frame length).

The unique word is 32-bit long:
01011010 00001111 10111110 01100110 (binary)
0x 5A 0F BE 66 (hex)
The most significant bit (left-most) is transmitted first.

The unique word is always modulated as differentially encoded BPSK, irrespective of the modulation selected for the following 2048 symbols.

Pseudo-Random Bit Stream

A periodic pseudo-random sequence can be used as modulator source instead of the input data stream. A typical use would be for end-to-end bit-error-rate measurement of a communication link. The sequence is 2047-bit long maximum length sequence generated by an 11-tap linear feedback shift register:



The first 100 bits of the PN sequence are as follows:
0000000000 0111111111 0011111110 0001111100
1100111000 0000010011 1111010001 1110110100
1101001100 0011000001

Timing

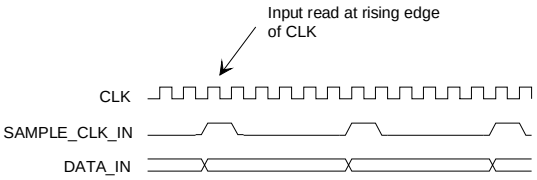
The I/O signals are synchronous with the rising edge of the reference clock CLK (i.e. all signals

transitions always occur after the rising edge of the reference clock CLK). The maximum CLK frequency is 40 MHz.

The maximum modulation symbol rate is equal to the reference clock frequency CLK/4.

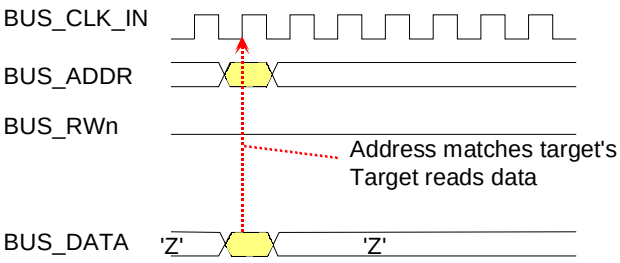
Input

Point to Point connection (REG9 bit4 = 0)

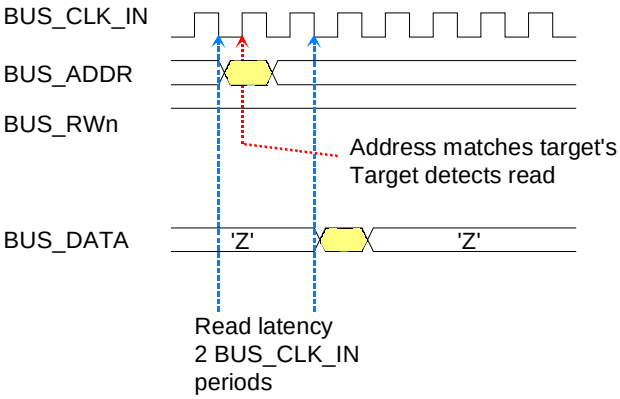


Input

Point to Multi-points connection (REG9 bit4 = 1). COM-1002 is a bus slave. It always listens to BUS_CLK_IN, BUS_ADDR, BUS_RWN.

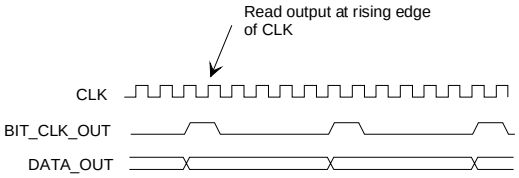


Master writes data streams to COM-1002 target(s)



Master reads flow control from COM-1002 target

Output



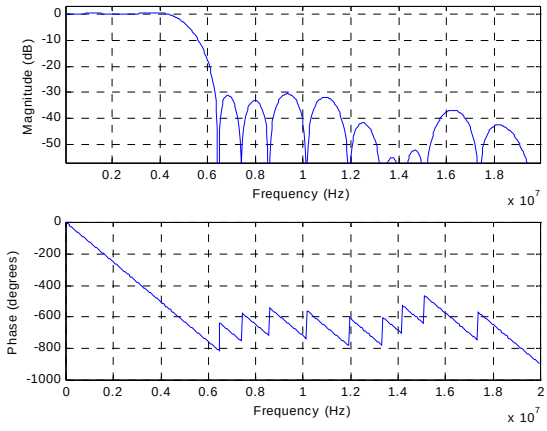
Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
TP1	Symbol rate x 4
TP2	Input data, DATA_IN(0)
TP3	Input data, DATA_IN(1)
TP4	Output I channel MSB, DATA_I_OUT(9)
TP5	Unique word flag, '1' during 32-bit unique word insertion.
TP6	Modulator input data stream, I-channel
TP7	Modulator input data stream, Q-channel
TP8	Modulator input symbol clock
TP9	PRBS-11 test sequence
TP10	PRBS-11 periodic start of test sequence

Performance

Filter Response (20% rolloff)

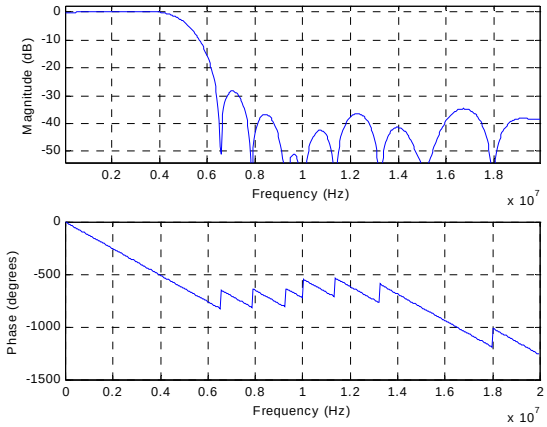


*(filter response normalized for 4*symbol rate = 40 MHz)*

The raised cosine square root filter with 20% rolloff is a 29-tap FIR filter with the following impulse response:
Coeff(0) = -8/1024
Coeff(1) = -16/1024
Coeff(2) = -8/1024
Coeff(3) = 8/1024

Coeff(4) = 24/1024
Coeff(5) = 24/1024
Coeff(6) = 12/1024
Coeff(7) = -16/1024
Coeff(8) = -48/1024
Coeff(9) = -52/1024
Coeff(10) = -16/1024
Coeff(11) = 64/1024
Coeff(12) = 160/1024
Coeff(13) = 240/1024
Coeff(14) = 272/1024
Coeff(j=15:28) = coeff(28-j);

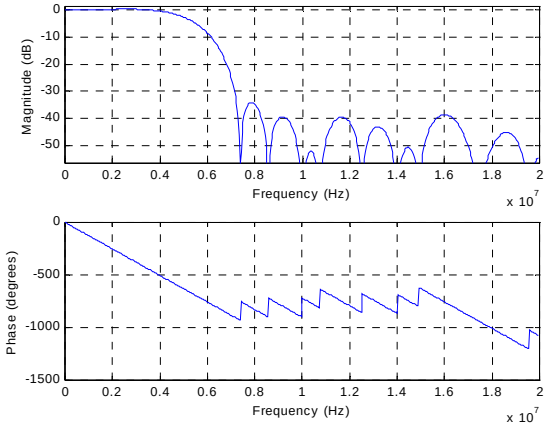
Filter Response (25% rolloff)



*(filter response normalized for 4*symbol rate = 40 MHz)*

The raised cosine square root filter with 25% rolloff is a 29-tap FIR filter with the following impulse response:
Coeff(0) = -4/1024
Coeff(1) = -12/1024
Coeff(2) = -8/1024
Coeff(3) = 2/1024
Coeff(4) = 16/1024
Coeff(5) = 24/1024
Coeff(6) = 12/1024
Coeff(7) = -16/1024
Coeff(8) = -48/1024
Coeff(9) = -48/1024
Coeff(10) = -16/1024
Coeff(11) = 64/1024
Coeff(12) = 160/1024
Coeff(13) = 240/1024
Coeff(14) = 272/1024
Coeff(j=15:28) = coeff(28-j);

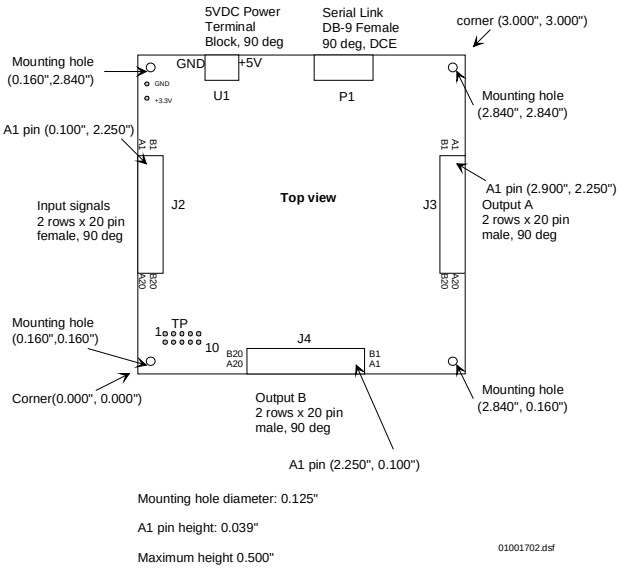
Filter Response (40% rolloff)



*(filter response normalized for 4*symbol rate = 40 MHz)*

The raised cosine square root filter with 40% rolloff is a 29-tap FIR filter with the following impulse response:
Coeff(0) = 4/1024
Coeff(1) = 1/1024
Coeff(2) = -4/1024
Coeff(3) = -4/1024
Coeff(4) = 2/1024
Coeff(5) = 12/1024
Coeff(6) = 14/1024
Coeff(7) = -2/1024
Coeff(8) = -30/1024
Coeff(9) = -48/1024
Coeff(10) = -24/1024
Coeff(11) = 48/1024
Coeff(12) = 152/1024
Coeff(13) = 248/1024
Coeff(14) = 284/1024
Coeff(j=15:28) = coeff(28-j);

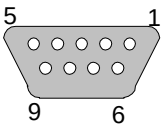
Mechanical Interface



Pinout

Serial Link P1

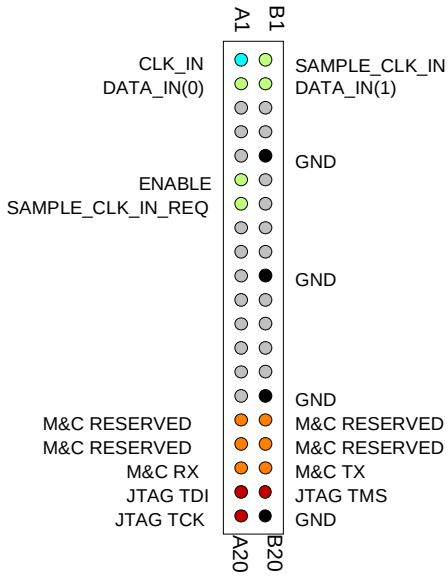
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



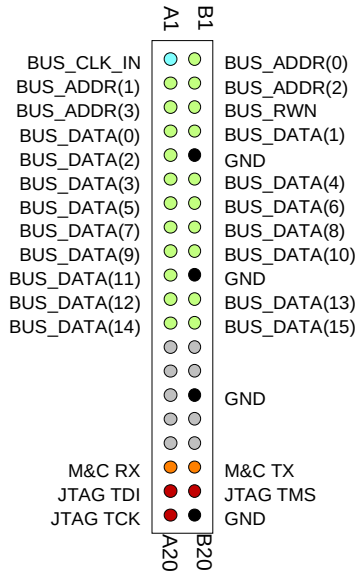
DB-9 Female

2 Transmit
3 Receive
5 Ground

Input Connector J2

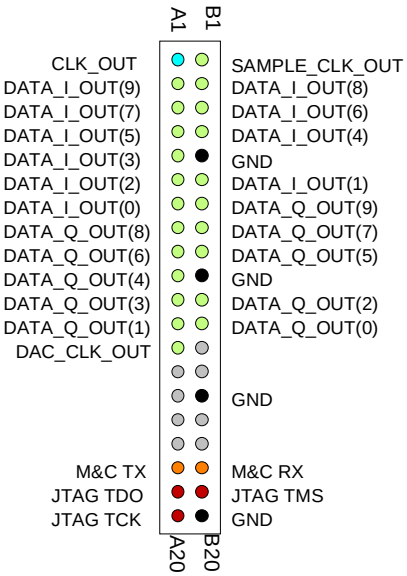


This connector is used for point-to-point input, i.e. direct connection between two ComBlocks when control register REG9(4) = '0'.

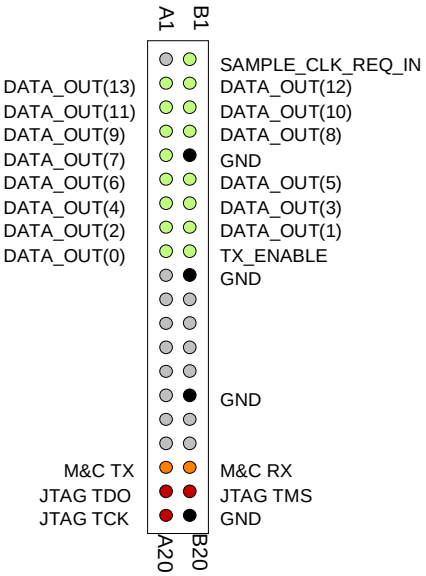


This connector is used for point-to-multipoint (bus) connection when control register REG9(4) = '1'. COM-1002 is a bus slave. It always listens to BUS_CLK_IN, BUS_ADDR, BUS_RWN.

Output Connectors J3, J4



This connector is used when output data is pushed out (configuration REG9 bit2 = 0).



This connector is used when output data is pulled out by the next module (configuration REG9 bit 2 = 1).

I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-1010 Convolutional encoder	COM-1001 BPSK/QPSK/OQPSK Demodulator (back to back)
COM-7001 Turbo Code Error Correction	COM-2001 digital-to-analog converter (baseband).
COM-8001 Pattern generator 256MB	COM-4004 70 MHz IF modulator
COM-8004 Signal diversity splitter	COM-1023 BER generator, Additive White Gaussian Noise Generator
COM-5003 TCP-IP / USB Gateway	COM-1024 Multipath simulator.

Configuration Management

This specification is to be used in conjunction with VHDL software revision 32.

ComBlock Ordering Information

COM-1002
BPSK/QPSK/OQKSK modulator

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