COM-1005
BIT ERROR RATE MEASUREMENT
VHDL SOURCE CODE OVERVIEW

Overview

The COM-1005 ComBlock Module comprises two pieces of software:

- VHDL code to run within the FPGA for all signal processing functions.
- C/Assembly code running within the Atmel AT90S8515 or ATMega8515L microprocessor for non application-specific monitoring and control functions.

The VHDL code interfaces to the monitoring and control functions by exchanging byte-wide registers on the Atmel microcontroller 8-bit data bus. The control and monitoring registers are defined in the specifications [1].

The Atmel microprocessor code is generic (i.e. non application specific), not user-programmable and functionally transparent to the user. It is thus not described here.

The COM-1005 VHDL code runs on the generic COM-1000 hardware platform. The schematics [2] for this platform are available in this CD.

Reference documents

[1] specifications: com1005.pdf

[2] hardware schematics: com_1000schematics.pdf

[3] VHDL source code in directory com-1005_013\src

[4] Xilinx ISE project files com-1005_013\com-1005.npl

[5] .ucf constraint files com-1005_013\src\com1005.ucf

[6] .mcs FPGA bit files com-1005_013\ com1005_013.mcs

Configuration Management

The current software revision is 13.

Configuration Options

No option.

VHDL development environment

The VHDL software was developed using two development environments:

(a) Xilinx ISE 4.1 with Synopsys FPGA Express 3.6 as synthesis tool.

(b) Xilinx ISE 6.3 with XST as synthesis tool.

Target FPGA

The VHDL code was synthesized for the Xilinx Spartan-II XC2S200-5PQ208 FPGA.

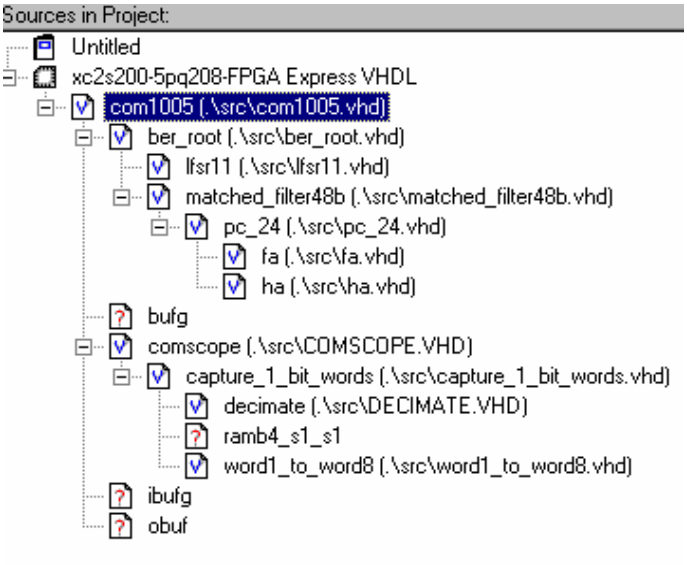
Xilinx-specific code

The VHDL source code was written in generic VHDL with few Xilinx primitives. No Xilinx CORE is used. The Xilinx primitives are:

- BUFG
- IBUFG
- OBUF
- RAMB4_S1_S1

MSS • 18221 Flower Hill Way #A • Gaithersburg, Maryland 20879 • U.S.A.
Telephone: (240) 631-1111 Facsimile: (240) 631-1676 www.ComBlock.com

VHDL software hierarchy



The code is stored with one, and only one, entity per file as shown above.

The root program (highlighted) is *com1005.vhd.*

Clock / Timing

The software uses a single 40 MHz clock, CLK_IN2, as provided externally through pin A1 of the J2 input connector. CLK_IN2 served a triple purpose: (a) internal processing clock, (b) synchronous input clock and (c) synchronous output clock. The code is written to meet the timing requirements on the target FPGA at a speed of at least 40 MHz.

Principle of operation

The COM-1005 expects a 2047-bit periodic pseudo-random data sequence. It first attempts to detect the 2047-bit periodic nature of the input data stream and synchronizes with it. Once synchronized, the COM-1005 compares the input data stream with the synchronized internal replica. Bit errors are counted in windows 1000-bit to 1Gbit long, as selected by the user.

The COM-1005 is also capable of synchronizing with data streams subject to phase ambiguities in a preceding QPSK demodulator. QPSK phase ambiguities cause a remapping of the data stream two bits at a time. The four phase ambiguity combinations are detected during synchronization using four correlators (*matched_filter48b.vhd*). The actual phase map is listed within the COM-1001 specifications
www.comblock.com/download/com1001.pdf

The replica is generated by the component *lfsr11.vhd.*

FPGA Occupancy

```
Design Summary:
   Number of errors:      0
   Number of warnings:    4
   Number of Slices:                841 out of  2,352   35%
   Number of Slices containing
      unrelated logic:                0 out of    841    0%
   Number of Slice Flip Flops:      683 out of  4,704   14%
   Total Number 4 input LUTs:     1,203 out of  4,704   25%
      Number used as LUTs:                         1,046
      Number used as a route-thru:                   157
   Number of bonded IOBs:            39 out of    140   27%
      IOB Flip Flops:                              17
   Number of Block RAMs:              3 out of     14   21%
   Number of GCLKs:                   4 out of      4  100%
   Number of GCLKIOBs:                1 out of      4   25%
Total equivalent gate count for design:  63,083
Additional JTAG gate count for IOBs:  1,920
```

Contact Information

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E-mail: info@comblock.com