COM-1008 VARIABLE DECIMATION (1:1024) & PILOT TONE DETECTION

Key Features

- Variable decimation from 1 to 1024.
  Stage 1: anti-aliasing filter + fixed 1:2 decimation
  Stages 2,3,4,5:
  anti-aliasing filter + fixed 1:4 decimation
  Stage 6: anti-aliasing filter.
  Stage 0 or 7: x2 interpolation + variable N:2^{24} decimation.
- Maximum 40 Msamples complex input sampling rate.
- AGC control for analog circuit.
- Pilot tone detection and accurate frequency measurement for aided acquisition.
- Single 5V supply.
- Connectorized 3"x 3" module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom) .
- Interfaces with 5V and 3.3V logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1008.pdf.
These specifications are subject to change without notice.

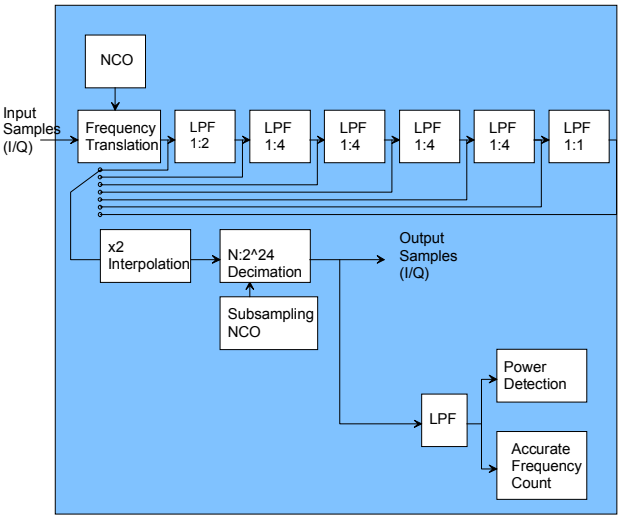
For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

Justification

In many receiver architectures, the signal digitization is performed at a fixed high sampling rate, often orders of magnitude larger than the desired signal bandwidth. This has many advantages: from being able to perform agile frequency conversion in the digital domain, to providing modulation and data rate flexibility.

Sampling reduction from the high A/D sampling clock to a bandwidth just above twice the modulation bandwidth (Nyquist!) is performed by successive steps of anti-aliasing filter and decimation. In order to minimize implementation complexity, multiple small decimation steps are preferred to a single large decimation step.

Block Diagram



Variable Decimation + Pilot Tone Detection
(Variable decimation stage last)

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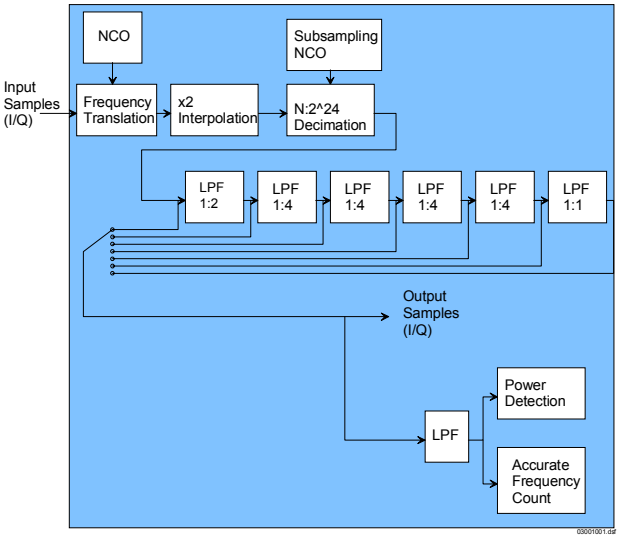


Variable Decimation + Pilot Tone Detection (Variable decimation stage first)

Electrical Interface

The input signals are synchronous with the rising edge of the reference clock ADC_CLK_IN (i.e. all signals transitions always occur after the rising edge of the clock).

The output signals are synchronous with the rising edge of the reference clock CLK_IN / CLK_OUT (i.e. all signals transitions always occur after the rising edge of the clock).

Inputs / Outputs

Input Module Interface	**Definition**
DATA_I_IN[9:0]	Samples from the A/D converter in-phase channel Format: 10-bit unsigned.
DATA_Q_IN[9:0]	Samples from the A/D converter quadrature channel. Format: 10-bit unsigned.
ADC_CLK_IN	A/D sampling clock. Read samples at rising edge of ADC_CLK_IN. Determines the input sampling frequency $\mathbf{f_s}$. Maximum $\mathbf{f_s}$ is 40 MHz.
AGC_OUT	Output. When this demodulator is connected directly to an analog receiver, it generates a pulse-width modulated signal to control the analog gain prior to A/D conversion. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3V is the minimum gain.
CLK_IN	Input reference clock used to generate the internal processing clock CLK and the output clock CLK_OUT. Its frequency must be such that $\mathbf{f_s} \le \mathbf{f_{clk}} \le 40$ MHz.
Output Module Interface (Option A)	**Definition**
DATA_I_OUT[9:0]	Output data samples. In-phase channel. 10-bit precision. Format: 2's complement or unsigned selected by configuration REG3 bit 6.
DATA_Q_OUT[9:0]	Output data samples. Quadrature channel. 10-bit precision. Same format as DATA_I_OUT.
SAMPLE_CLK_OUT	Output sample clock. One CLK-wide pulse. Read output data at rising edge of CLK when SAMPLE_CLK_OUT = '1'
DAC_CLK_OUT	Output sampling clock for Digital to Analog Converters. DAC reads the output sample at the rising edge.
Output Module Interface (Option B, 16-bit data bus)	**Definition**
BUS_DATA[15:0]	16-bit data bus (I/O)
BUS_A[6:0]	Address bus (I). High impedance output when BUS_IOMOD# = '1' or when address BUS_A is out of range.
BUS_IOMOD#	Module selection, active low (I)
BUS_CLK	Bus clock (I)
BUS_R/W#	Read/Write# (I)
BUS_READY#	Bus ready flag, active low (O). High impedance output when BUS_IOMOD# = '1' or when address BUS_A is out of range.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 300mA.

Configuration (via Serial Link / LAN)

Complete assemblies can monitored and controlled centrally over a single serial or LAN connection.

The module configuration parameters are stored in non-volatile memory.

Parameters	Configuration
Fine frequency translation ($f_{translation}$)	Fine frequency translation prior to narrow band filtering and decimation. Used to complement the RF frequency tuning, which has usually large frequency steps. Units: $f_{translation}$ / $\mathbf{f_s}$ * 2^24, where $\mathbf{f_s}$ is the sampling frequency. 2's complement signed representation. REG0 = bit 7-0 REG1 = bit 15 – 8 REG2 = bit 23 – 16
Filtering / Decimation (1:2) stage 1 bypass	0 = enable 1 = bypass REG3 bit 0
Filtering / Decimation (1:4) stage 2 bypass	0 = enable 1 = bypass REG3 bit 1
Filtering / Decimation (1:4) stage 3 bypass	0 = enable 1 = bypass REG3 bit 2
Filtering / Decimation (1:4) stage 4 bypass	0 = enable 1 = bypass REG3 bit 3
Filtering / Decimation (1:4) stage 5 bypass	0 = enable 1 = bypass REG3 bit 4
Filtering stage 6 bypass	0 = enable 1 = bypass REG3 bit 5
Output sample format	0 = unsigned 1 = 2's complement REG3 bit 6
Freeze monitoring data	As the monitoring data is constantly changing, it is important to be able to prevent changes while reading a multi-byte parameter. Write a zero in bit 7 to freeze the monitoring data prior to reading it. Write a one to re-enable the update. REG3 bit 7
Variable decimation ratio	The first or last decimation stage (following the x2 interpolation, see block diagram) is variable. The variable decimation value is computed as N:2^{24}, where N is always less than 2^{23} –1. Example: 1:2 decimation: N = 2^{23} –1 1:4 decimation: N = 2^{22} 23 bit unsigned integer. REG4: bit 7-0 REG5: bit 15-8 REG6: bit 22-16
Variable decimation stage location	The variable decimation can be implemented as the first or the last decimation stage. Use as first decimation stage if the analog anti-aliasing filter prior to the A/D conversion is small with respect to the sampling frequency $\mathbf{f_s}$. 1 = first decimation stage 0 = last decimation stage REG6 bit 7

Monitoring (via Serial Link / LAN)

Parameters	Monitoring
Option/Version	Returns '1008xy' when prompted for the option x and version y number.
Pilot tone power measurement	REG7: bit 7 – 0 REG8 bit 2 – 0: bit 10 – 8
Pilot tone frequency measurement	Number of zero crossing detected over 2^{14} output samples. There are 4 zero crossings per period. REG8 bit 7 - 3: bit 4 – 0 REG9 bit 6 - 0: bit 11 – 5
Pilot tone frequency sign	0 if positive 1 if negative REG9 bit 7
IF AGC Gain	8 most significant bits of the IF/RF gain settings controlled by the IF/RF AGC. REG10 bit 7-0

Test Points

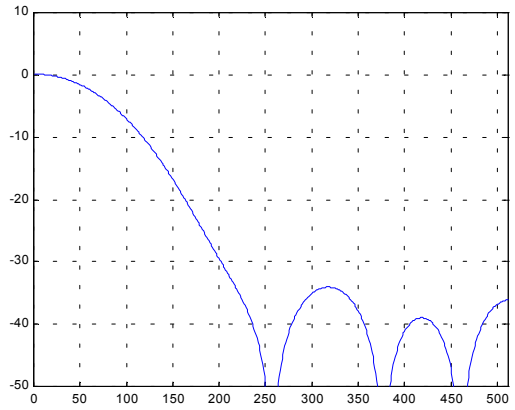
Test points are provided for easy access by an oscilloscope probe. Most of the test points are used to monitor the output data bus interface (firmware option –B).

Test Point	Definition
TP1	Input sampling clock
TP2	Output bus MODIOn (module select)
TP3	Output data bus address 0 decode
TP4	Output data bus address 1 decode
TP5	Output data bus address 2 decode
TP6	Output data bus address 3 decode
TP7	Output elastic buffer write pointer LSB
TP8	Output elastic buffer write pointer MSB
TP9	Output elastic buffer read pointer LSB

TP10	Output elastic buffer read pointer MSB

Operations

Anti-Aliasing filter (single stage)



Each anti-aliasing filter is an 11-tap FIR filter with the following impulse response:
Coeff(0) = 0.0156;
Coeff(1) = 0.0313;
Coeff(2) = 0.0703;
Coeff(3) = 0.1250;
Coeff(4) = 0.1719;
Coeff(5) = 0.1875;
Coeff(6) = 0.1719;
Coeff(7) = 0.1250;
Coeff(8) = 0.0703;
Coeff(9) = 0.0313;
Coeff(10) = 0.0156

The –3dB bandwidth is 0.126*(sampling frequency at the filter input).

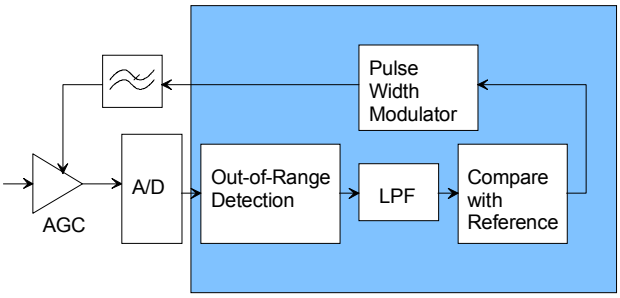
AGC

The purpose of this AGC is to prevent saturation at the external A/D converter(s) while making full use of the 10-bit A/D converter dynamic range. The principle of operations is outlined below:

(a) out-of-range at the A/D converter is detected. An out-of-range condition occurs if the quantized A/D samples are equal to either “1111111111” or “0000000000”.

(b) The AGC will adjust the analog circuitry gain so that out-of-range conditions do not occur more than 1 in 64 samples in the average.

(c) The resulting gain control signal is a pulse-width modulated (PWM) signal with 10-bit precision.



AGC principle

The analog circuit shall filter this 3.3V low-voltage TTL PWM signal with a low-pass filter prior to controlling the analog gain. The PWM is randomized and its spectral distribution shifted to the higher frequencies so as facilitate the analog low-pass filter design.

The AGC loop bandwidth is typically 1 Hz when used in conjunction with COM-30xx receivers and a 40 MHz processing clock. The loop response time is assymetrical: it responds faster to a saturation condition than to a ‘low signal’ condition.

The gain control signal will increase if too many out-of-range conditions occur.

Pilot Tone Detection

It is sometimes desirable to detect the presence of reference pilot tones (i.e. unmodulated carriers), for example to identify a satellite beam. In addition, many satellite/wireless networks use pilot tones for frequency reference, for the purpose of calibrating receivers frequency.

This module includes both power and frequency measurement.

The frequency measurement is based on the number of zero crossings by the in-phase (I) and quadrature (Q) signals as detected over a period of 2^14 output samples. In order to improve the signal to noise ratio of the pilot tone, the received signal undergoes another low-pass filtering stage of bandwidth $f_{so}/8$, where f_{so} is the output sampling clock.

The frequency measurement is signed. It is accurate to within $f_{so}/2^{16}$ Hz.

Output Interfaces

Two distinct output interfaces can be selected at the time of firmware upload:
COM-1008-A Interface with other ComBlocks
COM-1008-B Interface with a 16-bit data bus.

These two firmware versions can be downloaded from www.comblock.com/download

16-bit data bus

The interface consists of a 7-bit address bus, a 16-bit data bus, clock BUS_CLK, module selection BUS_MODIO#, and read/write flag BUS_R/W#.

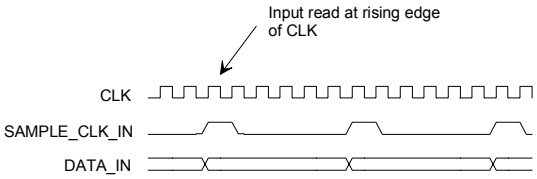
Signals are 3.3V low-voltage TTL. The inputs are 5V tolerant.

The output data samples are mapped into a 16-bit data bus as follows:

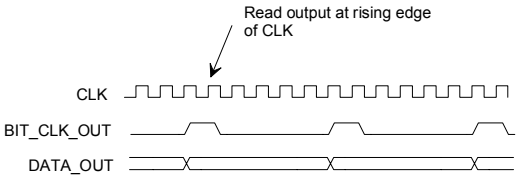
Address BUS_A[6:0]	**Data BUS_DATA[15:0]**
0	DATA_I_OUT[9:0] Output data samples. In-phase channel. 10-bit signed. 2's complement. Bit 15 on the data bus indicates whether the output elastic buffer is empty (0) or contains I/Q samples (1). When the output buffer is empty, the data bits 9:0 are meaningless. The host controller is expected to poll this bus address 0 until data is available, i.e. bit 15 = 1. Bus data bits 14:10 are unused.
1	DATA_Q_OUT[9:0] Output data samples. In-phase channel. 10-bit signed. 2's complement. As in-phase (I) and quadrature (Q) samples are inseparable, the output elastic buffer read pointer is incremented after reading the Q sample. It is thus important to read the I sample at bus address 0 before reading this Q sample at bus address 1. Bus data bits 15:10 are unused.
2	Monitoring registers REG7 (LSB) and REG8 (MSB)
3	Monitoring registers REG9 (LSB) and REG10 (MSB)

Timing

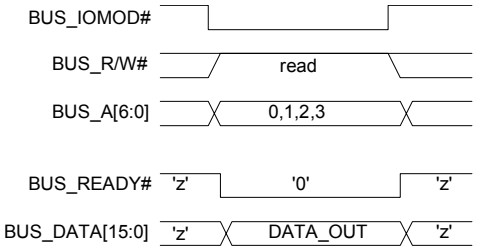
Input



Output (Firmware Option –A)

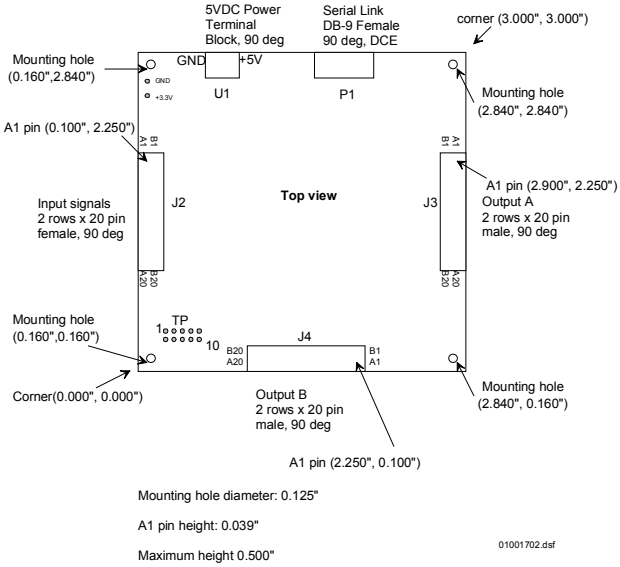


Output (Firmware Option –B)



Read cycle

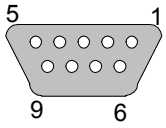
Mechanical Interface



Pinout

Serial Link P1

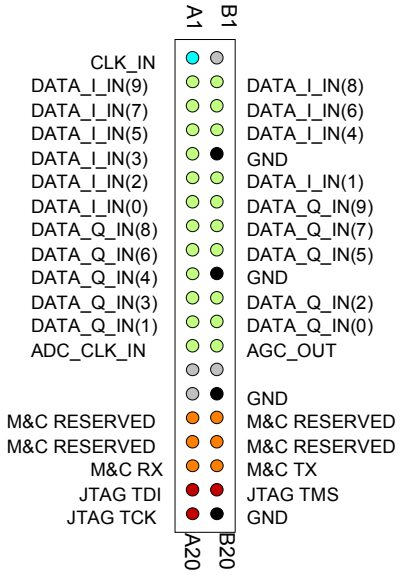
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



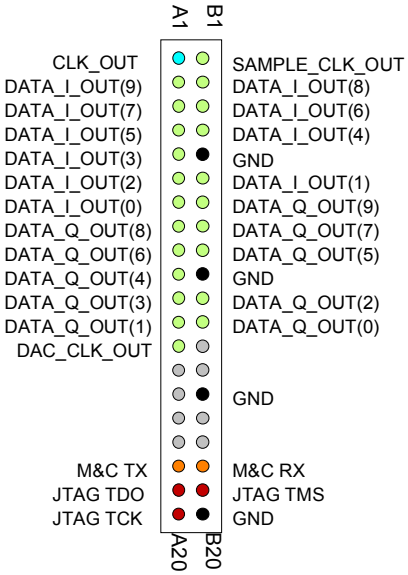
DB-9 Female

2 Transmit
3 Receive
5 Ground

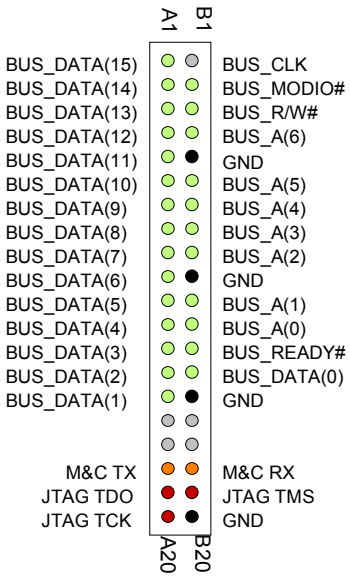
Input Connector J1



Output Connectors J3, J4 (Firmware Option -A)



Output Connector J3 (Firmware Option -B)



I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-300x RF receivers	COM-1001 BPSK/QPSK/OQPSK Demodulator
	COM-1011/18 DSSS Demodulator
	COM-1027 FSK/MSK/GFSK/GMSK Demodulator
	COM-2001 digital-to-analog converter (baseband).

ComBlock Ordering Information

COM-1008 VARIABLE DECIMATION

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