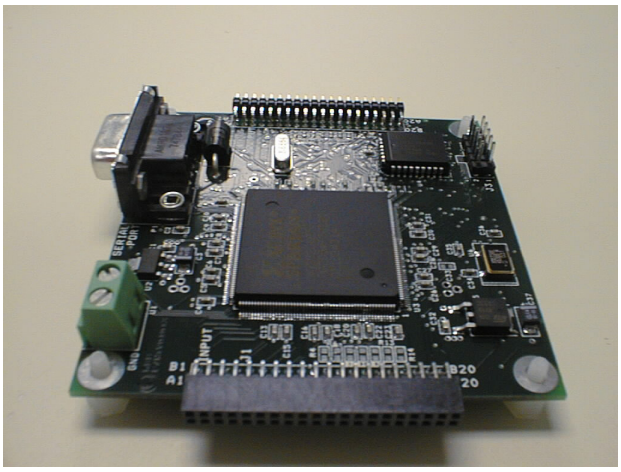
COM-1009 VITERBI ERROR CORRECTION DECODER K=7, K=5

Key Features

- Viterbi decoder for error correction.
- Selectable rate and constraint length:
  K = 5, rate 1/7
  K = 7, rates ½, ¾, 7/8
- Support for the following standards:
  Intelsat IESS-308/309
  DVB ETS 300 421
  DVB ETS 300 744
- Differential decoder to resolve bit stream inversion.
- Maximum throughput (at input): 8Mbps.
- 4-bit soft-quantized demodulated bits.
- Single 5V supply
- Connectorized 3"x 3" module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right). Interfaces with 3.3V LVTTL logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1009.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .



Electrical Interface

Input Module Interface	**Definition**
DATA_IN[3:0]	4-bit soft-quantized demodulated bits. Unsigned representation: 0000 for maximum amplitude '0', 1111 for maximum amplitude '1'.
SAMPLE_CLK_IN	Input signal sampling clock. One CLK-wide pulse. Read the input signal at the rising edge of CLK when SAMPLE_CLK_IN = '1'.
SOF_IN	Optional start of frame reset input. Used only in block mode. Ignored in continuous mode. 1 CLK-wide pulse. Aligned with SAMPLE_CLK_IN.
CLK_IN	Input reference clock for I/O and internal processing. Maximum speed is 40 MHz.
Output Module Interface	**Definition**
DATA_OUT	Output data stream. 1-bit serial
SAMPLE_CLK_OUT	Output symbol clock. One CLK-wide pulse. Read the output signals at the rising edge of CLK when SAMPLE_CLK_OUT = '1'.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.

MSS • 18221 Flower Hill Way #A • Gaithersburg, Maryland 20879 • U.S.A.
Telephone: (240) 631-1111 Facsimile: (240) 631-1676 www.ComBlock.com
 Issued 6/15/2008

Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional CLK_IN . The maximum power consumption at 40 MHz is 500mA.

Important: I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration (via Serial Link / LAN)

Complete assemblies can monitored and controlled centrally over a single serial or LAN connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

Parameters	Configuration
Constraint length K and rate R	COM-1009A firmware installed 0001 = (K = 7, R=1/2) 0011 = (K = 7, R=3/4) 0101 = (K = 7, R=7/8) COM-1009B firmware installed 0000 = (K=5, R=1/7) REG0 bits 4-1
Differential Decoding	0 = disabled 1 = enabled REG0 bit 5
Continuous / Block mode	Determines whether the start of frame SOF_IN signal should be enabled for resetting the decoder at the start of a block. 0 = continuous 1 = block mode. REG0 bit 6
Input format	0 = hard decision (uses input signal DATA_IN(3) only). 1 = 4-bit soft quantized input. REG0 bit 7
Measurement window	Number of bits in the window where raw bit errors (bit errors on the encoded bit stream) are computed: 000 = 1,000 011 = 1,000,000 REG1 bits 2 -0

Baseline configurations can be found at www.comblock.com/tsbasic_settings.htm and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

Monitoring (via Serial Link / LAN)

Status registers are read-only. Start to read at address 0 to latch in the multi-byte status words.

Parameters	Monitoring
Synchronized	Synchronized SREG0 bit 0
BER	Encoded stream bit errors detected over the specified BER measurement window. SREG1 = bits 7 – 0 (LSB) SREG2 = bits 15 – 8 SREG3 = bits 23 - 16

Digital Test Points

Test points are provided on the J1 header center row 2.

Test Point	Definition
TP1 (FPGA-side)	Solid '1' when the decoder is synchronized. Toggling otherwise.
TP2	Detected bit error in the encoded bit stream
TP3	Re-synchronization attempt. Each time the Viterbi decoder attempts to re-synchronize, it generates this pulse.
TP4	Actual received encoded bit stream. Compare with TP5.
TP5	Reconstructed encoded bit stream (by re-encoding the nearly error-free decoded bit stream). Compare with TP4.
DONE	'1' indicates proper FPGA configuration.

Implementation

K = 5

The generator polynomials for K = 5 R = 1/7 is

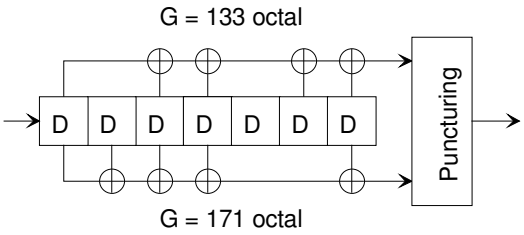
$G_0(x) = 1 + x + x^2 + x^4$
$G_1(x) = 1 + x^2 + x^3 + x^4$
$G_2(x) = 1 + x^2 + x^4$
$G_3(x) = 1 + x^2 + x^3 + x^4$
$G_4(x) = 1 + x + x^3 + x^4$
$G_5(x) = 1 + x + x^2 + x^4$
$G_6(x) = 1 + x + x^2 + x^3 + x^4$

K = 7

The generator polynomials for K = 7 R = ½ are

$G_0(x) = 1 + x^2 + x^3 + x^5 + x^6$
$G_1(x) = 1 + x + x^2 + x^3 + x^6$

133(octal) and 171(octal). The implementation is depicted below:

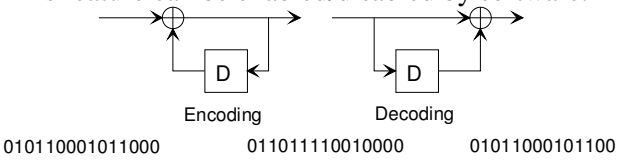


Rates other than ½ are implemented by puncturing the rate ½ encoded data stream. The puncturing pattern is as follows (1 denotes transmission, 0 blocking)

Rate ¾	G_0	110
	G_1	101
Rate 7/8	G_0	1111010
	G_1	1000101

Differential Decoding

Differential decoding can be used following FEC decoding as specified in Intelsat IESS-308/309. This feature can be enabled/disabled by software.



This mode compensates for any bit inversion occurring in the transmission channel (for example at a BPSK demodulator which cannot resolve the inherent 180deg phase ambiguity). For example, this mode should be enabled at the COM-1010 FEC encoder and COM-1009 FEC decoder when used in conjunction with the COM-1001 BPSK demodulator.

Self Synchronization

When the decoder detects that the bit error is greater than 25%, it attempts to re-synchronize. The resynchronization trigger event is counting 128 bit errors over a period of no more than 512 bits.

Bit Error Rate Measurement

The decoder estimates the bit error rate on the encoded bit stream by comparing the actual received bit stream with an estimate of the transmitted bit stream. This estimate is generated by re-encoding the nearly error-free decoded bit stream.

The algorithm is based on the proposition that the decoded bit stream is nearly error-free. If the decoded bit stream were error-free, then the re-encoded bit stream would be the actual transmitted encoded bit stream before bit errors occur in the transmission channel.

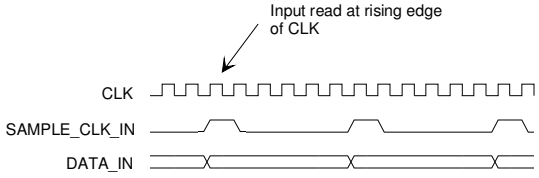
The bit error rate is computed over a window of N bits, where N is user-selectable though control register REG1.

Timing

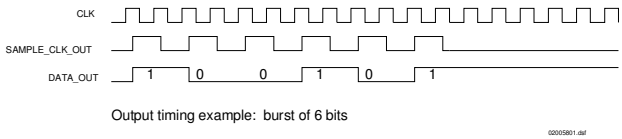
This module operates at an internal clock rate $\mathbf{f_{clk}}$ = 2*CLK_IN of 80 MHz. However, the maximum I/O clock (CLK_IN) is 40 MHz.

The I/O signals are synchronous with the rising edge of CLK_IN (i.e. all signals transitions always occur after the rising edge of the reference clock CLK_IN).

Input

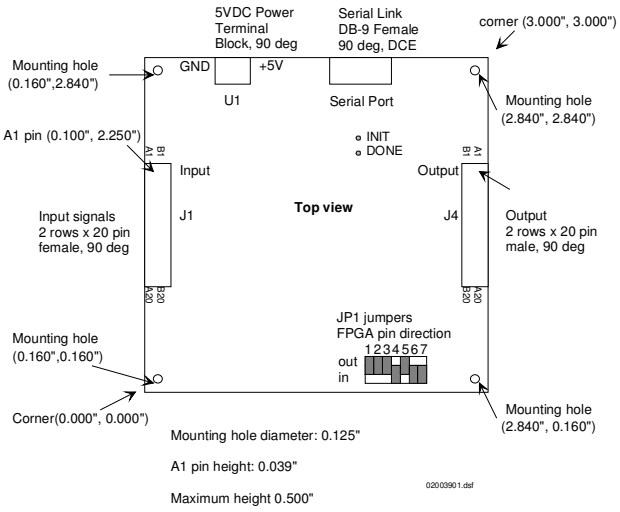


Output



The diagram above illustrates the bursty nature of the demodulated output. Typically, output bits are grouped in burst of 6 bits.

Mechanical Interface



Note: JP1 jumpers can be in any location "IN", 'OUT' or not installed.

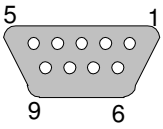
Schematics

The board schematics are available on-line at http://www.comblock.com/download/com_8001schematics.pdf

Pinout

Serial Link

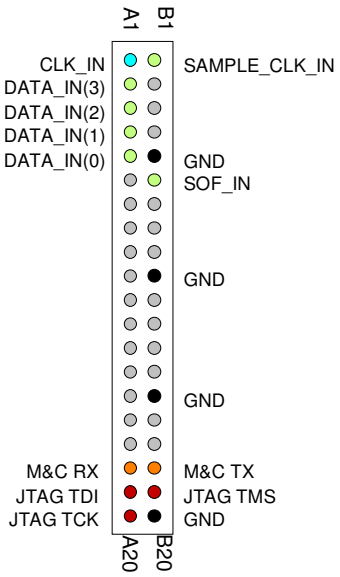
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



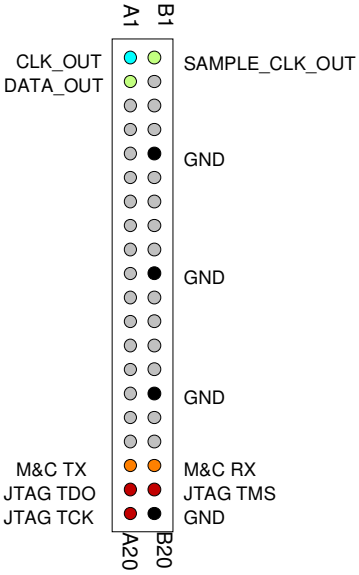
DB-9 Female

2 Transmit
3 Receive
5 Ground

Input Connector J1



Output Connector J4



01004202.dsf

I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-1001 BPSK/QPSK/OQPSK demodulator	COM-1005 BER measurement
COM-1011/1018 DSSS demodulator	COM-5003 TCP-IP / USB Gateway
COM-1027 FSK/MSK/GFSK/GMSK demodulator	COM-8002 Data acquisition 256MB.
COM-1023 BER generator, Additive White Gaussian Noise Generator	
COM-1010 Convolutional encoder (back to back)	

Configuration Management

This specification is to be used in conjunction with VHDL software revision 8.

ComBlock Ordering Information

COM-1009-A Viterbi error correction decoder, K=7
COM-1009-B Viterbi error correction decoder, K=5

MSS • 18221 Flower Hill Way #A •
Gaithersburg, Maryland 20879 • U.S.A.
Telephone: (240) 631-1111
Facsimile: (240) 631-1676
E-mail: sales@comblock.com