COM-1009A VITERBI ERROR CORRECTION DECODER K=7
VHDL SOURCE CODE OVERVIEW

Overview

The COM-1009A ComBlock Module comprises two pieces of software:

- VHDL code to run within the FPGA for all signal processing functions
- C/Assembly code running within the Atmel AT90S8515 or ATMega8515L microprocessor for non application-specific monitoring and control functions.

The VHDL code interfaces to the monitoring and control functions by exchanging byte-wide registers on the Atmel microcontroller 8-bit data bus. The control and monitoring registers are defined in the specifications [1].

The COM-1009A VHDL code runs on the generic COM-8000 hardware platform. The schematics [2] for this platform are available in this CD.

Reference documents

[1] specifications: com1009.pdf

[2] hardware schematics: com_8000schematics.pdf

[3] VHDL source code in directory com-1009_008\src

[4] .ucf constraint file com-1009_008\src\com1009.ucf

[5] .mcs FPGA bit file com-1009_008\com1009A_008.mcs

Configuration Management

The current software revision is 8.

VHDL development environment

The VHDL software was developed using the Xilinx ISE 8.2/9.1 development environment. The synthesis tool is Xilinx XST.

Target FPGA

The VHDL code was synthesized for the Xilinx Spartan-IIE XC2S300E-6PQ208 FPGA.

Xilinx-specific code

The VHDL source code was written in generic VHDL with few Xilinx primitives. No Xilinx CORE is used. The Xilinx primitives are:

- BUFG
- IBUFG
- CLKDLL (x2)
- RAMB4_S1_S1
- RAMB4_S16_S16

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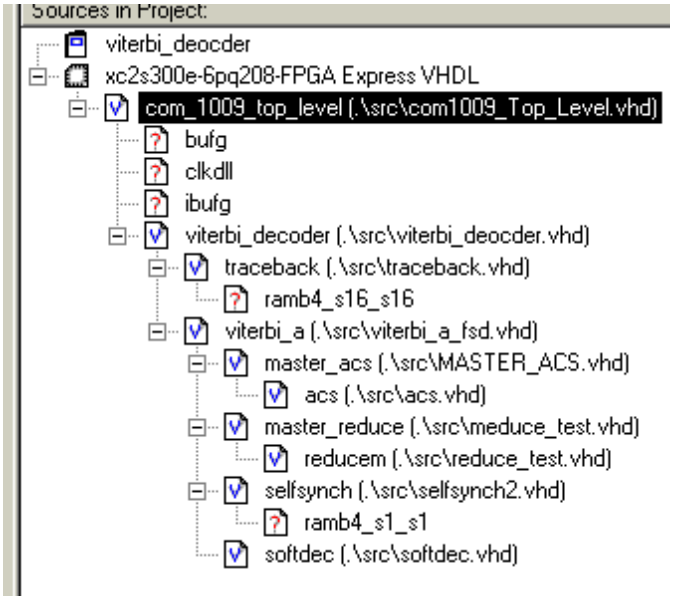
VHDL software hierarchy



The code is stored with one, and only one, entity per file as shown above.

Clock / Timing

The software uses a single master clock (CLK_IN2) which serves as input clock, output clock and reference for the double-frequency processing clock. The code is written to meet the timing requirements on the target FPGA at a speed of at least 80 MHz (40 MHz maximum frequency for CLK_IN2).

Contact Information

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Occupied Resources

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Design Information
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Command Line   : c:\Xilinx\bin\nt\map.exe -ise
C:/L3/com-1009_007/com-1009_007/ISE91.ise -intstyle ise -p xc2s300e-pq208-6 -cm
area -pr b -k 4 -tx off -o COM_1009_Top_Level_map.ncd COM_1009_Top_Level.ngd
COM_1009_Top_Level.pcf
Target Device  : xc2s300e
Target Package : pq208
Target Speed   : -6
Mapper Version : spartan2e -- $Revision: 1.36 $

Design Summary
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Number of errors:      0
Number of warnings:   33
Logic Utilization:
  Number of Slice Flip Flops:     5,093 out of  6,144   82%
  Number of 4 input LUTs:         4,697 out of  6,144   76%
Logic Distribution:
    Number of occupied Slices:                       3,070 out of  3,072   99%
    Number of Slices containing only related logic:  2,318 out of  3,070   75%
    Number of Slices containing unrelated logic:       752 out of  3,070   24%
        *See NOTES below for an explanation of the effects of unrelated logic
Total Number of 4 input LUTs:        5,512 out of  6,144   89%
      Number used as logic:                     4,697
      Number used as a route-thru:                815
   Number of bonded IOBs:            23 out of    142   16%
      IOB Flip Flops:                              15
   Number of Block RAMs:             11 out of     16   68%
   Number of GCLKs:                   4 out of      4  100%
   Number of GCLKIOBs:                3 out of      4   75%
```

```
   Number of DLLs:                    1 out of      4   25%

Total equivalent gate count for design:  267,043
```