COM-1010 CONVOLUTIONAL ENCODER

Key Features

- Convolutional encoder for error correction.
- Selectable rate and constraint length:
  K = 5, rate 1/7
  K = 7, rates ½, 2/3, ¾, 5/6, 7/8
  K = 9, rates 1/3, ½, 2/3
- Treillis Coding Modulation (TCM) encoder:
  Rate 2/3 (8-PSK)
  Rate ¾ (16-PSK)
- Continuous or Block mode operation.
- Support for the following standards:
  Intelsat IESS-308/309
  Intelsat IESS-310
  DVB ETS 300 421
  DVB ETS 300 744
  CCSDS 101.0-B-6
- Differential encoder.
- Maximum throughput (at output): 40 Mbps.
- On-board or external clock selection.
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Single 5V supply. Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom). Interfaces with 5V and 3.3V logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1010.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

Electrical Interface

Input Module Interface	**Definition**
DATA_IN	Input data stream
SAMPLE_CLK_IN	Input signal sampling clock. One CLK-wide pulse. Read the input signal at the rising edge of CLK when SAMPLE_CLK_IN = ‘1’.
SAMPLE_CLK_IN_REQ	One CLK-wide pulse output. Requests a sample from the module upstream. For flow-control purposes.
SOF_RESET	Optional start of frame reset input. Used only in block mode. Ignored in continuous mode. 1 CLK-wide pulse. Aligned with SAMPLE_CLK_IN.
CLK_IN	Input reference clock for synchronous I/O and processing. Yields internal CLK clock. Maximum frequency $\mathbf{f_{clk}}$ is 40 MHz.
Output Module Interface	**Definition**
DATA_OUT[3:0]	Output data stream. Can be one-bit serial, 2/3/4 bit parallel depending on the format selection. 2-bit parallel typically used for I/Q QPSK modulation. 3-bit parallel typically used for 8-PSK modulation. 4-bit parallel typically used for 16-PSK modulation.

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SAMPLE_CLK_OUT	Output symbol clock. One CLK-wide pulse. Read the output signals at the rising edge of CLK when SAMPLE_CLK_OUT = '1'.
SAMPLE_CLK_OUT_REQ	One CLK-wide pulse input. Requests for a sample from the module downstream. For flow-control purposes.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 300mA.

Configuration (via Serial Link / LAN)

Complete assemblies can monitored and controlled centrally over a single serial or LAN connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

Parameters	**Configuration**
Constraint length K and rate R	0000 = (K=5, R=1/7) 0001 = (K = 7, R=1/2, Intelsat) 0010 = (K = 7, R=2/3, Intelsat) 0011 = (K = 7, R=3/4, Intelsat) 0100 = (K = 7, R=5/6, Intelsat) 0101 = (K = 7, R=7/8, Intelsat) 0110 = (K = 9, R=1/3) 0111 = (K = 9, R=1/2) 1000 = (K = 9, R=2/3) 1001 = (TCM, K=7, R=2/3) 1010 = (TCM, K=7, R=3/4) 1011 = (K = 7, R=1/2, CCSDS) 1100 = (K = 7, R=2/3, CCSDS) 1101 = (K = 7, R=3/4, CCSDS) 1110 = (K = 7, R=5/6, CCSDS) 1111 = (K = 7, R=7/8, CCSDS) REG0 bits 4-1
Differential Encoding	0 = disabled 1 = enabled REG0 bit 5
Continuous / Block mode	Determines whether the SOF_RESET mode should be enabled for resetting the encoder at the start of a block. 0 = continuous 1 = block mode. REG0 bit 6
Output sample format	00 = 1 bit serial 01 = 2 bit parallel (I/Q) for connection to QPSK modulator. 10 = 3-bit parallel for connection to 8-PSK modulator. 11 = 4-bit parallel for connection to 16-PSK modulator This field is ignored when TCM mode is selected. REG1 bits 1-0
Internal pattern generation (test mode)	00 = test mode disabled 01 = counting sequence: When set, the baseband input is disabled and a periodic pattern is internally generated at the encoder input. The pattern consists of an 8-bit counter, MSB transmitted first. 10 = PRBS-11. internal generation of 2047-bit periodic pseudo-random bit sequence as modulator input. (overrides external input bit stream). Useful in measuring BER performances in conjunction with COM-1005. The test pattern bit rate is automatically set by the external sink module (typically a modulator) as part of the flow control mechanism. REG1 bits 3-2
Output symbol rate internal / external selection	In most cases, the COM-1010 throughput is determined by modules downstream (for example a modulator). There are, however, cases when the throughput is set using an internal NCO (for example when testing convolutional encoder and Viterbi decoder back to back). 0 = exter nal. Output symbol rate is based on SAMPLE_CLK_OUT_REQ samples requests from following module. 1 = internal. Output symbol rate is selected internally by the NCO frequency set in REG2/3/4. Sample requests SAMPLE_CLK_OUT_REQ are ignored. REG1 bit 4
Output symbol rate NCO	Internal generation of the output symbol rate. Ignore this field when the output symbol rate is determined by modules downstream. 24-bit signed integer (2's complement

	representation) expressed as fsymbol rate * 2^{24} / $\mathbf{f_{clk}}$. The internal processing clock $\mathbf{f_{clk}}$ is typically 40 MHz. REG2 = bits 7-0 (LSB) REG3 = bits 15 – 8 REG4 = bits 23 – 16 (MSB)

Baseline configurations can be found at www.comblock.com/tsbasic_settings.htm and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

Monitoring (via Serial Link / LAN)

Monitoring registers are read-only.

Parameters	Monitoring
Option o / Version v	Returns '1010ov' when prompted for option o and version v numbers.

ComScope Monitoring

Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-1010 signal traces and trigger are defined as follows:

Trace 1 signals	Format	Nominal sampling rate	Buffer length (samples)
1: Input bit stream or test pattern	Binary	1 sample /bit	4096
2:Output symbol request (internally set by NCO or externally by SAMPLE_CLK_OUT_REQ)	Binary	processing clock $\mathbf{f_{clk}}$	4096
Trace 2 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: Input bit clock	Binary	processing clock $\mathbf{f_{clk}}$	4096
2: Output bit stream DATA_OUT(0)	Binary	1 sample/bit	4096
Trace 3 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: SAMPLE_CLK_IN_REQ	Binary	processing clock $\mathbf{f_{clk}}$	4096
2: SAMPLE_CLK_OUT	Binary	processing clock $\mathbf{f_{clk}}$	4096
Trigger Signal	**Format**		
1: Start of internal PRBS11 test sequence	binary		
2: SOF_RESET	binary		

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the $\mathbf{f_{clk}}$ processing clock as real-time sampling clock.

In particular, selecting the $\mathbf{f_{clk}}$ processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.

Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
TP1	Input serial stream bit clock
TP2	Input serial stream data
TP3	Output serial stream bit clock
TP4	Output serial stream data
TP5	Start of the periodic LFSR-11 2047-bit test pattern.

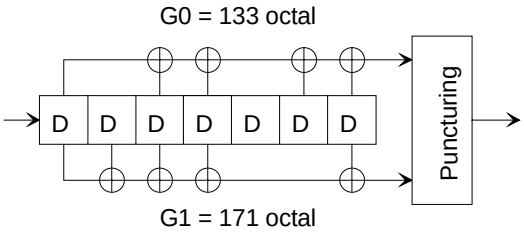
Implementation

K = 5

The generator polynomials for K = 5 R = 1/7 is
$G_0(x) = 1 + x + x^2 + x^4$
$G_1(x) = 1 + x^2 + x^3 + x^4$
$G_2(x) = 1 + x^2 + x^4$
$G_3(x) = 1 + x^2 + x^3 + x^4$
$G_4(x) = 1 + x + x^3 + x^4$
$G_5(x) = 1 + x + x^2 + x^4$
$G_6(x) = 1 + x + x^2 + x^3 + x^4$

K = 7 (Intelsat)

The generator polynomials for K = 7 R = ½ are
$G_0(x) = 1 + x^2 + x^3 + x^5 + x^6$
$G_1(x) = 1 + x + x^2 + x^3 + x^6$
133(octal) and 171(octal). The implementation is depicted below:

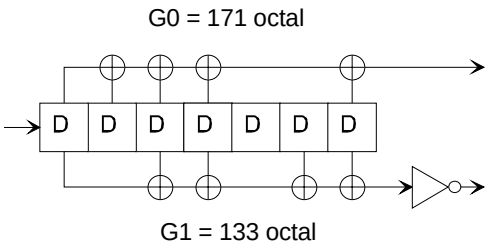


Rates other than ½ are implemented by puncturing the rate ½ encoded data stream. The puncturing pattern is as follows (1 denotes transmission, 0 blocking)

Rate 2/3	G_0	11
	G_1	10
Rate ¾	G_0	110
	G_1	101
Rate 5/6	G_0	11010
	G_1	10101
Rate 7/8	G_0	1111010
	G_1	1000101

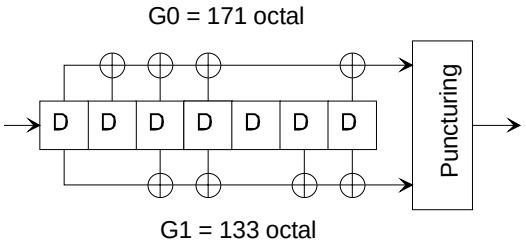
K = 7 (CCSDS)

The generator polynomials for K = 7 R = ½ are
$G_0(x) = 1 + x + x^2 + x^3 + x^6$
$G_1(x) = 1 + x^2 + x^3 + x^5 + x^6$
171(octal) and 133(octal). The implementation is depicted below:



Basic CCSDS convolutional encoder

The basic encoder inverts the G_1 output. When using puncturing, this inverter is removed.



CCSDS convolutional encoder with puncturing

Rates other than ½ are implemented by puncturing the rate ½ encoded data stream. The puncturing pattern is as follows (1 denotes transmission, 0 blocking)

Rate 2/3	G_0	10
	G_1	11
Rate ¾	G_0	101
	G_1	110
Rate 5/6	G_0	10101
	G_1	11010
Rate 7/8	G_0	1000101
	G_1	1111010

K = 9 R = 1/3

The generator polynomials for K = 9 R = 1/3 are
$G_0(x) = 1 + x^2 + x^3 + x^5 + x^6 + x^7 + x^8$.
$G_1(x) = 1 + x + x^3 + x^4 + x^7 + x^8$.
$G_2(x) = 1 + x + x^2 + x^5 + x^8$.

K = 9 R = ½, 2/3

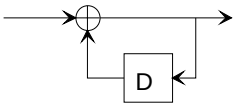
The generator polynomials for K = 9 R = 1/2 are
$G_0(x) = 1 + x + x^2 + x^3 + x^5 + x^7 + x^8$.
$G_1(x) = 1 + x^2 + x^3 + x^4 + x^8$.

The rate 2/3 is implemented by puncturing the rate ½ encoded data stream. The puncturing pattern is as follows (1 denotes transmission, 0 blocking):

Rate 2/3	G_0	11
	G_1	01

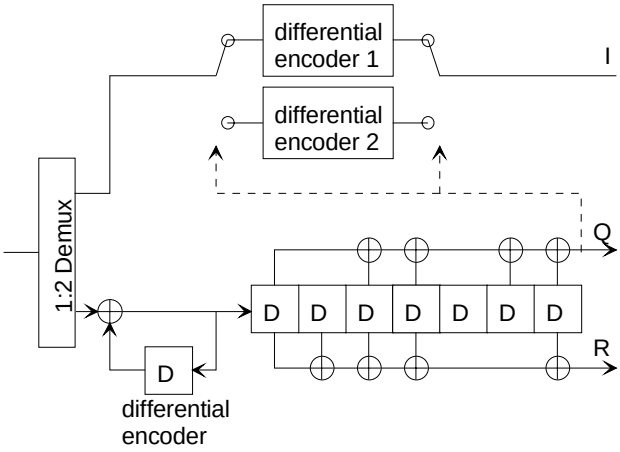
Differential Encoding

Differential encoding can be used prior to FEC encoding as specified in Intelsat IESS-308/309. This feature can be enabled/disabled by software.

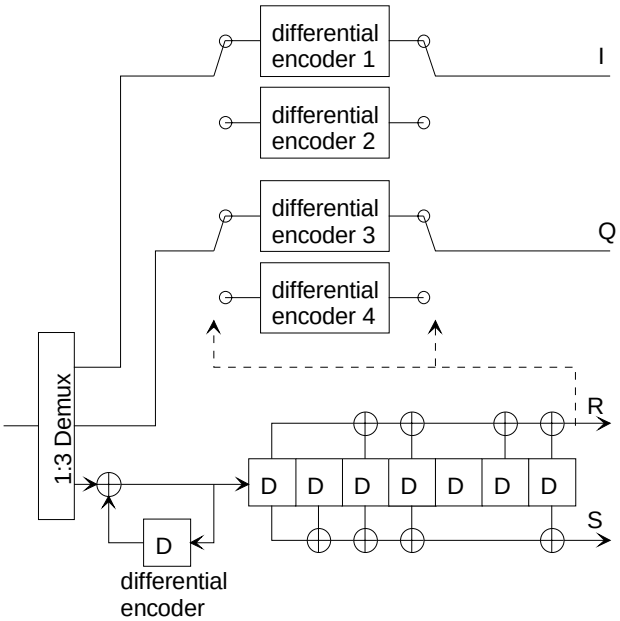


Treillis Coded Modulation (TCM) Encoder

As per Intelsat IESS-310 for rate 2/3 8-PSK.



TCM encoder, rate 2/3 for 8-PSK



TCM encoder, rate 3/4 for 16-PSK

Flow Control

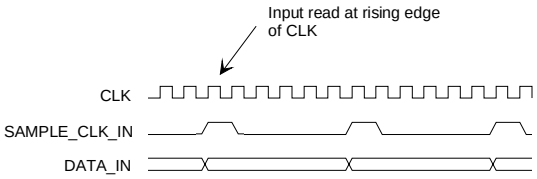
In most applications, the data samples are 'pulled' from the end module which is the timing reference. This is the case, for example when the reference real-time clock is the modulation rate. By 'pulled', we mean that the data processing is going downstream, whereby the clock requests are going in the opposite direction.

In order to cater to this requirement, the COM-1010 module includes a built-in numerically controlled oscillator which generates the SAMPLE_CLK_IN_REQ output based on the SAMPLE_CLK_OUT_REQ input. For example, if a rate ¾ puncturing is selected together with a 1-bit serial output, the NCO will generate 3 SAMPLE_CLK_IN_REQ output pulses for every 4 SAMPLE_CLK_OUT_REQ input pulses.

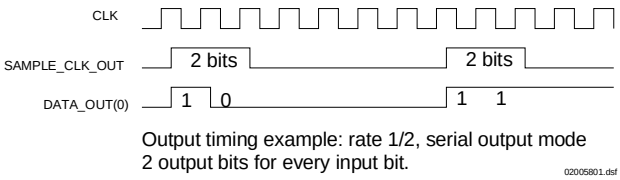
Timing

The I/O signals are synchronous with the rising edge of the reference clock CLK (i.e. all signals transitions always occur after the rising edge of the reference clock CLK). The maximum CLK frequency is 40 MHz.

Input

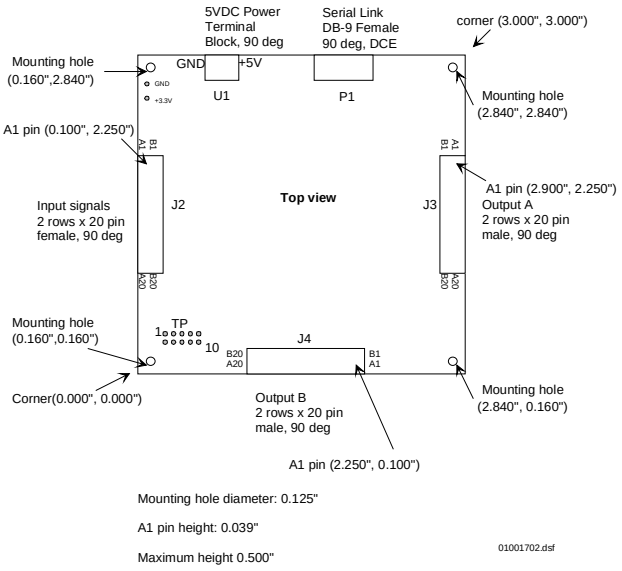


Output



Output samples can be bursty, depending on the FEC rate selected. The diagram above illustrates the output sampling clock for rate R = ½., serial output mode The next ComBlock module recognizes that multiple output bits are sent in each burst as it reads the output at the rising edge of CLK when SAMPLE_CLK_OUT = '1'.

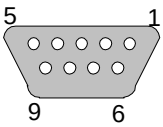
Mechanical Interface



Pinout

Serial Link P1

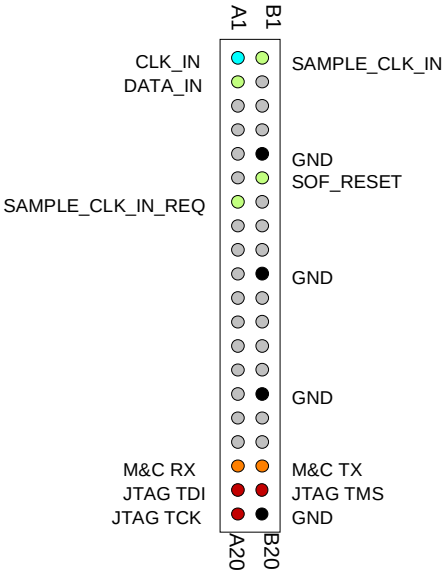
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



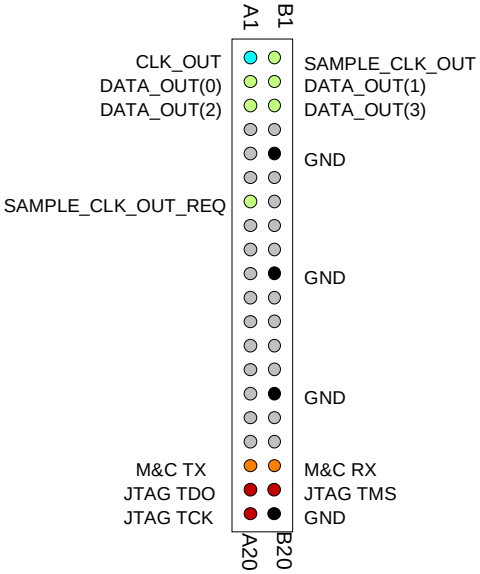
DB-9 Female

2 Transmit
3 Receive
5 Ground

Input Connector J2



Output Connectors J3, J4



I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-5003 TCP-IP / USB Gateway	COM-1002 BPSK/QPSK/OQPSK digital modulator
COM-1006 Reed-Solomon encoder	COM-1012/1019 DSSS digital modulator
	COM-1028 FSK/MSK/GFSK/GMSK digital modulator
	COM-1023 BER generator, Additive White Gaussian Noise Generator
	COM-1009 Viterbi decoder (back to back)

ComBlock Ordering Information

COM-1010 Convolutional Encoder

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