COM-1010 CONVOLUTIONAL ENCODER VHDL SOURCE CODE OVERVIEW

Overview

The COM-1010 ComBlock Module comprises two pieces of software:

- VHDL code to run within the FPGA for all signal processing functions
- C/Assembly code running within the Atmel AT90S8515 or ATMega8515L microprocessor for non application-specific monitoring and control functions.

The VHDL code interfaces to the monitoring and control functions by exchanging byte-wide registers on the Atmel microcontroller 8-bit data bus. The control and monitoring registers are defined in the specifications [1].

The COM-1010 VHDL code runs on the generic COM-1000 hardware platform. The schematics [2] for this platform are available in this CD.

Reference documents

[1] specifications: com1010.pdf

[2] hardware schematics: com_1000schematics.pdf

[3] VHDL source code in directory
com-1010_007\src

[4] Xilinx ISE project files
com-1010_007\com1010.npl

[5] .ucf constraint file
com-1010_007\src\com1010.ucf

[6] .mcs FPGA bit file
com-1010_007\com1010_007.mcs

Configuration Management

The current software revision is 7.

VHDL development environment

The VHDL software was developed using the Xilinx ISE 4.1 development environment. The synthesis tool is FPGA Express 3.6.

Target FPGA

The VHDL code was synthesized for the Xilinx Spartan-II XC2S200-5PQ208 FPGA.

Xilinx-specific code

The VHDL source code was written in generic VHDL with few Xilinx primitives. No Xilinx CORE is used. The Xilinx primitives are:

- BUFG
- IBUFG
- RAMB4_S1_S1

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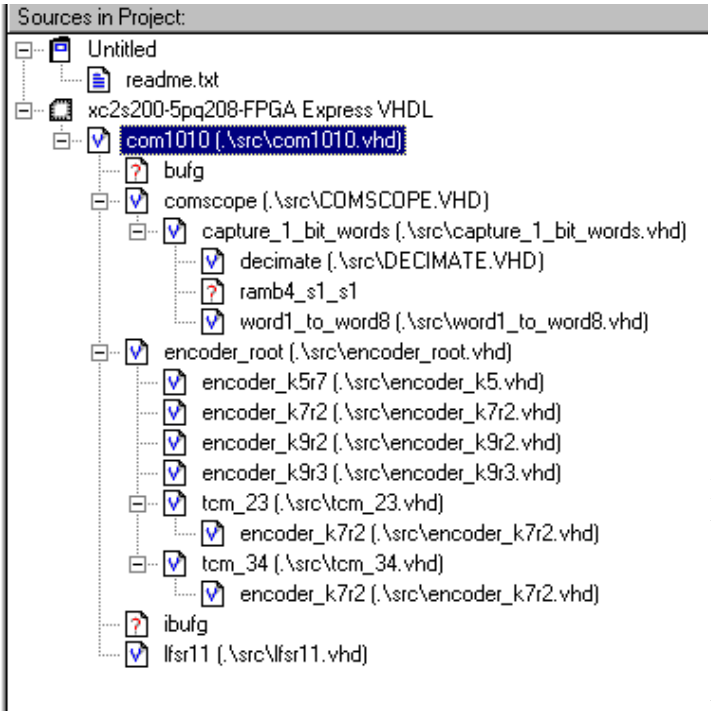
VHDL software hierarchy



The code is stored with one, and only one, entity per file as shown above.

The root program (highlighted) is *com1010.vhd.*

Clock / Timing

At any given time, the software uses one of two possible clocks:

- An external clock CLK_IN2.
- A 40 MHz internal clock CLK_IN1.

Selection of the internal versus external reference clock depends on the control register REG0 bit 0, under user control. The resulting selected clock is routed through global buffers. It serves as processing clock, output clock and input clock. The external clock should be selected in all cases, except when in test mode (the PRBS-11 pseudo-random sequence is generated internally, there is no external input).

The code is written to meet the timing requirements on the target FPGA at a speed of at least 40 MHz.

Architecture

The root component is *com1010.vhd*. It provides four key functions:

- Convolutional encoding in the *encoder_root.vhd* component.
- Global clock selection.
- Monitoring and control through the interface with the 8-bit Atmel microprocessor.
- Real-time data capture and display in the *comscope.vhd* component.

Monitoring and Control information is exchanged through 8-bit registers mapped on the 8-bit bus as follows:

- 4 control registers at microprocessor address 0 through 3
- 0 monitoring register.

A few registers are also reserved for special functions such as

- serial communication with the other comblocks on each of the four sides (REG254/REG255).
- VHDL code *REVISION* (REG253).
- VHDL code *OPTION* (REG252).
- ComScope (REG237-REG250)

The bus address and data are multiplexed over the same 8-bit data lines. The address is valid when the Address Latch Enable (*ALE*) signal is active high. Read and write cycles are identified by the *UC_RDN* and *UC_WRN* active-low signals respectively. Although the microprocessor is much slower than the FPGA, the Atmel uC timing can be difficult to meet, especially during write cycles because data is removed very shortly after the end of the write cycle when *UC_WRN* goes to '1'. Thus, it is wise to route the *UC_WRN* signal through a global buffer for best timing.

FPGA Occupancy

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Design Summary
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   Number of errors:      0
   Number of warnings:    5
   Number of Slices:                645 out of  2,352   27%
   Number of Slices containing
      unrelated logic:                0 out of    645    0%
   Number of Slice Flip Flops:      629 out of  4,704   13%
   Total Number 4 input LUTs:       907 out of  4,704   19%
      Number used as LUTs:                          815
      Number used as a route-thru:                   92
   Number of bonded IOBs:            46 out of    140   32%
      IOB Flip Flops:                               11
   Number of Block RAMs:              3 out of     14   21%
   Number of GCLKs:                   4 out of      4  100%
   Number of GCLKIOBs:                2 out of      4   50%
Total equivalent gate count for design:  60,734
Additional JTAG gate count for IOBs:  2,304
```

Contact Information

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