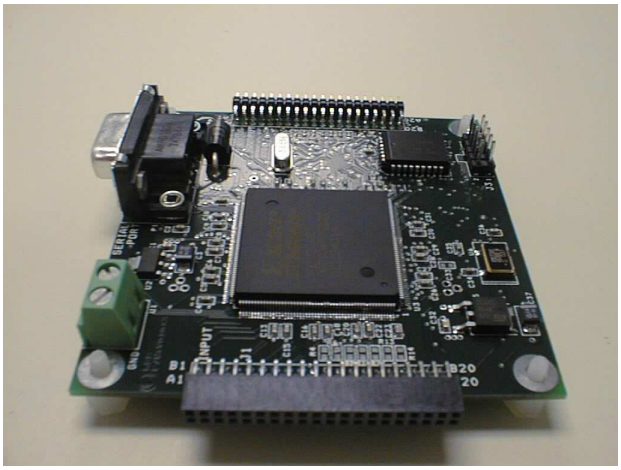
COM-1015 VITERBI ERROR CORRECTION DECODER K=9

Key Features

- Viterbi decoder for error correction.
- Constraint length K = 9.
  Selectable rate: 1/3 and 2/3.
- Performance:
  2.10^{-6} @ 4dB SNR R=1/3
  7.10^{-6} @ 5dB SNR R=2/3
- Continuous or block mode.
- Differential decoder.
- Maximum throughput (at output):
  1.48 Mbps.
- 4-bit soft-quantized or 1-bit hard decision input.
- Self synchronization.
- Coded BER measurement and lock status.
- Connectorized 3"x 3" module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right). Interfaces with 3.3V LVTTL logic..

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1015.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .



Electrical Interface

Input Module Interface	Definition
DATA_IN[3:0]	4-bit soft-quantized input bits (typically from a demodulator). Unsigned representation: 0000 for maximum amplitude '0', 1111 for maximum amplitude '1'. DATA_IN(3) represents the information bit When 1-bit hard decision is selected, the input is DATA_IN(3) only. Input pins DATA_IN(2:0) are ignored.
SAMPLE_CLK_IN	Input signal sampling clock. One CLK-wide pulse. Read the input signal at the rising edge of CLK when SAMPLE_CLK_IN = '1'.
SOF_IN	Optional start of frame reset input. Used only in block mode. Ignored in continuous mode. 1 CLK_IN-wide pulse. Aligned with SAMPLE_CLK_IN.
CLK_IN	Input reference clock for Inputs. Maximum speed is 40 MHz.

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Output Module Interface	Definition
DATA_OUT	Output data stream. 1-bit serial
SAMPLE_CLK_OUT	Output bit clock. One CLK_OUT-wide pulse. Read the output bit at the rising edge of CLK_OUT when SAMPLE_CLK_OUT = '1'.
LOCK STATUS	'1' when the Viterbi Decoder is in lock, '0' otherwise. See Lock Status. Available on both Input and Output connectors.
SOF_OUT	Start of frame output. When in block mode, this pulse marks the first decoded bit in the block. 1 CLK_OUT-wide pulse. Aligned with SAMPLE_CLK_OUT.
CLK_OUT	40 MHz output reference clock. (from internal oscillator).
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption is 300mA.

Important: I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration (via Serial Link / LAN)

Complete assemblies can monitored and controlled centrally over a single serial or LAN connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Parameters	Configuration
Rate R	0000 = (K=9, R=1/3) 0001 = (K = 9, R=2/3) In block mode, any change in the rate is effective at the next start of frame (SOF_RESET). In continuous mode, any change in the rate is effective immediately. REG0 bits 4-1
Differential Decoding	0 = disabled 1 = enabled REG0 bit 5
Continuous / Block mode	Determines whether the SOF_RESET mode should be enabled for resetting the decoder at the start of a block. 0 = continuous 1 = block mode. REG0 bit 6
Soft/Hard Decision Decoding	Determines whether 4 bits (soft decision) or 1 bit (hard decision) will be used to decode the data. 0 = Soft Decision 1 = Hard Decision REG0 bit 7
Bit Error Threshold	Determines the % of Bit Errors necessary to put the decoder out of lock. 001 = 6.25% 010 = 12.5% 011 = 25.0% 100 = 33.3% REG1 = bits 2-0

Configuration example

REG0 = 0x00
REG1 = 0x04
K=9 rate 1/3, no differential decoding, continuous mode, soft decision decoding. Bit Error Threshold set to 33.3%.

Baseline configurations can be found at www.comblock.com/tsbasic_settings.htm and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

Monitoring (via Serial Link / LAN)

Monitoring registers are read-only.

Parameters	Monitoring
Bit Errors	The number of bit errors detected on the *encoded* input bits. Errors are computed over a 3000 bit window and are updated every 3000 bits. REG2: error_count[7:0] LSB REG3 bits 2-0: error_count[10:8] MSB
Lock Status	0 = No Lock (Errors > User Defined Bit Error Threshold) 1 = Lock (Errors < User Defined Bit Error Threshold) See Lock Status REG4: bit 0.
Version	Returns '1015x' when prompted for version number.

Implementation

K = 9

The generator polynomials for K = 9 R = 1/3 is
$G_0(x) = 1 + x^2 + x^3 + x^5 + x^6 + x^7 + x^8$
$G_1(x) = 1 + x + x^3 + x^4 + x^7 + x^8$
$G_2(x) = 1 + x + x^2 + x^5 + x^8$

The generator polynomials for K = 9 R = 2/3 is
$G_0(x) = 1 + x + x^2 + x^3 + x^5 + x^7 + x^8$
$G_1(x) = 1 + x^2 + x^3 + x^4 + x^8$

The rate 2/3 decoder is configured for a rate ½ encoded data stream with the following puncturing pattern (1 denotes transmission, 0 blocking):

Rate	G_0	11
2/3	G_1	01

Synchronization

This Viterbi decoder implementation is self-synchronizing. The synchronization algorithm is described below.

The nature of the Viterbi algorithm requires that the input data bits occur in a certain order.

Example: For every giving input bit (B_{In}) the Rate 1/3 generator polynomials will give three output bits (B_{Out0}, B_{Out1}, B_{Out2}). For the Viterbi algorithm to decode properly, the bits must be received in the order B_{Out0}, B_{Out1}, B_{Out2}.

In addition, the decoder expects to *start* decoding at a certain position. This is determined by the first input bit. In the previous example, the Viterbi expects the first input bit to be B_{Out0}, followed by B_{Out1} and B_{Out2}. Generally in block mode this is always the case.

However, due to startup conditions, this not guaranteed in continuous mode. In the case of the example, the first input bit may be B_{Out2}, followed by B_{Out0} and B_{Out1} (Note the order is still maintained). Since the Viterbi expects the first input bit to be B_{Out0}, it will decode this received input series of

B_{Out2}, B_{Out0}, B_{Out1}

As

B_{Out0}, B_{Out1}, B_{Out2}

Thus, the decoded output will be incorrect, and the decoder is considered to be unsynchronized.

REG1 determines the threshold for resynchronization. In the case where REG1 is configured as "0x04," resynchronization will occur after > 33% bit errors are detected. The lock status signal will equal '0' and the decoder will shift the input bit's position.

For example, in the received input sequence,

B_{Out2}, B_{Out0}, B_{Out1}

The decoder will bypass the first bit and start instead at:

Bypassed B_{Out0}, B_{Out1},

The decoder will continue to shift until it is synchronized.

Lock Status & BER Measurement

The COM-1015 continuously measures the encoded bit error rate (i.e. input bit stream BER) over a 3000-bit window.

The (encoded) input data is saved in an input buffer. After decoding, the bits are re-encoded and compared with those stored in the input buffer. The resulting BER measurement is displayed in monitoring registers REG2/3.

The Viterbi decoder is considered locked when the measured BER is below the used-defined threshold in REG1. The Lock Status is '1' for lock and '0' for no lock.

The Lock Status is available as bit 7 in monitoring register REG2 and as a pin on each the input and output connectors.

The BER measurement and the lock status are updated every 3000 input bits.

Phase Ambiguity

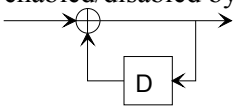
The COM-1015 does not correct for any phase ambiguity occurring in the demodulator upstream. It does, however, provide a means to detect such

phase ambiguity by using the lock status signal in conjunction with the user-defined BER threshold.

For example, phase ambiguities of n*90 degrees can exist for QPSK demodulators, resulting in bit error rates of 25% or 50%. In cases where a phase ambiguity exists, the Viterbi Decoder will never synchronize and the Lock Status will equal '0'. Since the Lock Status is available on the input, or 'upstream' connector, it can be used to provide this information to the demodulator.

Differential Decoding

Differential decoding can be used following FEC decoding as shown below. This feature can be enabled/disabled by software.



Bit Error Rate Performances

SNR	Theoretical BER	Rate 1/3 BER	Rate 2/3 BER
4.0 dB	0.0125	2e-6	4e-4
5.0 dB	0.0056	<10e-7	7e-6
6.0 dB	0.0023	<10e-8	

As is gleaned from the above table, improvements of 6dB occur for SNR > 4dB for the rate 1/3 decoder, and improvements of 4.5 dB occur for rate 2/3 at SNR > 4dB.

Data Rates

A significant rate change occurs within the decoder module. An illustration is provided below.

The maximum *output* data rates are as follows:

Rate 1/3: 1.48 Mbps
Rate 2/3: 1.48 Mbps

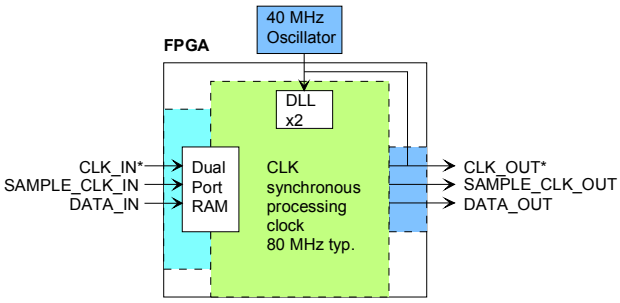
Thus the maximum *input* rates are:

Rate 1/3: 1.48 Mbps * 3 = 4.44 Mbps
Rate 2/3: 1.48 Mbps * 3/2 = 2.22 Mbps

Timing

Clocks

The clock distribution scheme embodied in the COM-1015 is illustrated below.



Baseline clock architecture
Green = 80 MHz processing zone
Light blue = user defined input clock
Darker blue = internal 40 MHz clock
**** indicates edge-trigger signal***

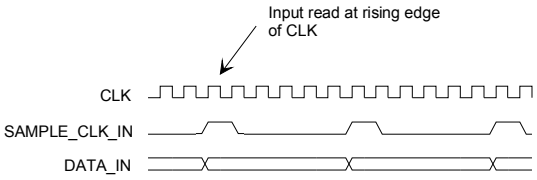
The core signal processing performed within the FPGA is synchronous with the 80 MHz processing clock locked onto a 40 MHz internal oscillator. The processing clock is not related to the CLK_IN clock.

A 512-sample dual-port RAM elastic buffer is used at the boundary between input and internal processing area. Thus, the input clock frequency can be independent from the internal processing clock frequency.

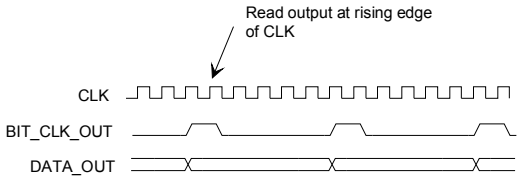
The input signals at the J1 connector are synchronous with the CLK_IN clock at J1/A1. This clock can be up to 40 MHz.

The output signals are synchronous with the rising edge of the 40 MHz reference clock CLK_OUT (i.e. all signals are stable at the rising edge of the reference clock CLK_OUT).

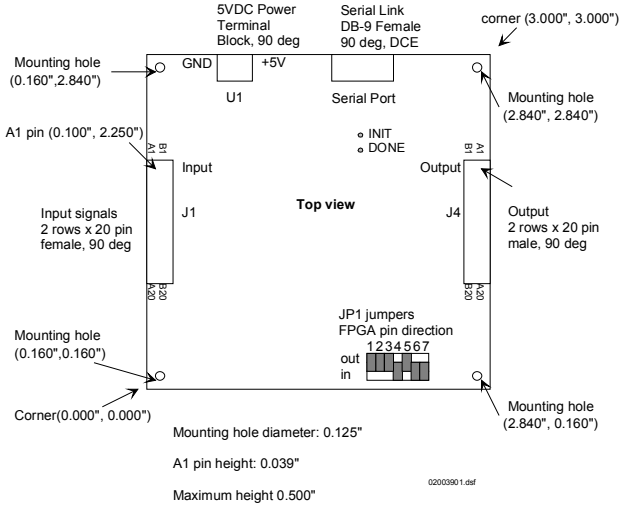
Input



Output



Mechanical Interface

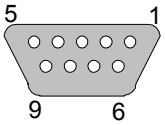


Note: The location of the seven JP1 jumpers is irrelevant.

Pinout

Serial Link P1

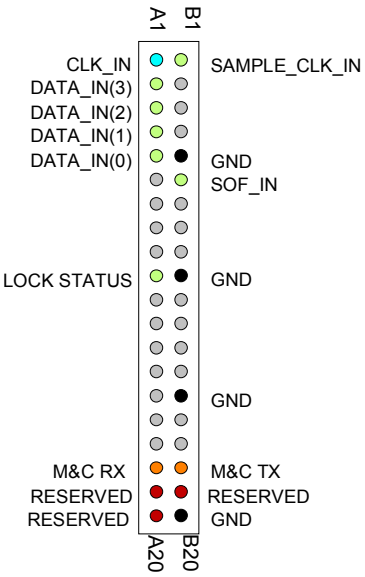
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



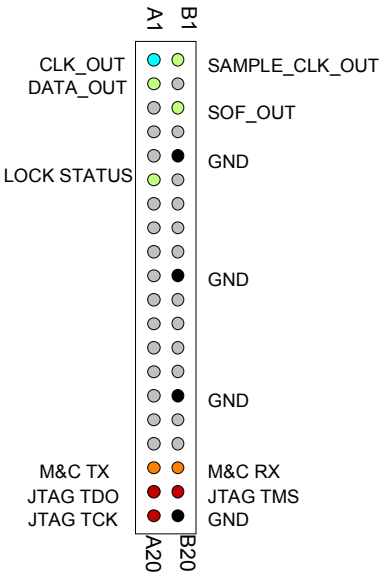
DB-9 Female

2 Transmit
3 Receive
5 Ground

Input Connector J1



Output Connectors J4



I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-1010 Convolutional encoder, K=9,7,5	COM-1005 Bit Error Rate measurement
COM-1027 FSK demodulator, up to 10 Msymbols/s.	
COM-1202 PSK/QAM/APSK modem	

This module is not compatible with the COM-1001, COM-1011, COM-1018, COM-1418 demodulators because demodulation phase ambiguities, although detected here, cannot be corrected at the demodulators.

ComBlock Ordering Information

COM-1015 Convolutional Decoder, K = 9

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