



COM-1015 VITERBI ERROR CORRECTION DECODER K=9 VHDL SOURCE CODE OVERVIEW

Overview

The COM-1015 ComBlock Module comprises two pieces of software:

- VHDL code to run within the FPGA for all signal processing functions
- C/Assembly code running within the Atmel AT90S8515 or ATMega8515L microprocessor for non application-specific monitoring and control functions.

The VHDL code interfaces to the monitoring and control functions by exchanging byte-wide registers on the Atmel microcontroller 8-bit data bus. The control and monitoring registers are defined in the specifications [1].

The COM-1015 VHDL code runs on the generic COM-8000 hardware platform. The schematics [2] for this platform are available in this CD.

Reference documents

[1] specifications: com1015.pdf

[2] hardware schematics: com_8000schematics.pdf

[3] VHDL source code in directory
com-1015_008\src

[4] .ucf constraint file
com-1015_008\src\com1015.ucf

[5] .mcs FPGA bit file
com-1015_008\com1015_008.mcs

Configuration Management

The current software revision is 8.

VHDL development environment

The VHDL software was developed using the Xilinx ISE 4.1 development environment. The synthesis tool is FPGA Express 3.6.

Target FPGA

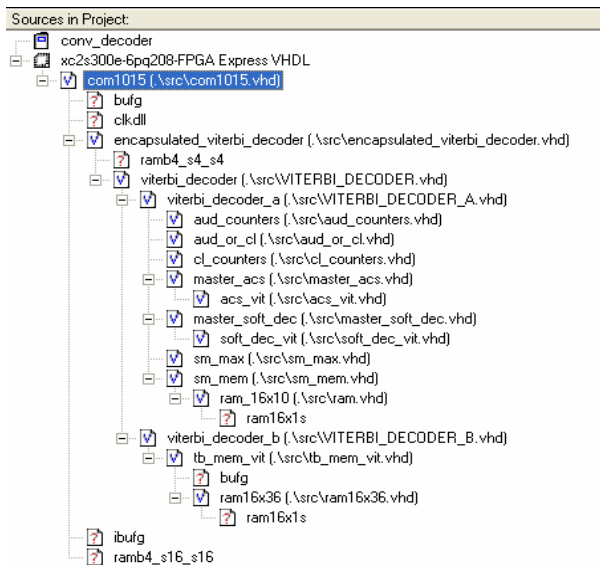
The VHDL code was synthesized for the Xilinx Spartan-IIe XC2S300E-6PQ208 FPGA.

Xilinx-specific code

The VHDL source code was written in generic VHDL with few Xilinx primitives. No Xilinx CORE is used. The Xilinx primitives are:

- BUFG
- IBUFG
- CLKDLL (x2)
- RAMB4_S1_S1
- RAMB4_S16_S16

VHDL software hierarchy



The code is stored with one, and only one, entity per file as shown above.

Clock / Timing

The software uses a single master clock (CLK_IN2) which serves as input clock, output clock and reference for the double-frequency processing clock. The code is written to meet the timing requirements on the target FPGA at a speed of at least 80 MHz (40 MHz maximum frequency for CLK_IN2).

Contact Information

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