COM-1016 BIT INTERLEAVER / DEINTERLEAVER

Key Features

- Interleaves any digital signal with an n*8-bit frame size.
  8 branches, 1024 depth increment.
  Total delay: 57,344 bits.
- Unique word insertion / detection for synchronization.
- Maximum throughput: 20 Mbps.
- Can be used as interleaver or deinterleaver.
- Single 5V supply
- Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom). Interfaces with 5V and 3.3V logic.

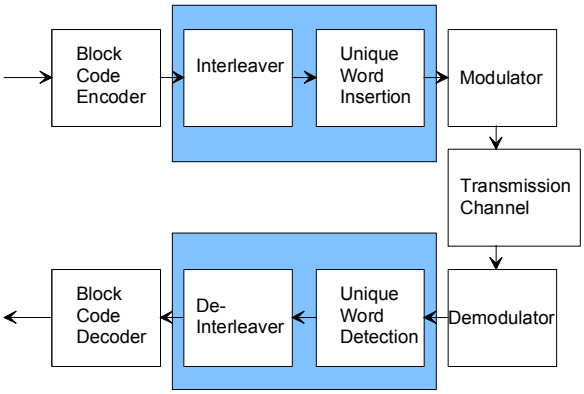
For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1016.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

Application

Bit interleaving is often used in conjunction with error correction block codes to spread bursts of errors over several blocks so that the maximum number of errors in each block stays within the number of correctable errors.

The bit de-interleaver used at the receiver needs to be synchronized with the bit interleaver at the transmitter. The conventional synchronization technique is to insert a periodic unique sequence (unique word) after interleaving. This unique word is detected at the receiver to recover the start of frame synchronization. The unique word is not subjected to interleaving.



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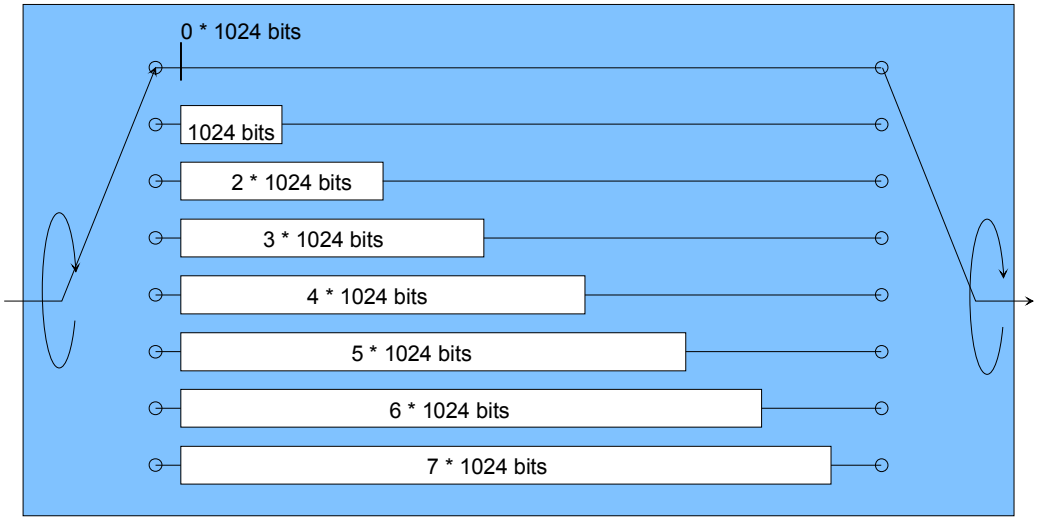
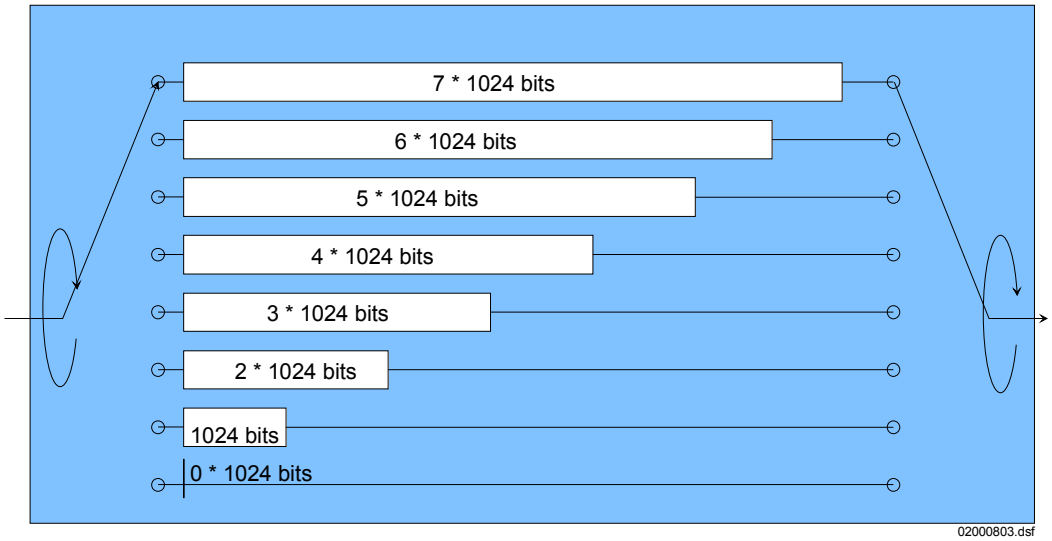
Block Diagram



Interleaver (COM-1016-A)



De-interleaver (COM-1016-B)

Electrical Interface

Input Module Interface	Definition
DATA_IN	1-bit serial data. Read at rising edge of CLK when SAMPLE_CLK_IN = '1'
SAMPLE_CLK_IN	Input signal sampling clock. One CLK-wide pulse. Read the input signal at the rising edge of CLK when SAMPLE_CLK_IN = '1'.
SOF_IN	Start of frame pulse. Input. One CLK wide pulse. Aligned with SAMPLE_CLK_IN. Input is required for synchronization purposes when the internal unique word insertion / detection feature is disabled.
SAMPLE_CLK_REQ_OUT	Output. Flow control signal requesting samples from the module upstream. Typically used in transmitters where data is pulled as needed from the end module (modulator).
CLK_IN	Input reference clock for synchronous I/O and processing. Yields internal CLK clock. Typically 40 MHz.
Output Module Interface	**Definition**
DATA_OUT	Output data stream. 1-bit serial
SAMPLE_CLK_OUT	Output symbol clock. One CLK-wide pulse. Read the output signals at the rising edge of CLK when SAMPLE_CLK_OUT = '1'.
SOF_OUT	Start of frame pulse. Output. One CLK wide pulse. Aligned with the first data bit in a frame (excluding any unique word preceding the first data bit).
SAMPLE_CLK_REQ_IN	Input. Flow control signal requesting samples from this module. Typically used in transmitters where data is pulled as needed from the end module (modulator).
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 200mA.

Configuration (via Serial Link / LAN)

Complete assemblies can be monitored and controlled centrally over a single serial or LAN connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

Parameters	Configuration
Internal / External clock selection	0 = internal clock 1 = external clock REG0 bit 0
Unique word insertion / detection	0 = disabled. 1 = enabled. When the unique word synchronization feature is disabled, a start of frame SOF_IN pulse must be provided at the input. When unique word detection is enabled, the unique word is removed from the data stream after detection. REG0 bit 1
Interleaving / Deinterleaving Enable	0 = disabled (bypassed) 1= enabled REG0 bits 2
Internal pattern generation (test mode for interleaver only)	An internally generated test signal can be inserted at the interleaver input for test purposes. 00 = test mode disabled 01 = counting sequence: When set, the external input is disabled and a periodic pattern is internally generated at the interleaver input. The pattern consists of an 8-bit counter, MSB transmitted first. 10 = internal generation of 2047-bit periodic pseudo-random bit sequence as input. (overrides external input bit stream). This pattern can be used for bit error rate measurement as it is recognized

	at the receiving end by the COM-1005 BER measurement module. 11 = force inputs to all zeros. The test pattern bit rate is automatically set by the external sink module (typically a modulator) as part of the flow control mechanism. REG0 bits 5-4
Frame size in bits	Total number of bits in a frame, excluding the 32 bit unique word. Range 8 – 4096. Must be an integer multiple of 8. REG1: LSB REG2: MSB

Monitoring (via Serial Link / LAN)

Monitoring registers are read-only.

Parameters	Monitoring
Bit error rate	When the transmission of periodic unique words is enabled, the deinterleaver can count the number of bit errors over 32 unique wors = 1024 received bits. This BER measurement method works even while transmitting regular payload data (no need to switch the transmitter to the PRBS-11 test mode). SREG0 bits 7-0 (LSB). SREG1(1:0): bits 9-8 (MSbs).

Operation

Unique Word

A unique word is used for synchronizing the deinterleaver (within the receiver) with the interleaver (within the transmitter). The data is inserted in periodic frames with fixed length, as defined by the user through registers REG1/2/3. The start of frame is marked by a 32-bit unique word at the start of each frame:
01011010 00001111 10111110 01100110 (binary)
0x 5A 0F BE 66 (hex)
The most significant bit (left-most) is transmitted first.

The bandwidth expansion can be kept to a small relative value (say less than 1%) by selecting a large frame size (say 4096 bits).

The unique word is not interleaved.

The unique word transmission or reception can be disabled by software command. This can be useful in configurations where frame synchronization references are available externally.

If unique word synchronization is enabled, the 32-bit unique word is removed from the received data stream prior to de-interleaving.

Software Version

The interleaving and de-interleaving functions are installed as separate software versions, as each consumes a significant portion of the FPGA resources.

All versions can be downloaded from www.comblock.com/download.

COM-1016-**A** Bit interleaver

COM-1016-**B** Bit de-interleaver

Test Configuration Examples

COM-1016-A interleaver -> COM-1016-B deinterleaver -> COM-1005 BER measurement.
The interleaver generates a PRBS-11 pseudo random test pattern, interleaves it. After deinterleaving, the COM-1005 confirms the absence of bit errors.

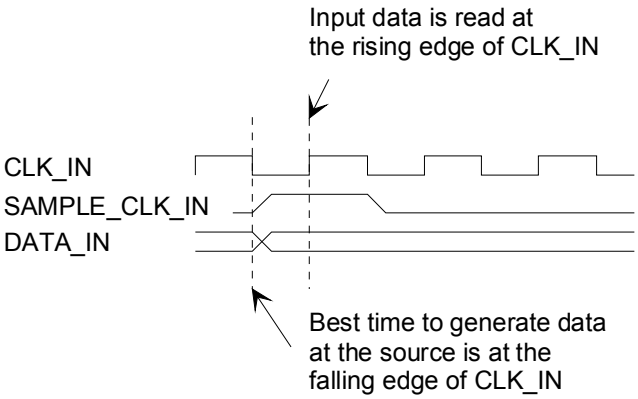
Registers configuration:
Interleaving/de-interleaving on, frame size 4096 bits, 32-bit unique word insertion prior to each frame, PRBS-11 test pattern, BER measured over 1 Mbits.
COM-1016-A: 26 00 10
COM-1016-B: 07 00 10
COM-1005: 0C

From the ComBlock control center, verify that the monitoring registers for COM-1005 show no bit error (registers 1/2/3 are all null) while register 5 shows lock (bit 0 = ‘1’).

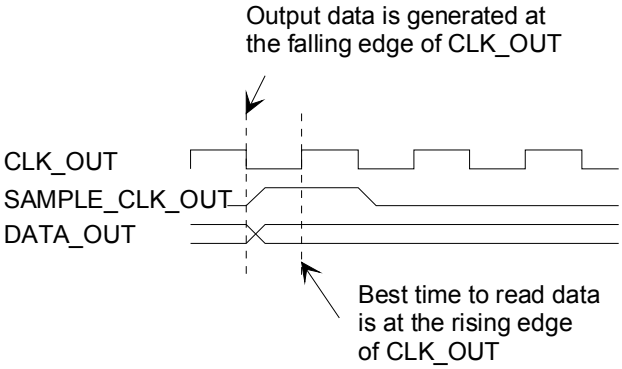
Timing

The I/O signals are synchronous with the rising edge of the reference clock CLK (i.e. all signals transitions always occur after the rising edge of the reference clock CLK). The maximum CLK frequency is 40 MHz.

Input



Output



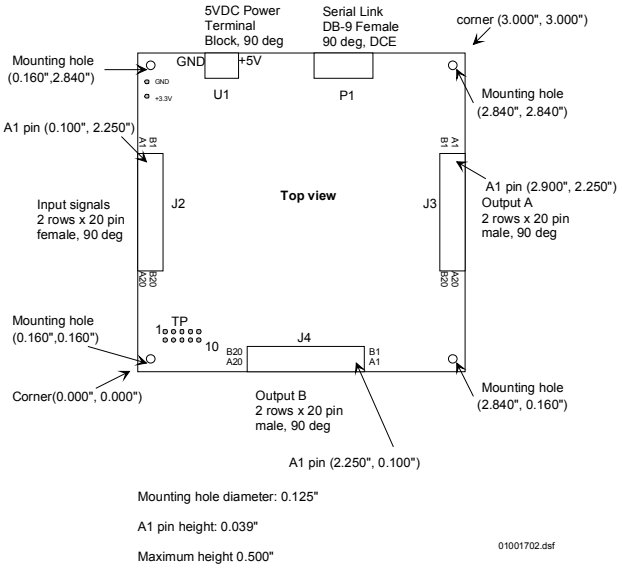
Test Points

Test points are provided for easy access by an oscilloscope probe. Test points are different for the interleaver (**-A**) and the deinterleaver (**-B**) versions:

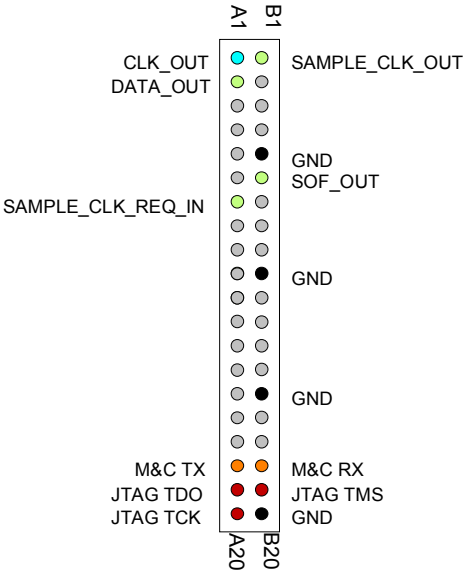
Interleaver Test Points	Definition
TP1	Start of frame at interleaver input.
TP2	Data stream at interleaver input
TP3	Bit clock at interleaver input.
TP4	Unique word enable at interleaver output
TP5	Start of frame at interleaver output
TP6	Data stream at interleaver output
TP7	Bit clock at interleaver output
TP8	Start of LFRS-11 internal test pattern

De-interleaver Test Points	Definition
TP1	Unique word detection pulses at the receiver
TP2	Start of frame synchronization lock status at the receiver. '1' when locked.
TP3	Start of frame at de-interleaver input
TP4	Data at de-interleaver input
TP5	Bit clock at de-interleaver input
TP6	Data enable (low during unique word)
TP7	Start of frame at de-interleaver output
TP8	Data at de-interleaver output
TP9	Bit clock at de-interleaver output
TP10	Zero bit errors out of 1024 sync bits.

Mechanical Interface



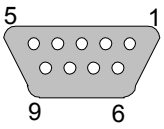
Output Connectors J3, J4



Pinout

Serial Link P1

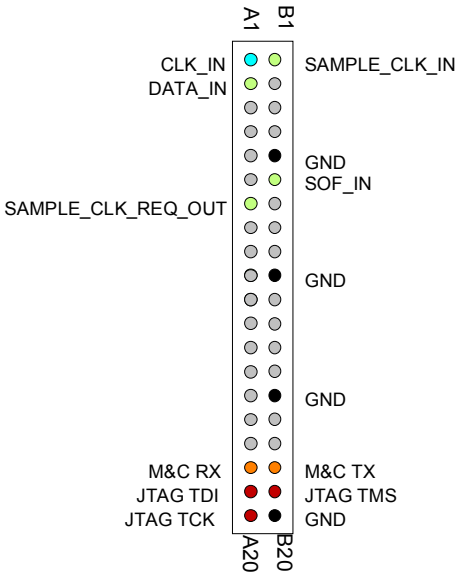
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



DB-9 Female

2 Transmit
3 Receive
5 Ground

Input Connector J2



I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-1009 Viterbi decoder	COM-1010 Convolutional encoder
COM-7002 Turbo Code Encoder	COM-7002 Turbo Code Decoder
COM-1202 PSK/QAM/APSK demodulator	COM-1402 PSK/QAM/APSK modulator
COM-1418 DSSS demodulator	COM-1019 DSSS modulator
COM-1027 FSK/MSK/GFSK/GMSK demodulator	COM-1028 DSSS FSK/MSK/GFSK/GMSK modulator
COM-5003 TCP-IP / USB Gateway	

Configuration Management

This specification is to be used in conjunction with VHDL software revision 5.

ComBlock Ordering Information

COM-1016 Bit Interleaver / Deinterleaver.

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