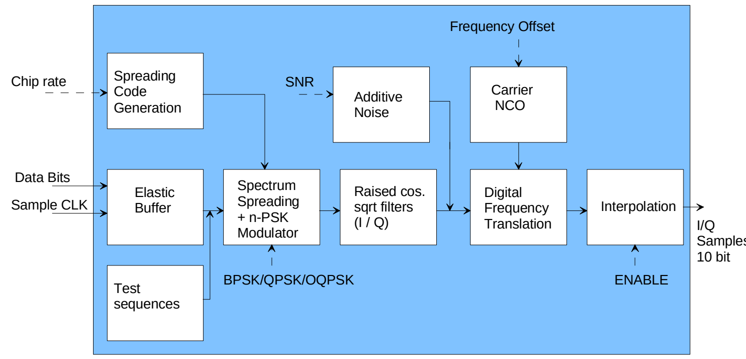
COM-1019 DIRECT-SEQUENCE SPREAD-SPECTRUM MODULATOR 20 Mchip/s

Key Features

- Direct sequence spread-spectrum (DS-SS) modulator.
- Programmable chip rates up to 20 Mchip/s.
- Spreading codes:
  - Gold sequences (up to 2^{23}-1 chips).
  - Maximal length sequences, (max length 2^{23}-1 chips).
  - Barker codes (length 11, 13).
  - GPS C/A codes.
- code modulation: BPSK/QPSK/OQPSK with output spectral shaping filter: raised cosine square root filter with 20%, 25%, 35% or 40% rolloff. Filter can be bypassed.
- Internal generation of pseudo-random bit stream and unmodulated carrier for test purposes.
- Built-in channel impairments generation:
  - additive white Gaussian noise
  - frequency offset (Doppler)
- Connectorized 3"x 3" module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right). Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.

Block Diagram

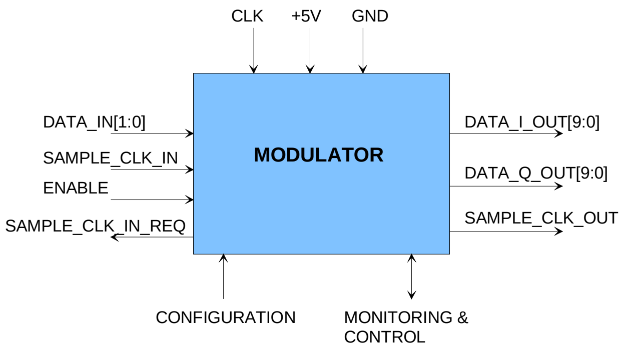


For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1019.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

Electrical Interface

Modulator Inputs / Outputs



Two basic types of input connections are available for user selection:

- direct connection between data source and modulator.
- single data source to multiple modulators over a shared bus.

Input Module Interface Direct connection between two ComBlocks, REG19(4) = '0'	**Definition**
CLK_IN	Synchronous clock reference for the input interface. All input signals (DATA_IN, SAMPLE_CLK_IN, ENABLE) are read at the rising edge of CLK_IN. Recommended maximum frequency: 40 MHz. LVTTL 0 – 3.3V
DATA_IN[1:0]	Input data stream. In 1-bit serial mode, use DATA_IN[0] only. In 2-bit parallel mode, DATA_IN[0] is the I data bit DATA_IN[1] is the Q data bit The Q data bit is ignored in BPSK mode. LVTTL 0 – 3.3V
SAMPLE_CLK_IN	Input sample clock. One CLK_IN-wide pulse. Read the input signals at the rising edge of CLK_IN when SAMPLE_CLK_IN = '1'. LVTTL 0 – 3.3V
ENABLE	Modulator enable input. Internally pulled high. Qualifies the SAMPLE_CLK_IN. Used for burst-mode transmission. In continuous mode, keep at '1'. LVTTL 0 – 3.3V
SAMPLE_CLK_IN_REQ	Output. Requests a sample from the module upstream. For flow-control purposes.

Input Module Interface Bus connection, REG19(4) = '1'	**Definition**
BUS_CLK_IN	40 MHz input reference clock for use on the synchronous bus.
BUS_ADDR[3:0]	Bus address. Input (since this module is a bus slave). Designates which slave module is targeted for this read or write transaction. All 1's indicates that the write data is to be broadcasted to all receiving slave modules. Read at the rising edge of BUS_CLK_IN
BUS_RWN	Read/Write#. Input (since this module is a bus slave). Indicates whether a read (1) or write (0) transaction is conducted. Read at the rising edge of BUS_CLK_IN. Read and Write refer to the bus master's perspective.
BUS_DATA[15:0]	Bi-directional data bus. Input when BUS_RWN='0'. Output when BUS_RWN='1'. Read data latency is 2 clock periods after the read command. Functional definition during write: • bit 0 SAMPLE_CLK_IN. '1' when DATA_IN is available • bit 1 DATA_IN data stream to modulator. • bits(15:2) undefined Functional definition during read: • bit 0 SAMPLE_CLK_IN_REQ requests data from the source. Used for flow control. • bits(15:1) undefined

Two basic types of output connections are available for user selection:

- connection to dual 10-bit DACs, parallel I and Q samples, output sampling clock.
- connection to dual 14-bit DACs, multiplexed I and Q samples, input sampling clock.

Output Module Interface. Parallel 10-bit I & Q samples. REG19(0) ='0'	**Definition**
CLK_OUT	40 MHz synchronous clock reference for the output interface. The output signals DATA_I_OUT, DATA_Q_OUT, SAMPLE_CLK_OUT change immediately after the rising edge of CLK_OUT. Recommended maximum frequency: 40 MHz.
DATA_I_OUT[9:0]	Modulated output signal, real axis. 10-bit precision. Format: 2's complement or unsigned, selected by configuration bit 1.
DATA_Q_OUT[9:0]	Modulated output signal, imaginary axis. 10-bit precision. Same format as DATA_I_OUT.
SAMPLE_CLK_OUT	Output signal sampling clock. Read the output signal at the rising edge of CLK_OUT when SAMPLE_CLK_OUT = '1'. Sampling rate is either 4 x symbol rate or fclk (interpolation off/on configuration bit 7). SAMPLE_CLK_OUT can stay high when output samples are transmitted in successive CLK_OUT periods.
DAC_CLK_OUT	Output sampling clock for Digital to Analog Converters. DAC reads the output sample at the rising edge.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the sampling frequency f_{sample_clk} . The maximum power consumption at 80 MHz is 600mA.

Important: I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- Asynchronous serial (DB9)

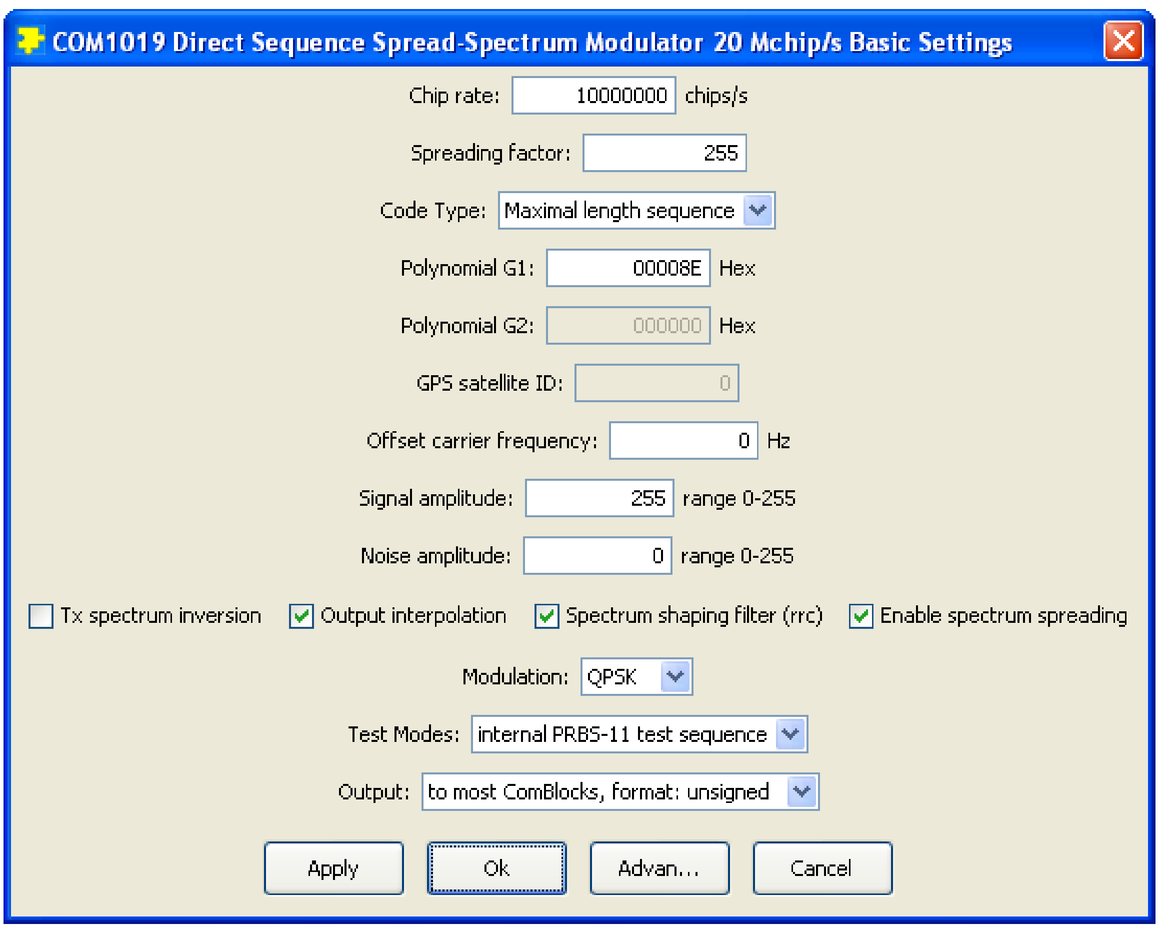
or connections via adjacent ComBlocks:

- USB
- TCP-IP/LAN,
- Asynchronous serial (DB9)
- PC Card (CardBus, PCMCIA).

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1019 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1019 module to be configured, next click the *Settings* button to display the *Settings* window shown below.



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center "Advanced" configuration or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Definitions for the Control registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

This module operates at an internal processing clock rate **f_{clk}** of 80 MHz.

Most processing is done at the sampling rate / **f_{sample_clk}** = 4 * chip rate.

In the definition below, a few control register bits may be undefined to maintain backward compatibility with previous versions. They can be ignored by the user when using the latest firmware release.

Parameters	Configuration
Chip rate	24-bit signed integer (2's complement) expressed as fchip rate * 2^{24} / **f_{clk}**. The maximum chip rate is **f_{clk}** /4 (20 Mchips/s). However, in practice it is recommended to limit the maximum chip rate to 0.99*(**f_{clk}**/4) to account for possible clock drifts between modulator and demodulator. REG0 = bits 7-0 REG1 = bits 15 – 8 REG2 = bits 23 – 16
Spreading factor (Processing gain)	Spreading code period Range: 3 – 2^{23}-1 • When using Gold codes or maximal length sequences, it is important that this field be consistent with the G1 and G2 generator polynomials below. Length is always in the form 2^n-1, where n is an integer. • When using Barker codes, the spreading factor must be either 11 (0x0B) or 13 (0x0D). • Truncated codes can be generated by selecting a spreading factor other than the code length. Please note that, even though generating very long codes is possible, their use may be impractible because of unacceptably long acquisition time at the demodulator. Recommended spreading factor: 3 to 2047. REG3 bits 7-0 (LSB) REG4 bits 7-0 REG5 bits 7-0 (MSB)
Code selection	001 = Gold code 010 = Maximal length sequence 011 = Barker code 100 = GPS C/A code REG6 bits 2-0
Gold sequence / Maximal Length Sequence generator polynomial G1	24-bit. Describes the taps in the linear feedback shift register 1: Bit 0 is the leftmost tap (2^0 in the polynomial). The largest non-zero bit is the polynomial order n. n determines the code period 2^n –1. Example: $G1 = 1 + x + x^4 + x^5 + x^6$ is represented as 0x000039 This field is used only if Gold code or Maximal length sequences are selected. REG7 = bits 7 – 0 REG8 = bits 15 – 8 REG9 = bits 23 – 16
Gold code generator polynomial G2	24-bit. Describes the taps in the linear feedback shift register 2: Same format as G1 above. This field is used only if Gold codes are selected. REG10 = bits 7 – 0 REG11 = bits 15 – 8 REG12 = bits 23 - 16
GPS satellite ID	GPS signals from different satellites are designated by a PRN signal number in the range 1 – 37. This field is used only if GPS C/A codes are selected. REG10 = bits 5 – 0

Offset carrier frequency f_c	24-bit signed integer (2's complement) expressed as $f_c * 2^{24} / f_{sample\_clk}$. REG13 = bits 7 – 0 REG14 = bits 15 – 8 REG15 = bits 23 - 16
Signal gain	Signal level. 8-bit unsigned integer. Maximum level 255, Minimum level 0. When the maximal level (255) is selected, the peak-to-peak dynamic range is +/- 371 out of a +/-512 (10-bit) range and the standard deviation is 249. REG16 = bits 7-0
Noise gain	Additive white Gaussian noise level. 8-bit unsigned integer. Maximum level 255, Minimum level 0. The noise samples standard deviation is 111 for a maximum noise gain setting of 255. (The noise bandwidth is +/- 2* symbol rate). REG17 = bits 7-0
Internal / External reference clock selection	This control bit selects the reference clock source. ■ Reference clock selection must be 'internal' when this module is the first in the transmission chain and when using the internally generated test sequences (see Test mode below). ■ Reference clock selection must also be 'internal' when user-supplied input data is synchronous with a CLK_IN clock frequency other than the recommended 40 MHz. ■ External reference clock should be used for applications whereby multiple modulators must be exactly synchronized (for example in the case of signal diversity combining applications). 0 = internal clock 1 = external clock REG18 bit 0
Output sample format	0 = 2's complement 1 = unsigned REG18 bit 1
Modulation	00 = BPSK 01 = QPSK 10 = OQPSK With BPSK, one data bit is transmitted every code period. With QPSK, two data bits (one symbol) are transmitted every code period. The code spectrum-spreading occurs after QPSK modulation of the data symbols. REG18 bits 3 – 2

Test mode	00 = disabled 01 = internal generation of 2047-bit periodic pseudo-random bit sequence as modulator input. (overrides external input bit stream). 10 = unmodulated carrier. (overrides external input bit stream) REG18 bits 5 – 4
Spectrum inversion	Invert Q bit. 0 = off 1 = on REG18 bit 6
Interpolation	Interpolation to maximum clock rate. 0 = off 1 = on REG18 bit 7
Output data flow	0 = output data is pushed to the next module (for example to COM-2001, or COM-1011/18) 1 = output data is pulled by next module (for example by the COM-4004) REG19 bit 0
Input format	0 = 1-bit serial 1 = 2-bit parallel (see also input bus enable bit below). REG19 bit 1
Ouput spectrum shaping filter enabled	Enables/Disables raised cosine square root output spectrum shaping filter. 0 = disabled 1 = enabled REG19 bit 2
Spreading	Enable/Disable spectrum spreading. 0 = disabled 1 = enabled REG19 bit 3
Input bus enabled	Controls whether the input connection is point-to-point or point-to-multipoint over a data bus (via a COM-9004 demultiplexing connector for example). The J1 input connector pinout is affected by this control bit. 0 = direct connection. Point to point. 1 = input data bus enabled. REG19 bit 4
Bus address	Unique 4-bit address identifying this module on the input bus (if the input bus is enabled in REG19 bit 4). Ignore otherwise. This module acts as bus slave: it performs the read/write transaction requested by the bus master if and only if the bus address matches its own address defined here. This address must be unique among modules connected to the same bus in order to avoid conflicts. REG20 bits 3-0

Writing or re-writing to the last register (REG20) resets the output interface. When interfacing with the COM-4004 70 MHz modulator, any configuration change in the COM-4004 should be followed by an interface reset.

Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
J1connector pin B7	Chip rate
J1 connector pin B8	Bit rate
J1 connector pin B9	PN code
J1 connector pin A9	PRBS-11 (test sequence) start of sequence.
TP1	FPGA DONE pin. High indicates proper download of the FPGA configuration file.

Operation

Spreading codes

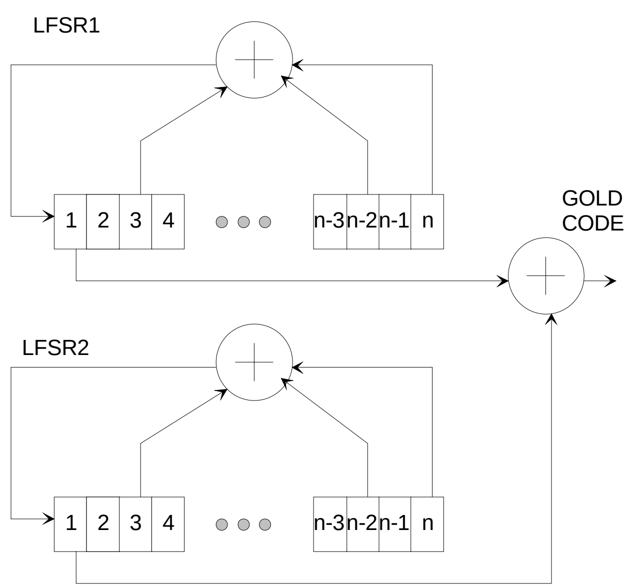
Spreading codes are pseudo random sequences which falls within the following categories:

- Gold sequences, for best autocorrelation properties
- Maximal length sequences
- Barker codes (length 11, 13)
- GPS C/A codes.

The same spreading code is used on both the in-phase (I) and quadrature (Q) channels.

Gold sequences

Gold sequences are generated using two linear feedback shift registers LFSR1 and LFSR2 as illustrated below:



The code period is 2^n-1, where n is the number of taps in the shift register. The LFRSa are initialized to all 1's at the start of each period. The LFRSs will generate all possible n-bit combinations, except the all zeros combination.

Each sequence is uniquely described by its two generator polynominals. The highest order is n. The generator polynominals are user programmable.

A few commonly used Gold sequences are listed below:

n = 5 (length 31):
$G1 = 1 + x^2 + x^5$ (0x000012)
$G2 = 1 + x + x^2 + x^4 + x^5$ (0x00001B)

n = 6 (length 63):
$G1 = 1 + x^5 + x^6$ (0x000030)
$G2 = 1 + x + x^4 + x^5 + x^6$ (0x000039)

n = 7 (length 127):
$G1 = 1 + x^3 + x^7$ (0x000044)
$G2 = 1 + x + x^2 + x^3 + x^4 + x^5 + x^7$ (0x00005F)

n = 9 (length 511):
$G1 = 1 + x^5 + x^9$ (0x000110)
$G2 = 1 + x^3 + x^5 + x^6 + x^9$ (0x000134)

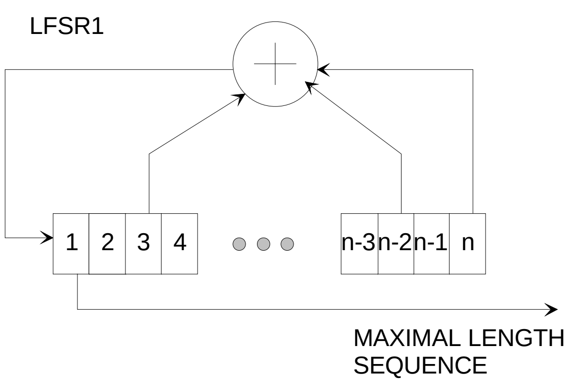
n = 10 (length 1023):
$G1 = 1 + x^7 + x^{10}$ (0x000240)
$G2 = 1 + x^2 + x^7 + x^8 + x^{10}$ (0x0002C2)

n = 11 (length 2047):
$G1 = 1 + x^9 + x^{11}$ (0x000500)
$G2 = 1 + x^3 + x^6 + x^9 + x^{11}$ (0x000524)

n = 17 (length 131071):
$G1 = 1 + x^3 + x^6 + x^7 + x^9 + x^{10} + x^{14} + x^{16} + x^{17}$ (0x01A364)
$G2 = 1 + x^9 + x^{13} + x^{14} + x^{17}$ (0x013100)

Maximal length sequences

Maximal length sequences are generated using one linear feedback shift register LFSR1 as shown below:



The code period is 2^n-1, where n is the number of taps in the shift register. The LFRSa are initialized to all 1's at the start of each period. The LFRSs will generate all possible n-bit combinations, except the all zeros combination.

Each sequence is uniquely described by its generator polynominal. The highest order is n. The generator polynominal is user programmable.

A few commonly used maximal length sequences are listed below:

n = 4 (length 15):
$G1 = 1 + x + x^4$ (0x000009)
n = 5 (length 31):
$G1 = 1 + x^2 + x^5$ (0x000012)
n = 6 (length 63):
$G1 = 1 + x + x^6$ (0x000021)
n = 7 (length 127):
$G1 = 1 + x + x^7$ (0x000041)
n = 8 (length 255):
$G1 = 1 + x^2 + x^3 + x^4 + x^8$ (0x00008E)
n = 9 (length 511):
$G1 = 1 + x^4 + x^9$ (0x000108)
n = 10 (length 1023):
$G1 = 1 + x^3 + x^{10}$ (0x000204)

Barker Codes

11 bit Barker code: 101 1011 1000, or 0x5B8
13 bit Barker code: 1 1111 0011 0101, or 0x1F35

The length (11 or 13) must be entered as spreading factor in REG3/4/5.

GPS C/A Codes

GPS C/A codes are modified Gold codes of length 1023 with generator polynomials:
$G1 = 1 + x^3 + x^{10}$
$G2 = 1 + x^2 + x^3 + x^6 + x^8 + x^9 + x^{10}$

The G2 generator output is slightly modified so as to create a distinct code for each satellite. The G2 output is generated by summing two specific taps of the shift register. In the case of Satellite ID 1 for example, taps 2 and 6 are summed.

The G2 output taps are listed below:

Satellite ID / GPS PRN Signal Number	G2 output taps selection	Satellite ID / GPS PRN Signal Number	G2 output taps selection
1	2 xor 6	21	5 xor 8
2	3 xor 7	22	6 xor 9
3	4 xor 8	23	1 xor 3
4	5 xor 9	24	4 xor 6

5	1 xor 9	25	5 xor 7
6	2 xor 10	26	6 xor 8
7	1 xor 8	27	7 xor 9
8	2 xor 9	28	8 xor 10
9	3 xor 10	29	1 xor 6
10	2 xor 3	30	2 xor 7
11	3 xor 4	31	3 xor 8
12	5 xor 6	32	4 xor 9
13	6 xor 7	33	5 xor 10
14	7 xor 8	34	4 xor 10
15	8 xor 9	35	1 xor 7
16	9 xor 10	36	2 xor 8
17	1 xor 4	37	4 xor 10
18	2 xor 5		
19	3 xor 6		
20	4 xor 7		

Compliant with "Navstar GPS Space Segment / Navigation User Interfaces" specifications, ICD-GPS-200, Revision C. IRN-200C-004, 12 April 2000.

Data Rate

The data rate is determined by the chip rate, the processing gain (i.e. the spreading code period) and the modulation (BPSK/QPSK).
For a QPSK modulated signal, the data rate is
2 *fchip rate / processing gain

Filter Response

This module is configured at installation with a 40% rolloff filter. The filter rolloff can be selected among 20%, 25%, 35% and 40%. Changing the rolloff selection requires loading the firmware once using the ComBlock control center, then switching between up to two stored firmware versions (it takes 5 seconds).

All firmware versions can be downloaded from www.comblock.com/download.

COM-1019-**A** DSSS demodulator 20% rolloff

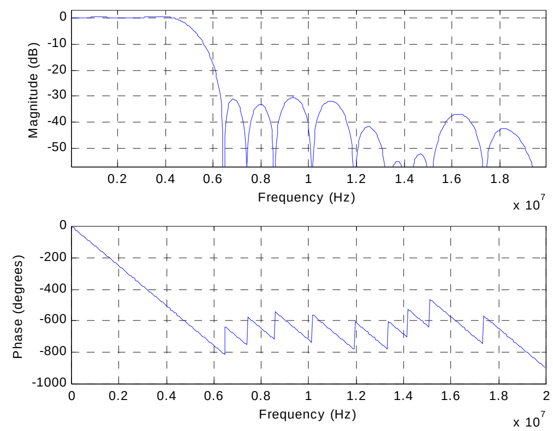
COM-1019-**B** DSSS demodulator 25% rolloff

COM-1019-**D** DSSS demodulator 35% rolloff

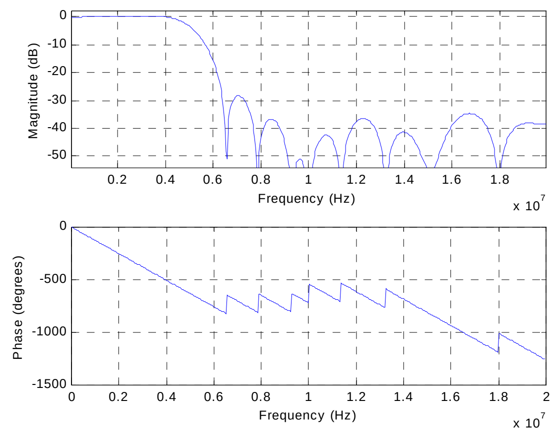
COM-1019-**E** DSSS demodulator 40% rolloff

To verify which firmware is currently installed, open the settings window and click on the "Advanced" button. The firmware option is listed at the bottom of the advanced settings window.

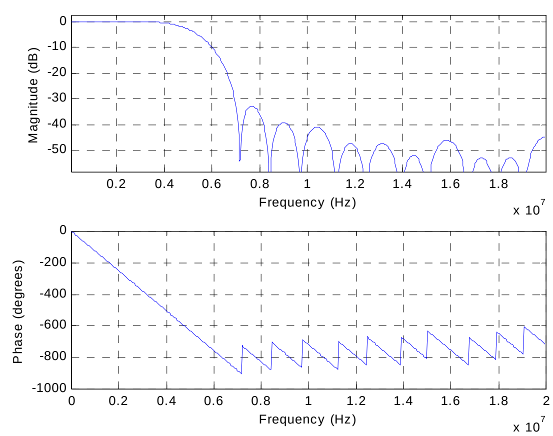
Filter Response (-A 20% rolloff)



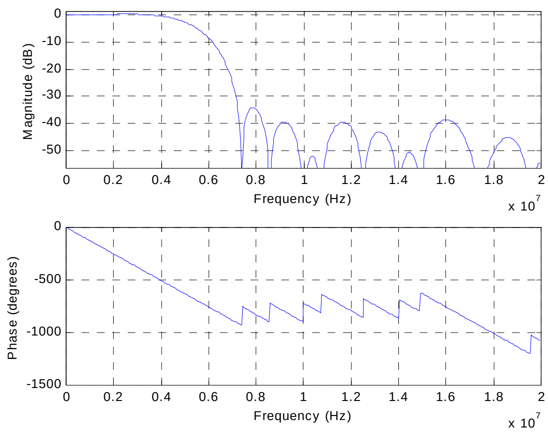
Filter Response (-B 25% rolloff)



Filter Response (-D 35% rolloff)

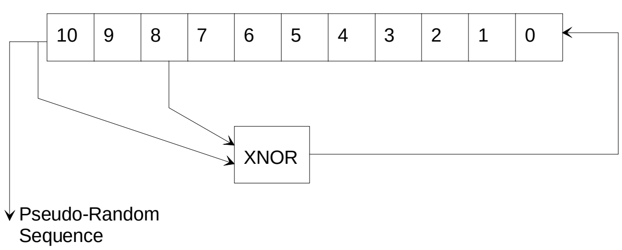


Filter Response (-E 40% rolloff)



Pseudo-Random Bit Stream (Test Pattern)

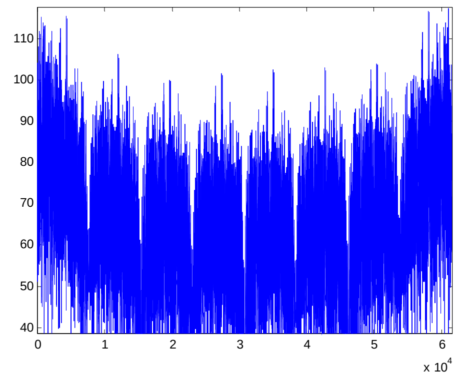
A periodic pseudo-random sequence can be used as modulator source instead of the input data stream. A typical use would be for end-to-end bit-error-rate measurement of a communication link. The sequence is 2047-bit long maximum length sequence generated by a 11-tap linear feedback shift register:



The first 100 bits of the PN sequence are as follows:
0000000000 0111111111 0011111110 0001111100
1100111000 0000010011 1111010001 1110110100
1101001100 0011000001

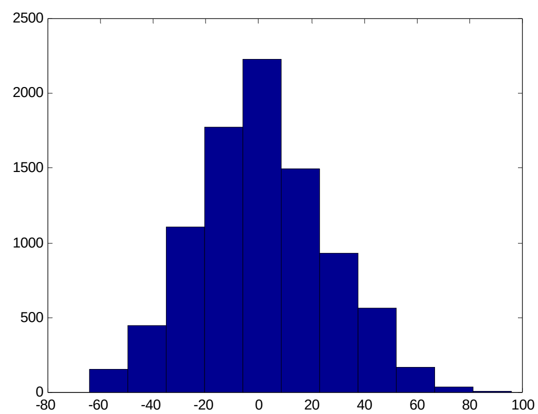
Additive White Gaussian Noise (Test Mode)

To help simulating link impairements, a simple digitally generated noise source is built in this module. The equivalent noise bandwidth is +/- 2 x chip rate. The noise samples do not undergo raised cosine square root filtering. Therefore its wideband spectrum tends towards a sin(x)/x function.



(Noise samples power spectrum over 66,000 samples)

The noise samples standard deviation is 27.8 for a noise gain setting of 64. Below is the amplitude histogram for this noise gain setting.



(Noise amplitude histogram, noise gain 64)

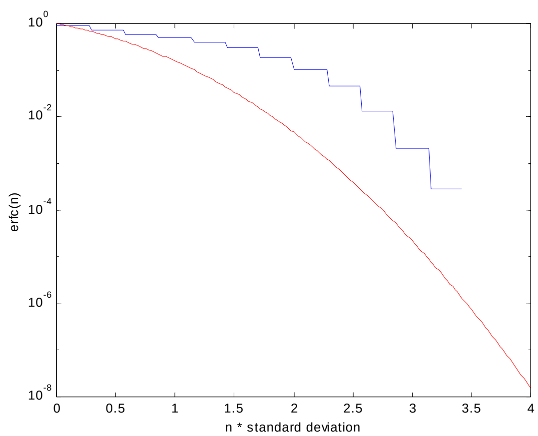
The noise standard deviation is proportional to the noise gain setting.

Below are a few useful reference points for setting the signal to noise ratio. All SNRs are measured in the modulated signal bandwidth, assuming QPSK modulation.

SNR (QPSK modulation)	Signal Gain	Noise Gain
19.3 dB	x40	x20
13.3 dB	x40	x40
10 dB	x40	x5B
7.3 dB	x40	x80
6.1 dB	x40	x90
5.3 dB	x40	xA0
4.5 dB	x40	xB0
3.7 dB	x40	xC0
3.0 dB	x40	xD0
2.3 dB	x40	xE0
1.2 dB	x40	xFF

When BPSK modulation is selected, the SNR is 3 dB lower for a given signal gain and noise gain setting: the reason is that noise is still added on both I and Q channels, whereas data is only transmitted on the I channel.

This noise generator is accurate as far as SNR measurements are concerned. However, it only approximates the Gaussian distribution. Therefore, this noise generator can only be used for bit error rate measurements if it is calibrated. The calibration plot below shows the erfc function for a theoretical Gaussian random variable (red) and for the built-in noise generator (blue).



Noise generator distribution calibration (erfc function)

Clock / Timing

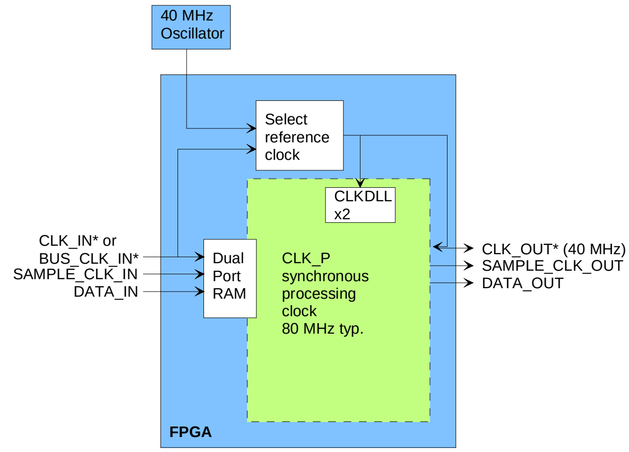
Clocks

The COM-1019 can use two different reference clocks:

- an external clock CLK_IN/BUS_CLK_IN.
- an internal 40 MHz oscillator on the COM-1019 module.

Under user-control (see REG18 bit 0), the COM-1019 selects external versus internal reference clock. Internal clock must be selected while the COM-1019 is in test mode (i.e. no input, the data stream is internally generated). External clock must be selected when synchronizing several modulators for signal diversity combining applications.

The selected clock is used as reference for the output CLK_OUT clock and, after frequency doubling, as the 80 MHz **f_{clk}** processing clock.



(*) denotes edge-trigger signal

When the internal reference clock is selected, the processing clock **f_{clk}** is not related to the CLK_IN clock frequency. In this case, the role of CLK_IN is restricted to that of input clock. It can therefore take any frequency value up to the maximum of 40 MHz.

When the external reference clock is selected, we recommend that a 40 MHz clock be used as CLK_IN.

Input buffer

Input data DATA_IN is first written into an input elastic buffer at the rising edge of CLK_IN when SAMPLE_CLK_IN = ‘1’.

The data is read out of the input elastic buffer at the selected bit rate (chip rate / spreading factor * 1 (BPSK) or *2 (QPSK)).

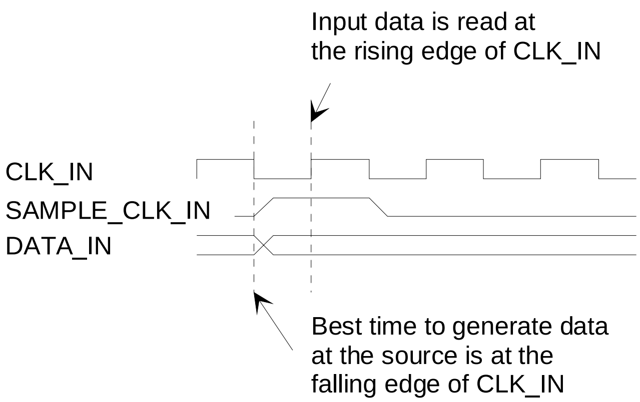
The input buffer size is 256 symbols.

I/Os

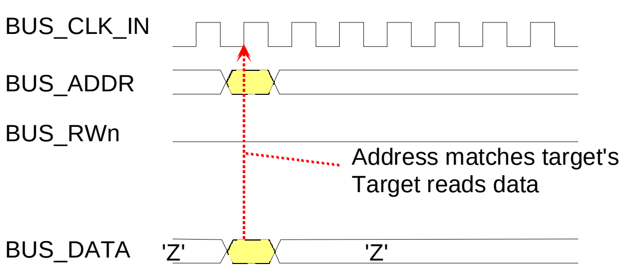
The I/O signals are synchronous with the rising edge of the reference clock CLK_IN or CLK_OUT (i.e. all signals transitions always occur after the rising edge of clock). The maximum frequency for CLK_IN is 40 MHz. The frequency for CLK_OUT is fixed at 40 MHz ($f_{clk}/2$) .

Input Connector

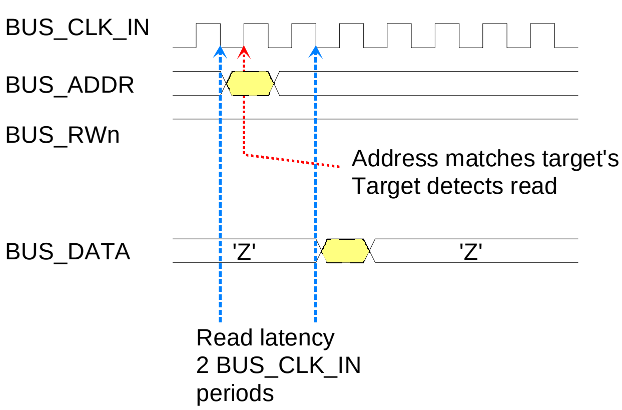
Point to Point connection (REG19 bit4 = 0)



Point to Multi-points connection (REG19 bit4 = 1).
COM-1019 is a bus slave. It always listens to
BUS_CLK_IN, BUS_ADDR, BUS_RWN.



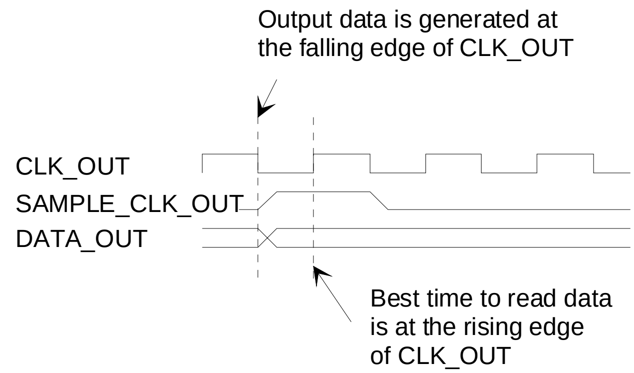
Master writes data streams to COM-1019 target(s)

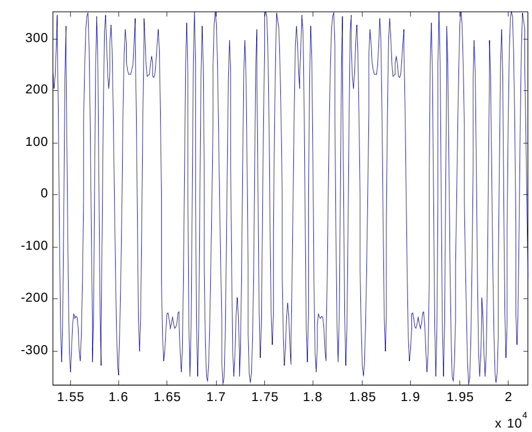


Master reads flow control from COM-1019 target

Output Connector

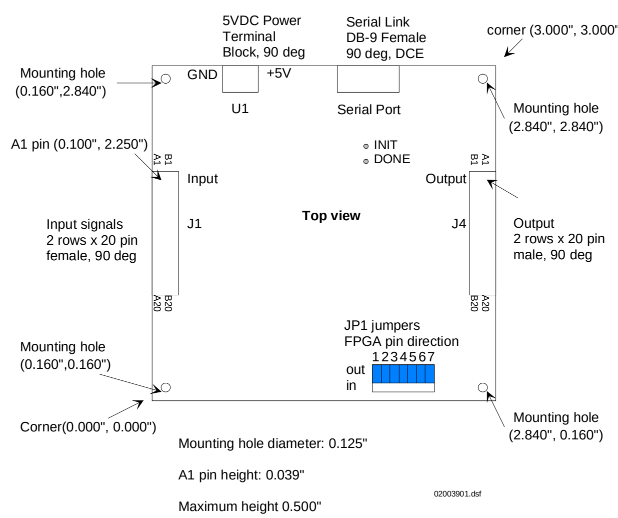
(REG19 bit0 = 0)





Sample output waveform (63-chip spreading code, 40% rolloff, 10-bit samples, maximum amplitude)

Mechanical Interface

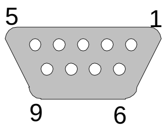


Note: All seven JP1 jumpers must be in the 'OUT' location.

Pinout

Serial Link

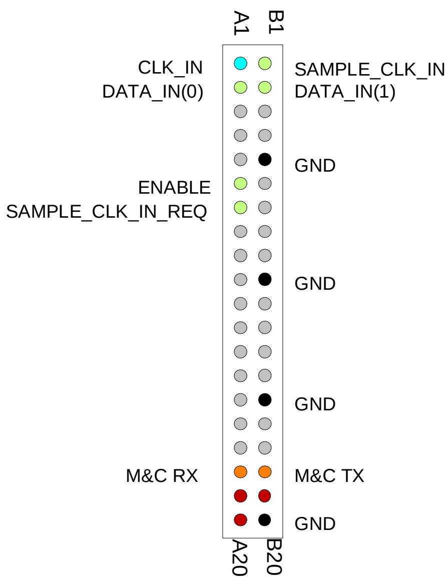
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



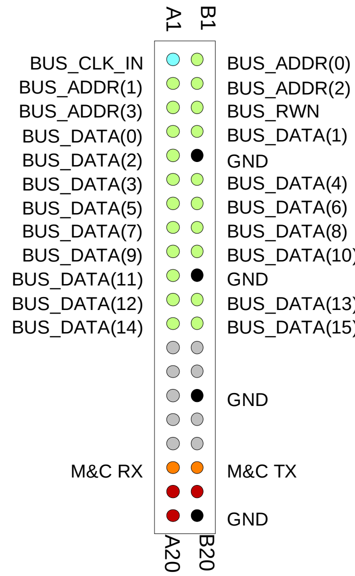
2 Transmit
3 Receive
5 Ground

DB-9 Female

Input Connector J1

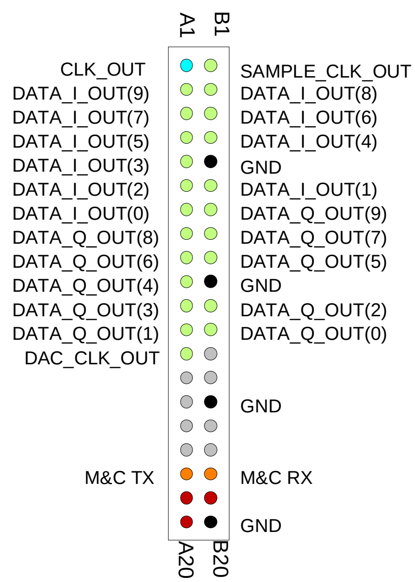


This connector is used for point-to-point input, i.e. direct connection between two ComBlocks when control register REG19(4) = '0'.

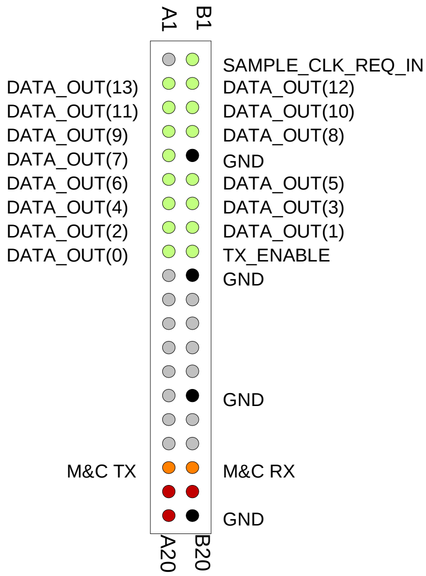


This connector is used for point-to-multipoint (bus) connection when control register REG19(4) = '1'. COM-1019 is a bus slave. It always listens to BUS_CLK_IN, BUS_ADDR, BUS_RWN.

Output Connector J4



This connector is used when output data is pushed out (configuration REG19 bit 0 = 0).



This connector is used when output data is pulled out by the next module (configuration REG19 bit 0 = 1).

I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-1010 Convolutional encoder	COM-1418 DSSS Demodulator 22 Mchips (back to back)
COM-7001 Turbo Code Error correction encoder	COM-2001 digital-to-analog converter (baseband).
COM-1410 LDPC + long BCH code error correction encoder	COM-4004 70 MHz IF modulator
COM-8001 Arbitrary waveform generator 256MB	COM-1024 Multi-path simulator
COM-8004 Signal diversity splitter	COM-1023 BER generator, Additive White Gaussian Noise Generator
COM-5003 TCP-IP / USB Gateway	

Configuration Management

This specification is to be used in conjunction with VHDL software revision 12.

ComBlock Ordering Information

COM-1019
Direct-sequence spread-spectrum modulator 20 Mchips.

MSS • 18221-A Flower Hill Way •
Gaithersburg, Maryland 20879 • U.S.A.
Telephone: (240) 631-1111
Facsimile: (240) 631-1676
E-mail: sales@comblock.com