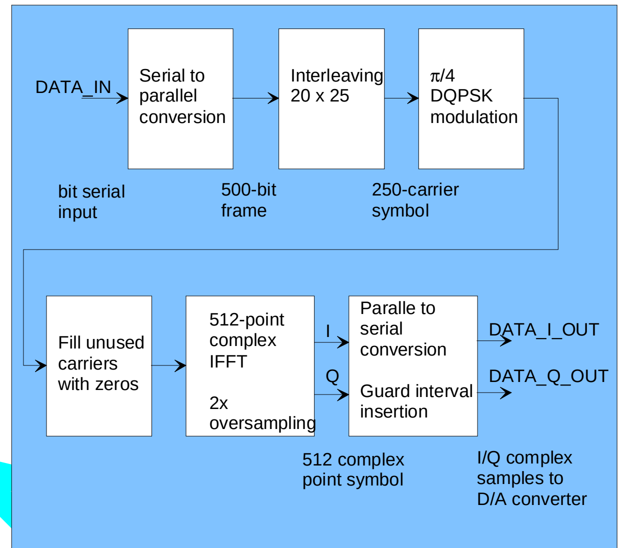
Com Block

COM-1022 COFDM MODULATOR 3 Mbit/s

Key Features

- COFDM Modulator. Variable data rate up to 3.3 Mbits.
- Modulation: 256 carriers, $\pi/4$ differential QPSK, 20x25 frequency interleaving.
- Variable guard interval.
- Internal generation of pseudo-random bit stream and unmodulated carrier for test purposes.
- Built-in channel impairments generation:
  - frequency offset (Doppler)
- Single 5V supply
- Connectorized 3"x 3" module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom)
- Interfaces with 5V and 3.3V logic.

Block Diagram



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For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1022.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

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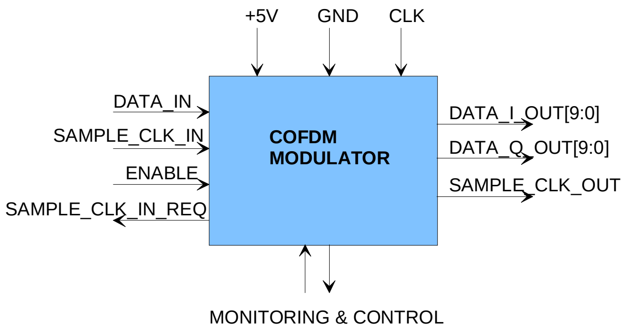
Electrical Interface

Modulator Inputs / Outputs



Input Module Interface	**Definition**
DATA_IN	Input data stream.
SOF_IN	Optional start of frame input pulse. A COFDM frame comprises 500 data bits. This 1-CLK wide pulse is aligned with SAMPLE_CLK_IN. If the SOF_IN signal is not externally provided, it is internally generated. This gives the user the option to synchronize the input stream with the COFDM frame.
SAMPLE_CLK_IN	Input data clock. One CLK-wide pulse. Read the input signals at the rising edge of CLK when SAMPLE_CLK_IN = '1'.
ENABLE	Modulator enable input. Internally pulled high. Qualifies the SAMPLE_CLK_IN. Used for burst-mode transmission. In continuous mode, keep at '1'.
SAMPLE_CLK_IN_REQ	One CLK-wide pulse. Requests a sample from the module upstream. For flow-control purposes.
Output Module Interface	**Definition**
DATA_I_OUT[9:0]	Modulated output signal, real axis. 10-bit precision. Format: 2's complement or unsigned, selected by configuration bit 1.
DATA_Q_OUT[9:0]	Modulated output signal, imaginary axis. 10-bit precision. Same format as DATA_I_OUT.
SAMPLE_CLK_OUT	Output signal sampling clock. Read the output signal at the rising edge of CLK when SAMPLE_CLK_OUT = '1'. Sampling rate is either 4 x symbol rate or fclk (interpolation off/on configuration bit 7). SAMPLE_CLK_OUT can stay high when output samples are transmitted in successive CLK periods.
DAC_CLK_OUT	Output sampling clock for Digital to Analog Converters. DAC reads the output sample at the rising edge.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 300mA.

Configuration (via Serial Link / LAN)

Complete assemblies can monitored and controlled centrally over a single serial or LAN connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

Parameters	**Configuration**
Output sampling rate f_s	Unsigned 24-bit integer expressed as f_s * 2^24 / fclk, where fclk is the processing clock, typically 40 MHz. The occupied bandwith is $f_s/2$, nearly centered around zero frequency. The spacing between COFDM carriers is $f_s/512$. REG0 = bit 7-0 REG1 = bit 15 – 8 REG2 = bit 23 – 16
Guard interval	The guard interval between symbols is expressed as an integer number of output samples. REG3 = bits 7-0 REG4 = bits 15-8
Offset carrier frequency	24-bit signed integer (2's complement) expressed as fc * 2^24 / f_s. Default value: **0** REG5 = bit 7 – 0

	REG6 = bit 15 – 8 REG7 = bit 23 - 16
Signal gain	Signal level. 8-bit unsigned integer. Maximum level 255, Minimum level 0. REG8 = bit 7-0
Output sample format	0 = 2's complement 1 = unsigned REG9 bit 0
Test mode	00 = disabled 01 = truncated PRBS-11, internally generated. Truncated from 2047 to a single COFDM frame of 500 bits. (overrides external input bit stream). 10 = PRBS-11, internally generated. (overrides external input bit stream). 11 = unmodulated carrier. (overrides external input bit stream) REG9 bit 2-1
Output data flow	0 = output data is pushed to the next module (for example to COM-2001, or COM-1001) 1 = output data is pulled by next module (for example by the COM-4004) REG9 bit 3
Interpolation	Interpolation to maximum clock rate. 0 = off 1 = on REG9 bit 4

COFDM Modulation Specifications

Step 1: Serial to parallel conversion

The serial input bit stream d_i first undersgoes a serial to parallel conversion into a 500-bit long frame. (d_0 , d_1, d_2, ,…. d_{499}).

Step 2: Interleaving

Multi-paths occurring naturally in terrestrial transmissions cause selective frequency fading. Each 'hole' in the spectrum results in a burst of bit errors in a demodulated COFDM frame. In order to spread the bit errors as uniformly as possible, the bits within a COFDM frame are reshuffled by a 20 columns x 25 rows interleaver. Let us denote i_j the interleaver output. The 20x25 matrix is written by filling one complete column after another. It is read by emptying one complete row after another.

	Column 1	Column 2	…….	Column 19	Column 20
Row 1	$i_0 = d_0$	$i_1 = d_{25}$		$i_{18} = d_{450}$	$i_{19} = d_{475}$
Row 2	$i_{20} = d_1$	$i_{21} = d_{26}$		$i_{38} = d_{451}$	$i_{39} = d_{476}$
…….					
Row 24	$i_{460} = d_{23}$	$i_{461} = d_{48}$		$i_{478} = d_{473}$	$i_{479} = d_{498}$
Row 25	$i_{480} = d_{24}$	$i_{481} = d_{49}$		$i_{498} = d_{474}$	$i_{499} = d_{499}$

Step 3: $\pi/4$ differential QPSK modulation

Each group of two bits (i_j , i_{j+1}) is mapped into a phase on the constant amplitude complex circle: (0,0) for 0 deg, (1,0) for 90 deg, (0,1) for 180 deg and (1,1) for 270 deg.

For each group of two bits, the phase difference between the current frame and the last frame is computed. An offset of 45 degrees is added to force a change even when data is constant. This results in a complex vector of 250 symbols: S = (s_0, s_1, s_2, ….., s_{249}). All elements have the same amplitude.

As this processing is performed in the frequency domain (the vector will undergo an IFFT in the next step), each element of the vector represents a $\pi/4$ DQPSK modulated subcarrier.

Step 4: IFFT

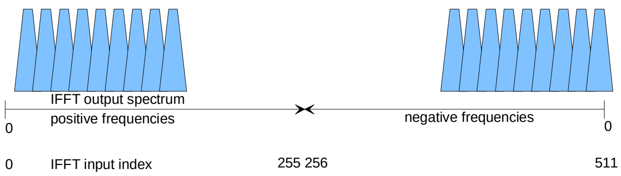
Conversion from the frequency domain to the time domain is performed using a 512 point inverse FFT (IFFT). The IFFT generates 256 carriers with 2x oversampling. 250 of these carriers are modulated with the DQPSK symbols. The other 6 carriers are used to create nulls and unmodulated pilot tones in the modulated signal to help the COFDM receiver perform coarse frequency acquisition.

The modulated spectrum is kept approximately symmetrical to help the COFDM receiver with very coarse frequency acquisition (the upper cutoff frequency is f_s*127.5/512, while the lower cutoff frequency is =f_s*128.5/512).

Let us denote as X = (x_0, x_1, x_2, ….., x_{511}) the complex vector at the IFFT input. The DQPSK complex vector is mapped into the X vector as follows:

For i = 0 to 124, the DQPSK symbols are modulated onto positive frequency subcarriers $x_{i+3} = s_i$

For i = 125 to 249, the DQPSK symbols are modulated onto negative frequency subcarriers $x_{262+i} = s_i$

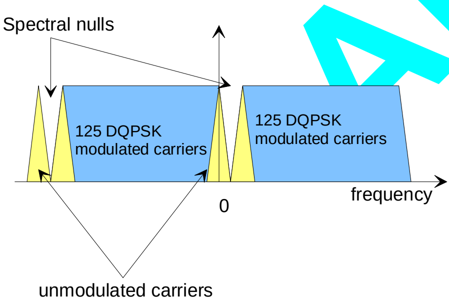


The IFFT also creates two spectrum nulls at IFFT indices 1 and 385. Each null is surrounded by two unmodulated carriers. These spectral artifacts are used by the COFDM receiver for frequency acquisition and tracking. The wide frequency separation of these two nulls is designed to enhance the receiver algorithm resilience to occasional fading caused by multi-paths.

$x_0 = 1$.
$x_1 = 0$.
$x_2 = 1$.

$x_{384} = 1$.
$x_{385} = 0$.
$x_{386} = 1$.

All other carriers are set to zero.



Output spectrum

Step 5: Parallel to serial conversion

Conversion from the frequency domain to the time domain. The IFFT output is clocked out as 512 complex I/Q samples. The output sampling clock is user defined (see configuration registers REG0/1/2).

A guard interval is placed between two successive IFFT frames. The guard interval duration is user defined (see configuration register REG3/4). During the guard interval, the modulator output is zero. The purpose of the guard interval is to ensure detection of the most direct path at the receiver.

The following Matlab code also describes the COFDM modulation as implemented within the COM-1022 module. TBD.

Operation

Maximum speed

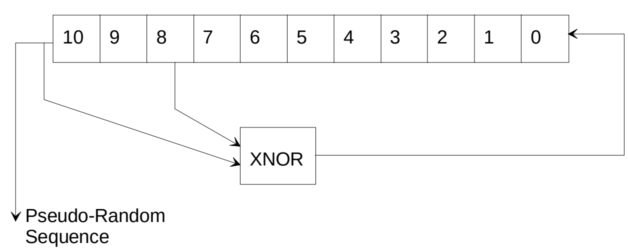
The speed is limited by the Xilinx Spartan2-200 FPGA's ability to compute a 512-point FFTs at the clock rate of 40 MHz. The mimum time between two COFDM frames is 150 µs.

For example, if a 10 µs guard interval is programmed, the maximum output sampling clock f_s is 512/(150 µs – 10µs) = 3.65 Msamples/s.

The maximum data rate (for a 10 µs guard interval) is 500 bits / 150 µs = 3.3 Mbit/s.

Pseudo-Random Bit Stream (Test Pattern)

A periodic pseudo-random sequence can be used as modulator source instead of the input data stream. A typical use would be for end-to-end bit-error-rate measurement of a communication link. The sequence is 2047-bit long maximum length sequence generated by a 11-tap linear feedback shift register:

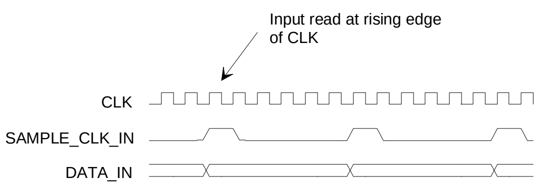


The first 100 bits of the PN sequence are as follows:
0000000000 0111111111 0011111110 0001111100 1100111000 0000010011 1111010001 1110110100 1101001100 0011000001

Timing

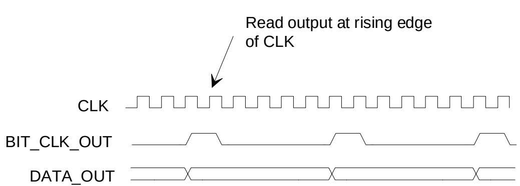
The I/O signals are synchronous with the rising edge of the reference clock CLK (i.e. all signals transitions always occur after the rising edge of the reference clock CLK). The maximum CLK frequency is 40 MHz.

Input



Output

(REG9 bit3 = 0)

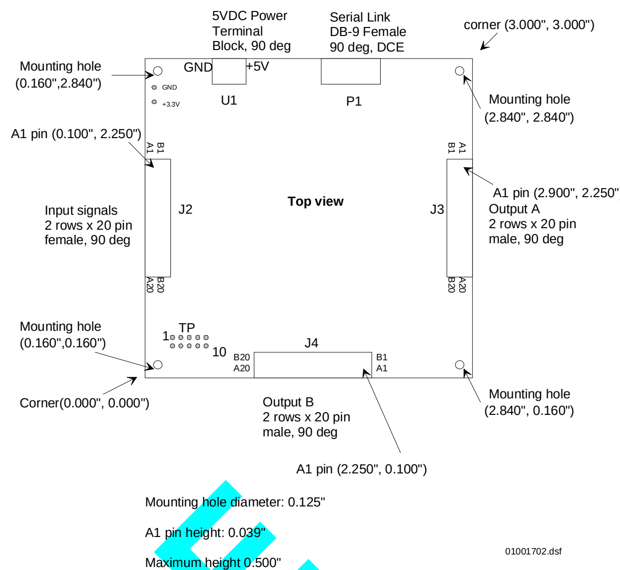


Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
TP1	Symbol rate
TP2	Guard interval
TP3	Output sample clock

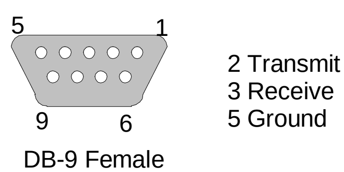
Mechanical Interface



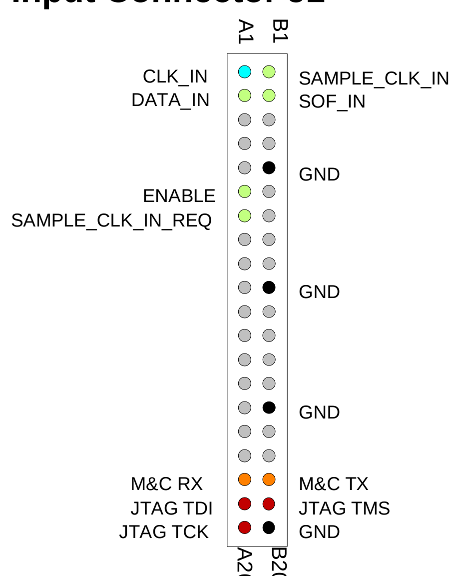
Pinout

Serial Link P1

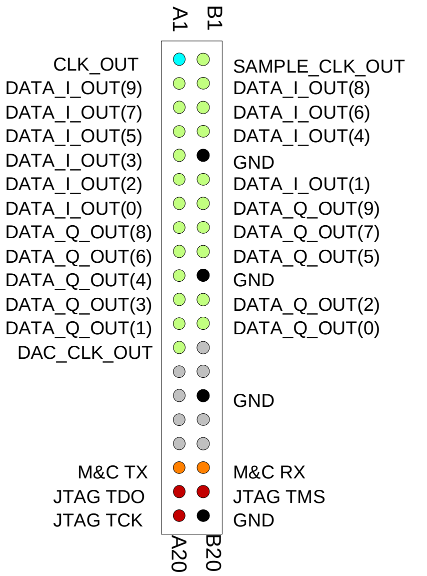
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



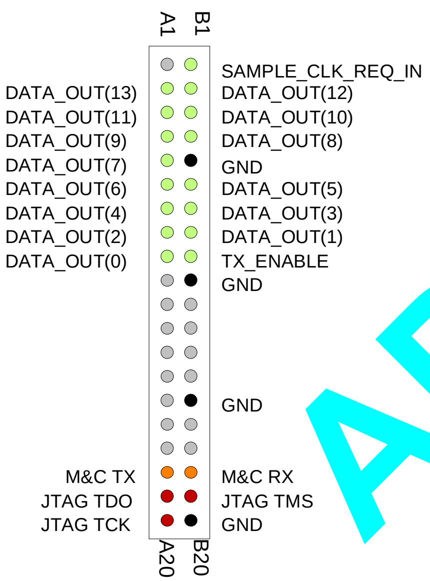
Input Connector J2



Output Connectors J3, J4



This connector is used when output data is pushed out (configuration REG9 bit 3 = 0).



This connector is used when output data is pulled out by the next module (configuration REG9 bit 3 = 1).

I/O Compatibility List

(not an exhaustive list)

Input	**Output**
COM-1010 Convolutional encoder	COM-2001 digital-to-analog converter (baseband).
COM-7001 Turbo Code Error Correction	COM-4004 70 MHz IF modulator
COM-8001 Pattern generator 256MB	COM-1023 BER generator, Additive White Gaussian Noise Generator
	COM-1024 Multipath simulator.

ComBlock Ordering Information

COM-1022
COFDM modulator

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