COM-1023
BIT ERROR RATE GENERATOR
ADDITIVE WHITE GAUSSIAN NOISE GENERATOR

Key Features

- Synchronous serial bit error rate generator. Generates randomly distributed bit errors.
- Additive white gaussian noise generator. 2-channel, 10 bits/sample
- Maximum throughput 40 Msamples/s.
- Accurately generates Additive White Gaussian Noise. Normal distribution up to 4.5 times the standard deviation. Box-Muller algorithm.
- Tabulates actual bit errors over an adjustable window from 1,000 bits to 1,000,000,000 bits, to trade off BER range and measurement duration.
- Single 5V supply
- Connectorized 3"x 3" module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom)
- Interfaces with 5V and 3.3V logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1023.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.html .

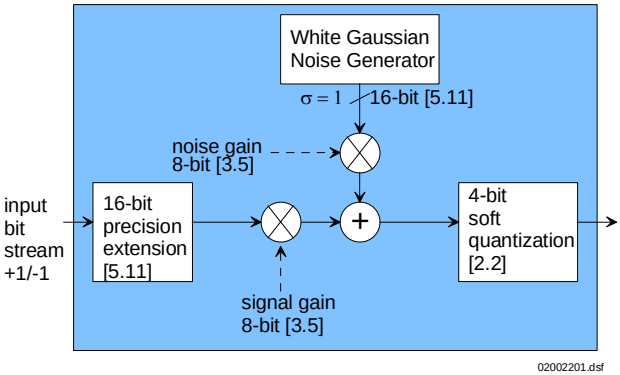
Application1 : Bit Error Rate Generator

Digital communication systems are often characterized in presence of additive white gaussian noise (AWGN) in the transmission channel. Whereas noise is easily generated by analog means, digital generation of AWGN is significantly more complex.

The purpose of this module is to generate an accurate AWGN with the following properties:

- random distribution up to +/- 4.5σ (4.5*standard deviation) .
- resolution: 10 bits
- periodicity greater than 2^{32} samples.

This makes this module practical for bit error insertion in the range from 0.5 to 10^{-10}.



Bit Error Rate Generator

Bit errors are generated by adding a white gaussian noise variable to the input bit stream. The number of bit errors is controlled by adjusting the standard deviation of the AWGN and/or the input signal amplitude. After the noise is added, the output bits are quantized with 4-bit precision to mimic the 4-bit soft-quantized output of a digital demodulator. Indeed, FEC decoders, whether Viterbi or Turbo-code decoders, often perform to their best ability when given soft quantized inputs.

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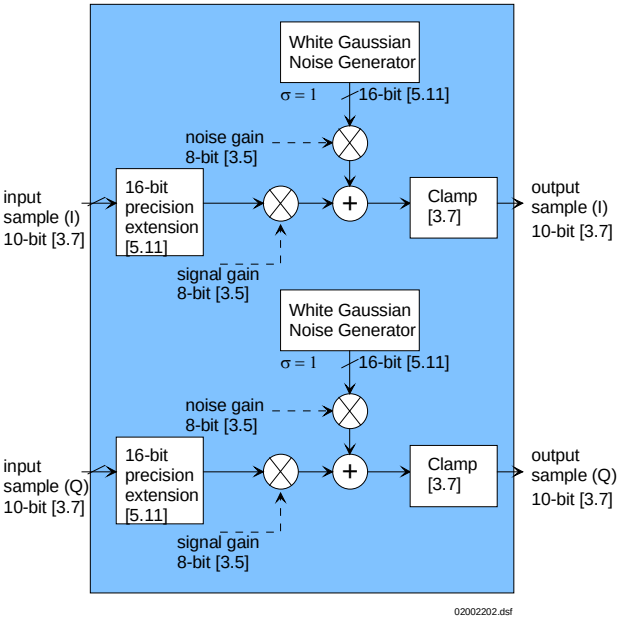
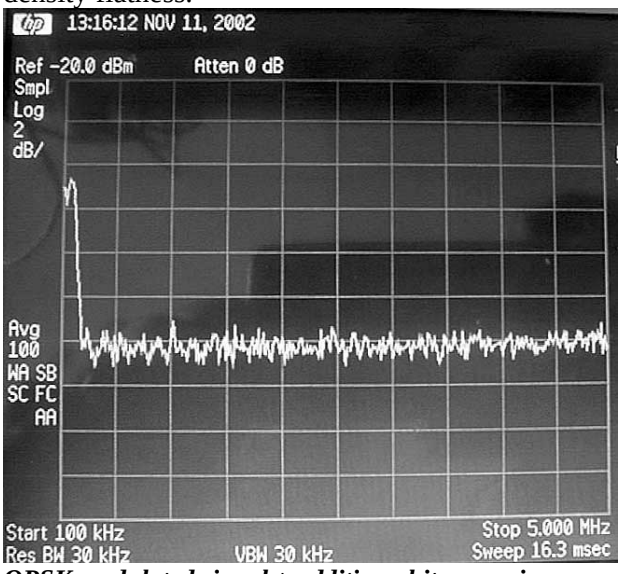
Application2 : AWGN Generator

Two independent white gaussian noise generators are used to add noise to a complex signal represented by two 10-bit I and Q samples.

In order to help with the SNR calibration process, the noise power and the signal power are measured.



The figure below illustrates an AWGN added onto a 500 Ksymbols/s QPSK signal generated by a COM-1002 module. The SNR is set at 6 dB within the modulation bandwidth. Note the noise spectral density flatness.



QPSK modulated signal + additive white gaussian noise. 2 dB/division. 6 dB SNR.

Electrical Interface

Input Interface	**Definition**
DATA_I_IN[9:0]	(a) In-phase sample. Unsigned 10-bit format, or (b) Input bit stream. 1-bit serial on DATA_I_IN(9)
DATA_Q_IN[9:0]	Quadrature sample. Unsigned 10-bit format.
SAMPLE_CLK_IN	Input sampling clock. One CLK-wide pulse. Read the input signals at the rising edge of CLK_IN when SAMPLE_CLK_IN = '1'.
SAMPLE_CLK_IN_REQ	One CLK-wide pulse. Requests a sample from the module upstream. For flow-control purposes.
CLK_IN	Input reference clock for synchronous I/O (inputs are read at the rising edge of CLK_IN). Also used as FPGA internal processing clock $\mathbf{f_{clk}}$. Maximum 40 MHz.
Output Interface	**Definition**
DATA_I_OUT[9:0]	(a) Output In-phase sample plus AWGN. Unsigned 10-bit format, or (b) Output bit stream. Mimics 4-bit soft-quantization. Unsigned representation.
DATA_Q_OUT[9:0]	Output quadrature sample plus AWGN. Unsigned 10-bit format.
SAMPLE_CLK_OUT	Output clock. One CLK-wide pulse. Read the output signals at the rising edge of CLK when SAMPLE_CLK_OUT = '1'.
SAMPLE_CLK_OUT_REQ	Input. Sample request from the module downstream. For flow control purposes.
DAC_CLK_OUT	Output sampling clock for Digital to Analog Converters. DAC reads the output sample at the rising edge.
CLK_OUT	40 MHz output reference clock. Same as CLK_IN.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow

	control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 300mA.

Configuration (via Serial Link / LAN)

Complete assemblies can be monitored and controlled centrally over a single serial or LAN connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

This module operates at a processing rate $\mathbf{f_{clk}}$ set by CLK_IN (typically 40 MHz).

Parameters	**Configuration**
Sampling rate	Sets a maximum sampling rate through this module. Special case: enter zero for the maximum sampling rate (40 Msamples/s). Note: this has no effect on most digital modulators upstream (COM-1002/1012/1019/1028/1402/1428). The sampling rate is regulated by two mechanism: (a) the downstream flow-control signal SAMPLE_CLK_OUT_REQ generated by the module downstream, and (b) the internal numerically controlled oscillator (NCO), the frequency of which is set here. In turn, this module generates a SAMPLE_CLK_IN_REQ upstream flow control signal to control the input data flow from the module upstream. The maximum sampling rate is expressed as bit rate * 2^{24} / $\mathbf{f_{clk}}$, where $\mathbf{f_{clk}}$ is the CLK_IN reference clock frequency (typically 40 MHz). REG0 = bit 7-0 (LSB) REG1 = bit 15 – 8 REG2 = bit 23 – 16 (MSB)
Input format	00 = 1-bit serial 01 = 10-bit unsigned, complex (I,Q) REG3 bits 2-1
Output format	00 = 4-bit soft-quantized 01 = 10-bit unsigned, complex (I,Q) REG3 bits 4-3
BER measurement window	Number of bits in the window where errors are counted: 000 = 1,000 001 = 10,000 010 = 100,000 011 = 1,000,000 100 = 10,000,000 101 = 100,000,000 110 = 1,000,000,000 Meaningful only when the input format selection is 1-bit serial. REG3 bits 7-5
Signal gain G_s	Scale the input signal in amplitude. The scaling factor G_s is expressed as a numerical value in fractional binary format 3.5, unsigned. Unit gain is 0x20 REG4 bits 7-0
Noise gain G_n (AWGN standard deviation)	Scale the AWGN in amplitude. The scaling factor G_n is expressed as a numerical value in fractional binary format 3.5, unsigned. Unit gain is 0x20. The AWGN standard deviation prior to this adjustment is 1.0. REG5 bits 7-0
Noise bandwidth B_n	Sampling rate for the independent AWGN noise samples. This parameter allows one to control the noise bandwidth. The resulting noise spectrum has a sin(x)/x shape, which approximates a uniform spectal density over +/- (noise bandwidth)/2. The noise bandwidth B_n is expressed as B_n * 2^{24} / $\mathbf{f_{clk}}$, where $\mathbf{f_{clk}}$ is the CLK_IN reference clock frequency (typically 40 MHz). Special case: the noise bandwidth can be chosen to be equal to the input signal sampling rate (SAMPLE_CLK_IN), by setting the three registers below to zero. REG6 = bit 7-0 (LSB) REG7 = bit 15 – 8 REG8 = bit 23 – 16 (MSB)

Baseline configurations can be found at ***www.comblock.com/tsbasic_settings.htm*** and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

Monitoring (Serial Link)

Monitoring registers are read-only.

Parameters	Monitoring
Bit Errors	Actual number of bit errors in a fixed-length window. 32 bit unsigned. REG10: error_count[7:0] REG11: error_count[15:8] REG12: error_count[23:16] REG13: error_count[31:24] This measurement is meaningful only when the input format selection is 1-bit serial.
Measured input signal power	24-bit unsigned number. The input signal power measurement is obtained by averaging $DATA\_I\_IN^2$ + $DATA\_Q\_IN^2$ over 16,384 complex input samples. The power measurement is measured prior to applying the signal amplitude scaling factor specified in control register REG4. REG14: bits 7-0 REG15: bits 15-8 REG16: bits 23-16
Measured noise power	24-bit unsigned number. The power measurement is obtained by averaging $NOISE\_I^2$ + $NOISE\_Q^2$ over 16,384 complex input samples. This noise power measurement is measured prior to applying the noise amplitude scaling factor specified in control register REG5. The format is 8.16. REG17: bits 7-0 REG18: bits 15-8 REG19: bits 23-16
Version	Returns '1023x' when prompted for version number.

Algorithm

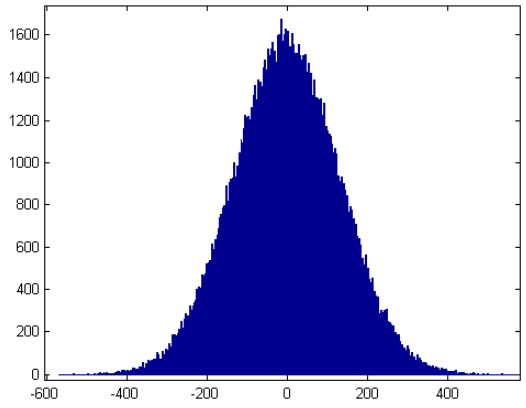
The Box-Muller algorithm is used to transform a uniformly distributed random variable to a gaussian-distribution random variable. A description of the algorithm, together with an elegant FPGA implementation method can be found in reference [1].

The MATLAB program below illustrates how the algorithm works:

```
% Box Muller algorithm verification
nsamples = 1000000;

% generate two independent uniform
distributed random variables
x1 = rand(nsamples,1);
x2 = rand(nsamples,1);

% transform the distributions
f = sqrt(-log(x1));
g = sqrt(2.0)*cos(2*pi*x2);

%gaussian distribution
n = f.*g;

% plot histogram
hist(n,500)

% standard deviation is 1.0
std(n)

% mean is zero
mean(n)
```

[1] "Efficient FPGA Implementation of Gaussian Noise Generator for Communication Channel Emulation". Jean-Luc Danger, Adel Ghazel, Emmanual Boutillon, Hedi Laamari. 2002.

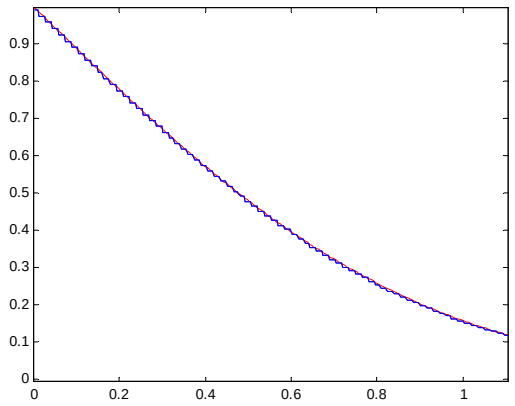
The resulting noise sample distribution is shown below:



Noise sample histogram (130K samples)

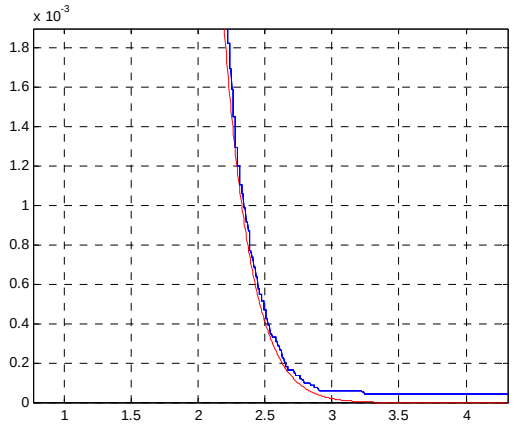
Mean = 0.
Standard deviation = 128

The plots below illustrate how accurate the noise generation is, by comparing the erfc function (red) with the AWGN normalized distribution (blue)



Theoretical erfc function (red) vs actual AWGN normalized distribution measurements (blue). Range 0 – 1, 130K samples.

The theoretical curve and the measured statistical distribution of noise samples are nearly superposed.



Theoretical erfc function (red) vs actual AWGN normalized distribution measurements (blue). Range 1-4, 130K samples.

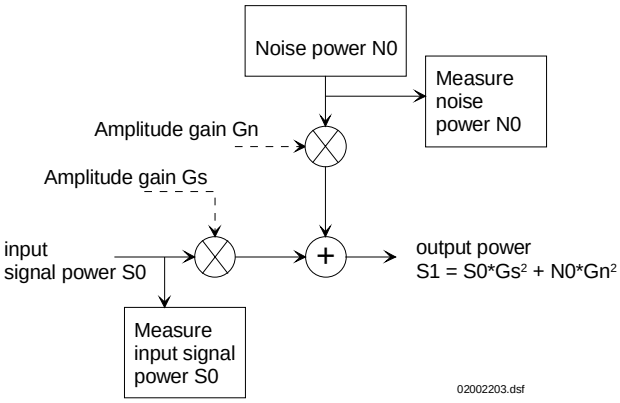
SNR Test Setup

In order to accurately set the signal to noise ratio, the following information must be known:

(a) input signal power S_0
(b) noise power N_0
(c) signal amplitude scaling coefficient G_s
(d) noise amplitude scaling coefficient G_n
(e) input signal bandwidth B_s
(f) noise bandwidth B_n

The signal power S_0 and noise power N_0 are computed by the COM-1023, by averaging power over 16,384 complex samples. The power measurements are expressed as 8.16 values in the monitoring registers REG14-16 and REG17-19 respectively.

The signal and noise amplitude scaling coefficients, G_s and G_n , are set by the user in control registers REG4 and REG5 respectively.



The input signal bandwidth B_s must be known by the user.

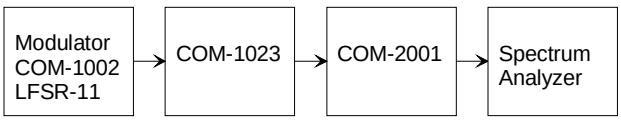
The noise signal bandwidth B_n is typically 40 MHz, as all noise samples are statistically independent. (lower B_n is also achievable, see control registers REG6/7/8)

The total output signal power after amplitude scaling is
$S = S_0 * G_s^2$

The output noise power in the modulation bandwidth, after amplitude scaling is :
$N = N_0 * G_n^2 * B_s / B_n$

The SNR in the modulation bandwidth is thus
$S/N = (S_0 * G_s^2) / (N_0 * G_n^2 * B_s / B_n)$

Example: 1 Msymbols/s QPSK, SNR = 6 dB



COM-1002 configuration: 99 99 19 00 00 00 FF 00 96 00
COM-1023 configuration: 00 00 00 0B 08 20 00 00 00 00
COM-2001 configuration: n/a

S_0 = x76DF4 (read from monitoring REG14-16)
N_0 = x021A13 (read from monitoring REG17-19)
G_s = 0.25 decimal (0x08 in fractional binary 3.5)
G_n = 1.0 decimal (0x20 in fractional binary 3.5)
B_s = 1 MHz
B_n = 40 MHz

S/N in the modulation bandwidth =
$(S_0 * G_s^2) / (N_0 * G_n^2 * B_s / B_n) = 9.48$ dB

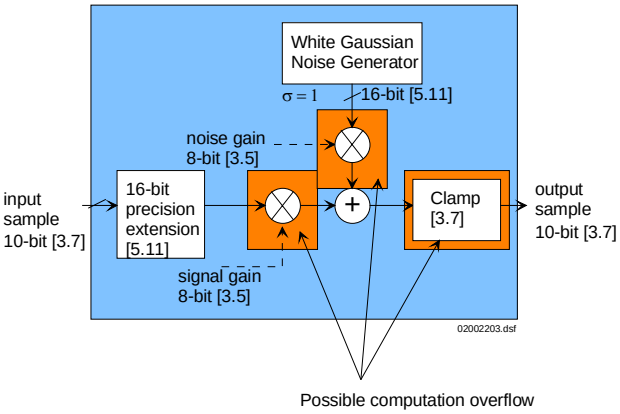
It can be verified that no overflow occurs at the test points TP7 and TP8. Rare overflow occurs at TP9.

Computation Overflow Detection

The COM-1023 module is intended to simulate linear channels. To maintain the linearity, it is essential to avoid any computation overflow condition which can occur in fixed-length digital signal processing. For most configurations and externally-supplied input signals, the COM-1023 ComBlock maintains the signal linearity throughout. In the rare cases when linearity cannot be preserved, the user should be made aware of it. For this reason, the COM-1023 includes three test points allowing the user to check linear operations.

When using this ComBlock as an AWGN generator, there are three places in the signal processing where computation overflow can occur because of the limitation in the number of processing bits:

(a) after scaling the input signal.
(b) after scaling the noise signal.
(c) while summing the scaled input signal and scaled noise signal.



To minimize the negative effects of overflow, overflow signals are clamped to the maximum (positive or negative) value. Overflow never causes a change in the signal sign.

Fractional Representation

Throughout this specification, key signals are described in fractional binary format denoted by x.y. The total number of bits is x+y. The number of bits representing the numerical value below the decimal point is y. x denotes the number of bits representing the numerical value above the decimal point, including one bit for the sign in the case of signed values.

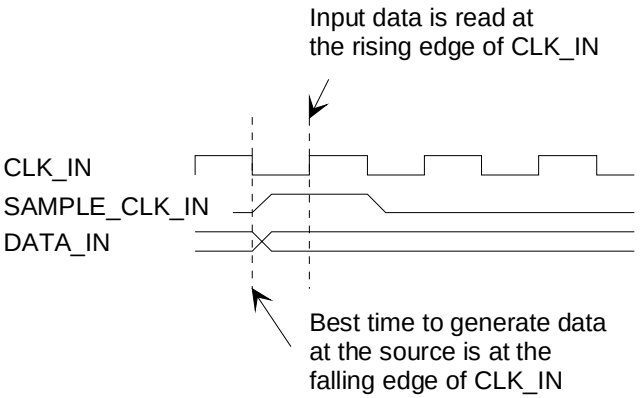
Examples:

Format	*Fractional representation*	*Decimal Equivalent*
3.5 unsigned	001 00000	1.0
3.7 signed	000 1000000	0.5
3.7 signed	111 1000000	-0.5

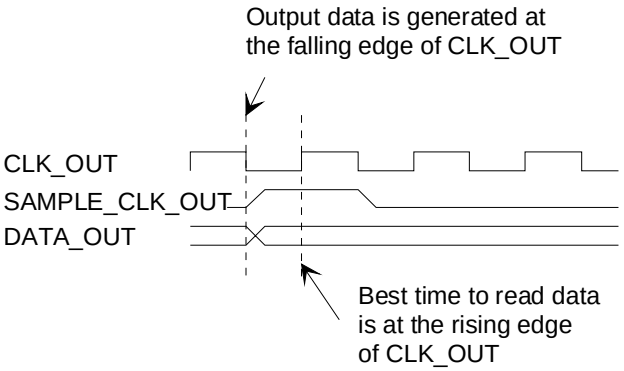
Timing

The I/O signals are synchronous with the rising edge of the reference clock CLK (i.e. all signals transitions always occur after the rising edge of the reference clock CLK). The maximum CLK frequency is 40 MHz.

Input



Output

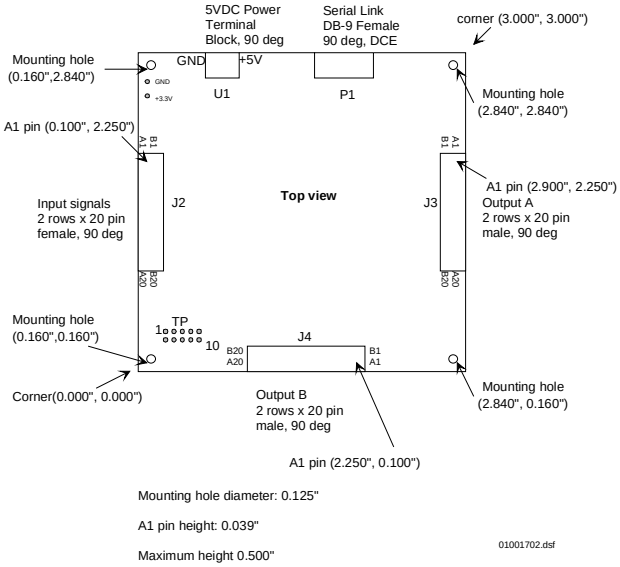


Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	**Definition**
TP1	Input data stream
TP2	Input bit clock
TP3	Bit clock request
TP4	Bit error (meaningful only when the input format selection is 1-bit serial.)
TP5	Output data stream (MSB)
TP6	Output bit clock
TP7	Overflow after signal scaling
TP8	Overflow after noise scaling
TP9	Overflow after summing signal + noise
TP10	BER measurement period

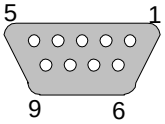
Mechanical Interface



Pinout

Serial Link P1

The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.

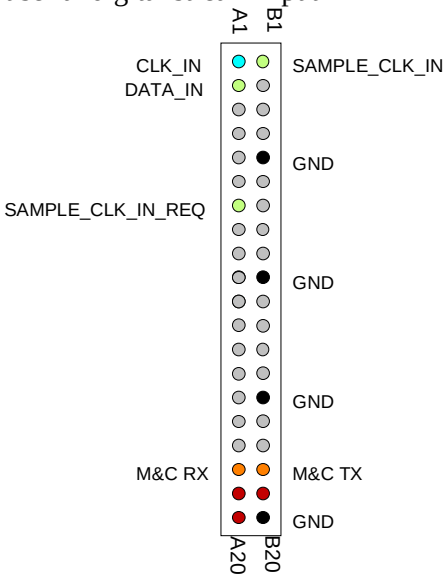


DB-9 Female

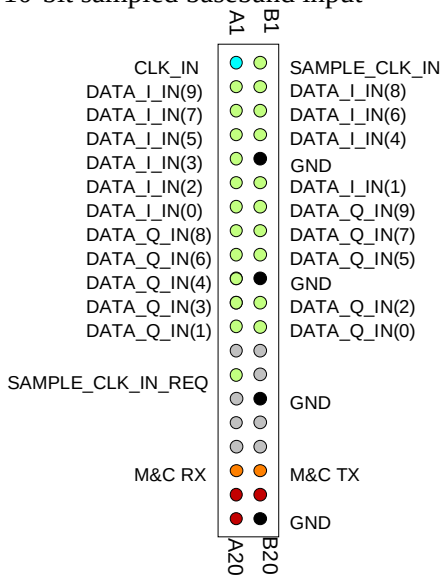
2 Transmit
3 Receive
5 Ground

Input Connector J2

(a) 1-bit serial digital stream input

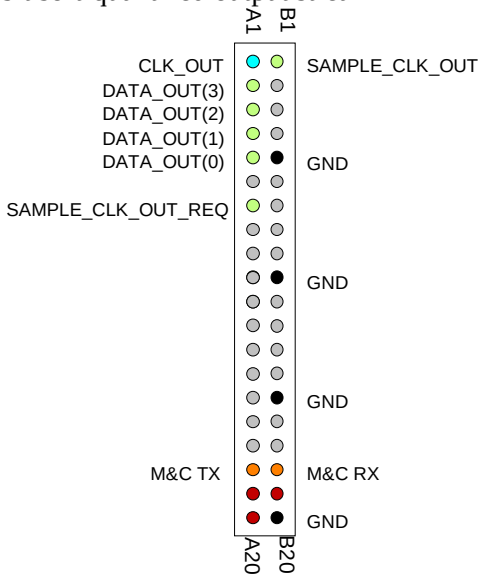


(b) 2 x 10-bit sampled baseband input

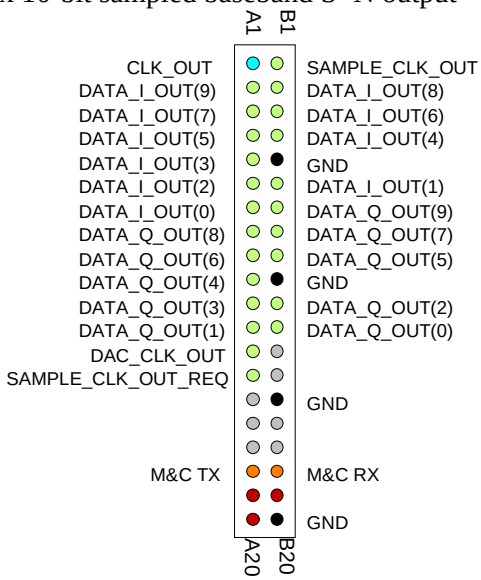


Output Connectors J3/J4

(a) 4-bit soft-quantized output stream



(b) 2 x 10-bit sampled baseband S+N output



I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-300x RF receivers	
COM-1024 Multipath simulator.	COM-1024 Multipath simulator.
COM-8001 Pattern generator 256MB	COM-2001 digital-to-analog converter (baseband).
COM-7001 Turbo code error correction encoder	COM-7001 Turbo code decoder
COM-1010 Convolutional encoder	COM-1009 Convolutional decoder K=7, 5
COM-1410 LDPC + long BCH code encoder	COM-1209 LDPC + long BCH decoder
	COM-1005 Bit Error Rate measurement
COM-1402 PSK/QAM/APSK digital modulator	COM-1202/1203 PSK/QAM/APSK modem
COM-1019 DSSS modulator	COM-1418 DSSS demodulator
COM-1028 FSK/MSK/GFSK/GMSK digital modulator	COM-1027 FSK/MSK demodulator
COM-5003 TCP-IP / USB Gateway	COM-5003 TCP-IP / USB Gateway

Configuration Management

This specification is to be used in conjunction with software revision 14.

ComBlock Ordering Information

COM-1023 BIT ERROR RATE GENERATOR ADDITIVE WHITE GAUSSIAN NOISE GENERATOR.

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