COM-1024 MULTIPATH SIMULATOR

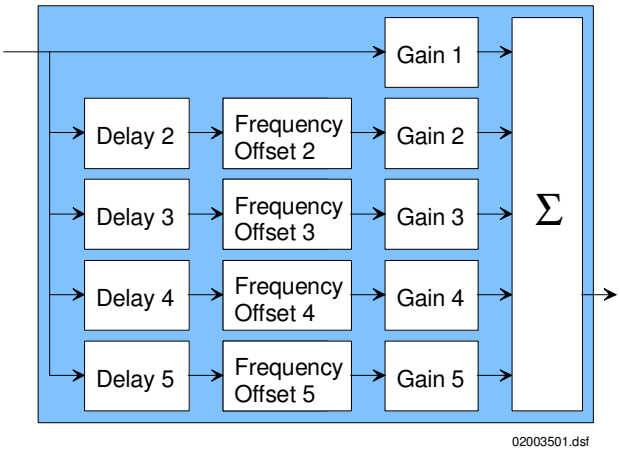
Key Features

- Baseband multipath simulator.
- 5 independently controllable paths described in terms of
  - delay (25 ns increment, 6.4us max)
  - Doppler (24-bit precision)
  - amplitude (16-bit multiplier)
- I/Os: 10-bit precision complex baseband samples.
- Maximum throughput 40 Msamples/s.
- Single 5V supply. Connectorized 3"x 3" module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom). Interfaces with 5V and 3.3V logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1024.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

Block Diagram



Path 1 is the direct path, and as such represents the reference against which the other paths are described in terms of relative delay and relative frequency offset. The path 1 gain can be set to zero to simulate the absence of line of sight.

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Electrical Interface

Input Interface	Definition
DATA_I_IN[9:0]	In-phase sample. Unsigned 10-bit format
DATA_Q_IN[9:0]	Quadrature sample. Unsigned 10-bit format.
SAMPLE_CLK_IN	Input clock. One CLK-wide pulse. Read the input signals at the rising edge of CLK when SAMPLE_CLK_IN = '1'.
SAMPLE_CLK_IN_REQ	One CLK-wide pulse. Requests a sample from the module upstream. For flow-control purposes.
AGC_PWM_OUT	Output. When this module is connected directly to an external receiver (COM-300x), it generates an digital pulse-width modulated 0 – 3.3V signal to control the gain prior to A/D conversion. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3.3V is the minimum gain.
CLK_IN	Input reference clock for synchronous I/O and processing. Yields internal CLK clock. Typically 40 MHz.

Output Module Interface (Output data pushed out)	Definition
DATA_I_OUT[9:0]	In-phase (real-axis) output sample. 10-bit precision. Format: 2's complement or unsigned as configured by user.
DATA_Q_OUT[9:0]	Quadrature (imaginary axis) output sample. Same format as DATA_I_OUT.
SAMPLE_CLK_OUT	Output clock. One CLK-wide pulse. Read the output signals at the rising edge of CLK when SAMPLE_CLK_OUT = '1'.
SAMPLE_CLK_OUT_REQ	Input. Sample request from the module downstream. For flow control purposes.
DAC_CLK_OUT	Output sampling clock for Digital to Analog Converters.
	DAC reads the output sample at the rising edge.
CLK_OUT	Output reference clock. Same as CLK_IN input clock and CLK internal processing clock. Typically 40 MHz.
Output Module Interface (Output data pulled)	**Definition**
SAMPLE_CLK_REQ_IN	Input. 100 MHz clock requesting output samples.
DATA_OUT[13:0]	Output. Quadrature baseband samples, 14-bit precision, 2's complement format. Bit 13 is the most significant bit. The in-phase (I) and quadrature (Q) samples alternate. Output samples are synchronous with the falling edge of SAMPLE_CLK_REQ_IN.
TX_ENABLE	Output. Transmit enable. Active high. The first sample after TX_ENABLE becomes active is an in-phase (I) sample.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 300mA.

Configuration (via Serial Link / LAN)

Complete assemblies can be monitored and controlled centrally over a single serial or, via adjacent ComBlocks, over LAN, USB, or CardBus connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

This module operates at an internal processing clock rate f_{clk} of 40 MHz.

Parameters	Configuration
Gain1	Path 1 amplitude gain. Expressed as an unsigned floating point number with 0.16 format. Thus, 0xFFFF represents the (near) unity amplitude gain. 0x0000 represents a null amplitude gain. Due to FPGA size limitations, the 5 least significant bits are ignored. REG0: bits 7-0 REG1: bits 15-8
Gain2	Path 2 amplitude gain. Same format. REG2: bits 7-0 REG3: bits 15-8
Gain3	Path 3 amplitude gain. Same format. REG4: bits 7-0 REG5: bits 15-8
Gain4	Path 4 amplitude gain. Same format. REG6: bits 7-0 REG7: bits 15-8
Gain5	Path 5 amplitude gain. Same format. REG8: bits 7-0 REG9: bits 15-8
Delay2	Path 2 delay, expressed as n/f_{clk}, where f_{clk} is the reference clock (typically 40 MHz) and n is an integer in the range 0 to 255. For example, a 3 usec delay is specified as x78. REG10: bits 7-0
Delay3	Path 3 delay, same format as above. REG11: bits 7-0
Delay4	Path 4 delay, same format as above. REG12: bits 7-0
Delay5	Path 5 delay, same format as above. REG13: bits 7-0
Frequency Offset 2	Path 2 frequency offset. The offset is expressed as a signed 2's complement number in the form $f_{offset} / f_{sampling} * 2^{24}$, where $f_{sampling}$ is the sampling frequency (as per the input sampling clock SAMPLE_CLK_IN). REG14: bits 7-0 REG15: bits 15-8 REG16: bits 23-16
Frequency Offset 3	Path 3 frequency offset. REG17: bits 7-0 REG18: bits 15-8 REG19: bits 23-16
Frequency Offset 4	Path 4 frequency offset. REG20: bits 7-0 REG21: bits 15-8 REG22: bits 23-16
Frequency Offset 5	Path 5 frequency offset. REG23: bits 7-0 REG24: bits 15-8 REG25: bits 23-16
Output sample format	0 = unsigned (for example to COM-2001) 1 = 2's complement (for example to COM-4004) REG26 bit 0
Enable AGC	0 = disabled 1 = enabled AGC. REG26 bit 1
Spectrum inversion	Invert Q bit. 0 = off 1 = on REG26 bit 2

Operations

Gain

The gain for each path is represented as a 0.16 unsigned floating point number. For example 0x8000 represents a amplitude gain of 0.5. The user should be aware of the possibility for saturation at the output, even if the sum of all amplitude gain coefficients is less than one.

Output Interfaces

Two distinct output interfaces can be selected at the time of firmware upload:

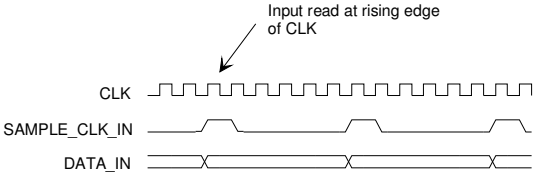
- COM-1024-**A** output data is pushed to the next module (for example to COM-2001, or COM-1001/1012/1018/1027 demodulators).
- COM-1024-**B** output data is pulled by next module (for example by the COM-4004)

These two firmware versions can be downloaded from www.comblock.com/download

Timing

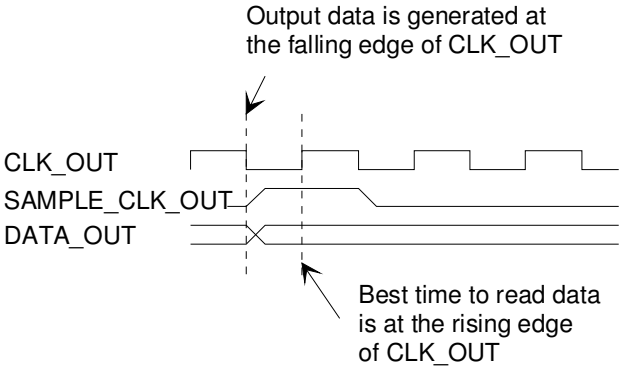
The I/O signals are synchronous with the rising edge of the reference clock CLK[1] (i.e. all signals transitions always occur after the rising edge of the reference clock CLK). The maximum CLK frequency is 40 MHz.

Input



Output

(REG26 bit1 = 0, data is pushed out, CLK=40 MHz)

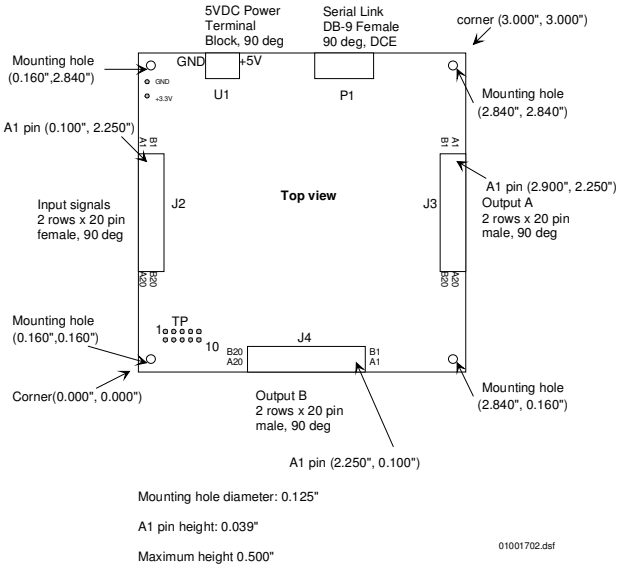


Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
TP1	I-channel most significant bit, input
TP2	I-channel most significant bit, path 1
TP3	I-channel most significant bit, path 2
TP4	I-channel most significant bit, path 3
TP5	I-channel most significant bit, path 4
TP6	I-channel most significant bit, path 5
DONE	FPGA DONE pin. High indicates proper download of the FPGA configuration file.

Mechanical Interface

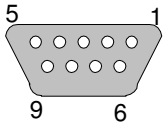


[1] The output timing for the interface with the COM-4004 module is synchronous with an external clock. For details, please refer to the COM-4004 specifications.

Pinout

Serial Link P1

The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.

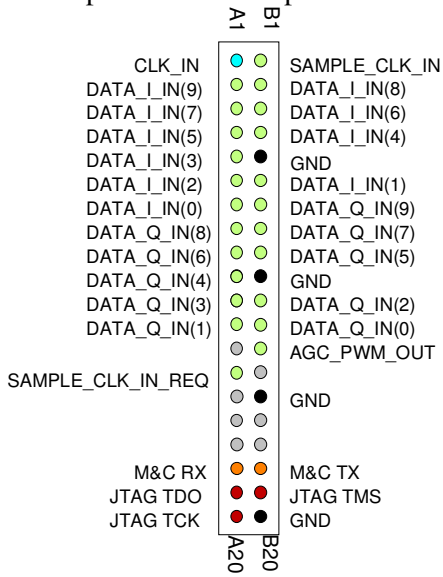


DB-9 Female

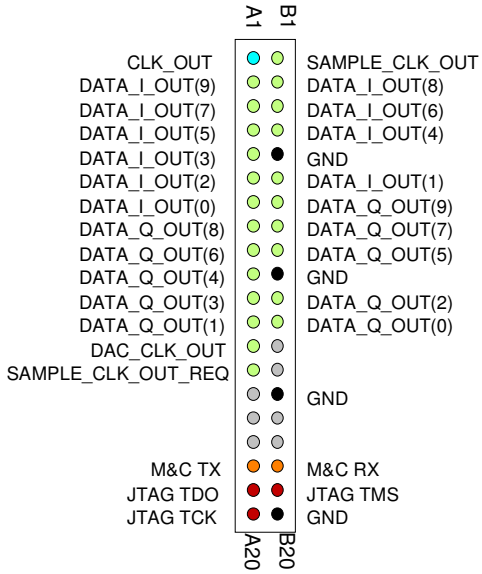
2 Transmit
3 Receive
5 Ground

Input Connector J2

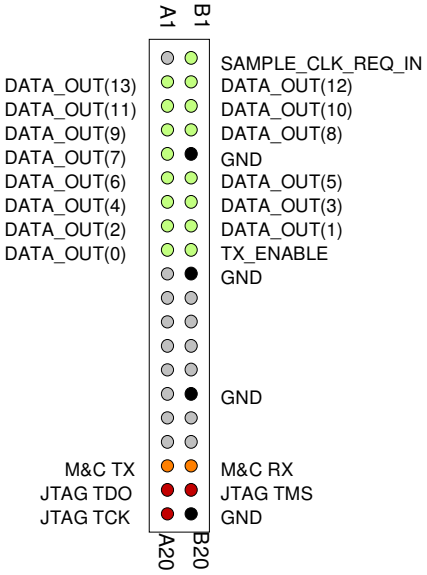
2 x 10-bit sampled baseband input



Output Connectors J3/J4



2 x 10-bit parallel output samples
This connector is used when output data is pushed out (Firmware option **-A**).



2x14-bit multiplexed output samples.
This connector is used when output data is pulled out by the next module (Firmware option **-B**).

I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-1002 BPSK/QPSK/OQPSK modulator	COM-1001 BPSK/QPSK/OQPSK demodulator
COM-1012/19 DSSS modulator	COM-1011/18 DSSS demodulator
COM-1028 FSK/MSK/GFSK/GMSK modulator	COM-1027 FSK/MSK/GFSK/GMSK demodulator
COM-1402 PSK/QAM/APSK modulator	COM-1418 DS spread-spectrum demodulator
COM-3001/2/3/4/5/6/7/8/9 RF/IF/baseband receiver	COM-1202/3 PSK/QAM/APSK demodulator
COM-8001 arbitrary waveform signal generator	COM-2001 Dual D/A converters
	COM-4004 70 MHz IF modulator

Configuration Management

This specification is to be used in conjunction with VHDL software release 6.

The option and version of the FPGA configuration currently active can be read from the ComBlock Control Center in the configuration panel (advanced).

ComBlock Ordering Information

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