COM-1025 8-CHANNEL PRBS-11 & TIME-DIVERSITY GENERATOR

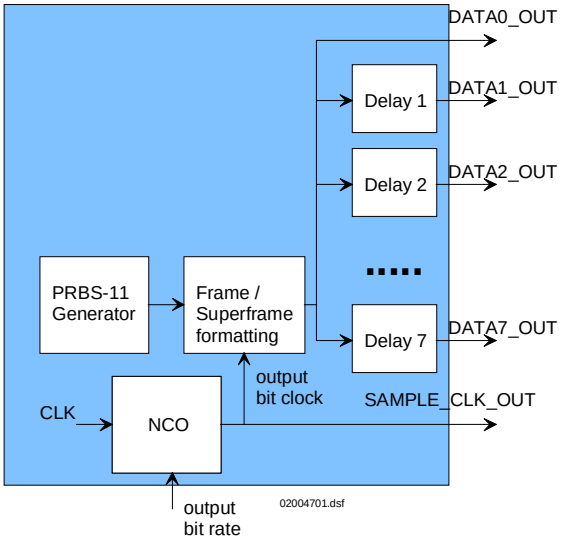
Key Features

- 8-channel pseudo-random binary sequence generator. 2047-bit period.
- 4096-bit frame formatting.
- N-frame long superframe formatting.
- Programmable output clock speed up to 20 Mbit/s.
- Time diversity: generates eight delayed copies of the data stream. Delays are programmable by integer number of superframes.
- Freeware for the COM-1000 module.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1025.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

Block Diagram



Electrical Interface

Input Interface	Definition
CLK_IN	Input reference clock for synchronous I/O and processing. Yields internal CLK clock. Typically 40 MHz.
Output Interface	**Definition**
DATA0_OUT	Output data stream 0. No delay.
DATA1_OUT	Output data stream 1. Programmable delay with respect to DATA0_OUT..
DATA2_OUT	Output data stream 2. Programmable delay with respect to DATA0_OUT..
DATA3_OUT	Output data stream 3. Programmable delay with respect to DATA0_OUT..
DATA4_OUT	Output data stream 4. Programmable delay with respect to DATA0_OUT..
DATA5_OUT	Output data stream 5. Programmable delay with respect to DATA0_OUT..
DATA6_OUT	Output data stream 6. Programmable delay with respect to DATA0_OUT..

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 Issued 10/26/2002

DATA7_OUT	Output data stream 7. Programmable delay with respect to DATA0_OUT..
SAMPLE_CLK_OUT	Output clock. One CLK-wide pulse. Read the output signals at the rising edge of CLK when SAMPLE_CLK_OUT = '1'.
CLK_OUT	Output reference clock. Same as CLK_IN input clock and CLK internal processing clock. Typically 40 MHz.

Configuration (via Serial Link / LAN)

Complete assemblies can be monitored and controlled centrally over a single serial or LAN connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

Parameters	**Configuration**
Internal/External clock	0 = internal 1 = external REG0 bit 0
Enable frame format (unique word insertion)	0 = disabled 1 = enabled REG0 bit 1
Enable superframe format	0 = disabled 1 = enabled REG0 bit 2
Output bit rate	24-bit unsigned expressed as f_{bit_rate} * 2^24 / f_{clk}. f_{clk} is typically 40 MHz. REG1 = bit 7-0 (LSB) REG2 = bit 15 – 8 REG3 = bit 23 – 16 (MSB)
Number of frames per superframe	1,2,4,8,16,32,64 or 128 REG4 bits 7-0
Delay Stream *n*	Time diversity differential delay for stream *n*. Expressed as number of super frames delayed with respect to stream 0. Minimum value is 0, i e, stream 0 is the reference and must never have a delay. Maximum value: 128 super frames. REG5 bits 7-0: stream 1 delay REG6 bits 7-0: stream 2 delay REG7 bits 7-0: stream 3 delay REG8 bits 7-0: stream 4 delay REG9 bits 7-0: stream 5 delay REG10 bits 7-0: stream 6 delay REG11 bits 7-0: stream 7 delay

Monitoring (Serial Link)

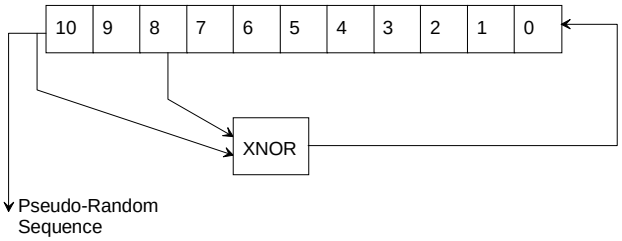
Monitoring registers are read-only.

Parameters	**Monitoring**
Version	Returns '1025x' when prompted for version number.

Specifications

Pseudo-Random Bit Stream

A periodic pseudo-random sequence can be used as modulator source instead of the input data stream. A typical use would be for end-to-end bit-error-rate measurement of a communication link. The sequence is 2047-bit long maximum length sequence generated by a 11-tap linear feedback shift register:



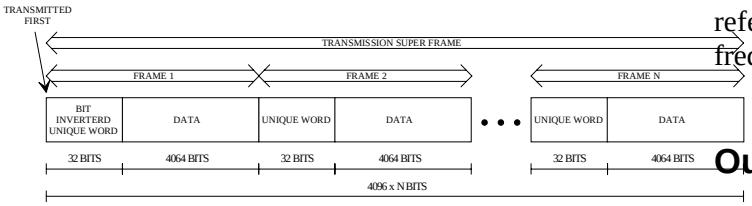
The first 100 bits of the PN sequence are as follows:
0000000000 0111111111 0011111110 0001111100 1100111000 0000010011 1111010001 1110110100 1101001100 0011000001

Frame / Superframe Format

A transmission frame consists of 4096 bits, of which 32 are unique word bit and the remaining 4064 are actual data bits.

A super frame consists of N 4096-bit frames, where N is a variable between 1 and 128. The first unique word in each super frame is the bit inverted version of the regular unique word.

The purpose of the superframe is to help the receiver remove any time ambiguity which occurs when the frame transmission duration is smaller than the propagation delay statistical distribution. Depending on the data rate being transmitted, the user can adjust the superframe duration.



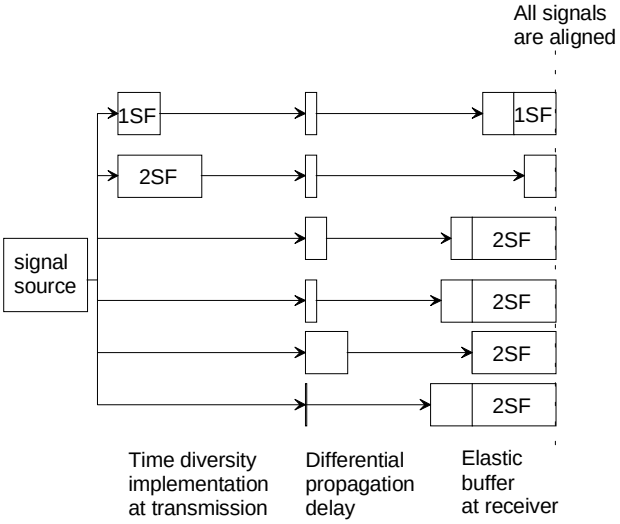
Unique Word

A unique word is used for frame synchronization. The unique word is 32-bit long:
01011010 00001111 10111110 01100110 (binary)
0x 5A 0F BE 66 (hex)
The most significant bit (left-most) is transmitted first.

An inverted version of the unique word is used to identify the start of superframe.

Time-Diversity Delay

In time-diversity system, multiple copies of the same signal are sent over independent transmission channels. The receiver re-synchronize the multiple copies and add them coherently to maximize the signal to noise ratio. This method is illustrated below:

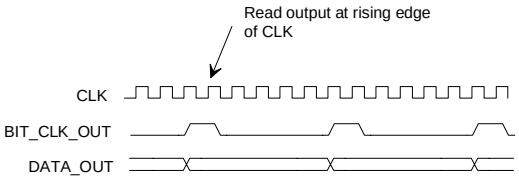


The COM-1025 software generates up to 8 differentially delayed copies. The delay is known, user-programmable and always an integer multiple of superframes.

Timing

The I/O signals are synchronous with the rising edge of the reference clock CLK (i.e. all signals transitions always occur after the rising edge of the reference clock CLK). The maximum CLK frequency is 40 MHz.

Output



Test Points

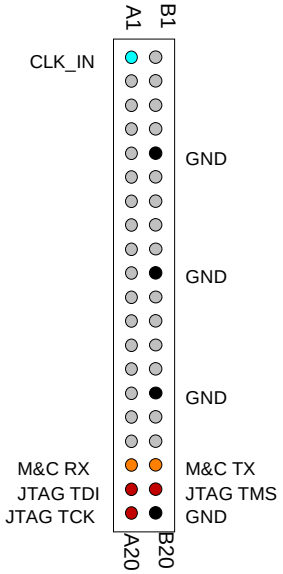
Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
TP1	PRBS-11 sequence, stream 0
TP2	Start of frame pulse, all streams
TP3	Start of superframe, all streams
TP4	Output stream stream 0
TP5	Output stream stream 1
TP6	Output stream stream 2
TP7	Output bit clock, all streams

Pinout

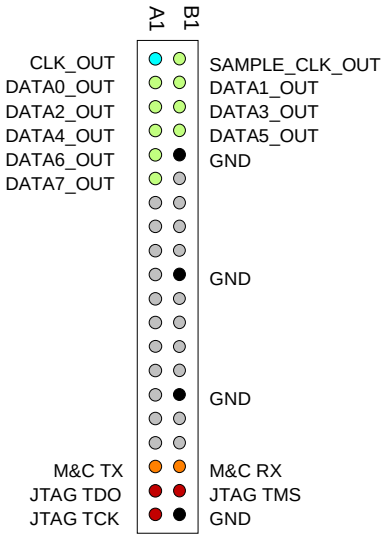
Input Connector

J2 on the COM-1000 module.



Output Connectors

J3/J4 on the COM-1000 module.



I/O Compatibility List

(not an exhaustive list)

Input	Output
	COM-9003 multiplexing connector

ComBlock Ordering Information

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