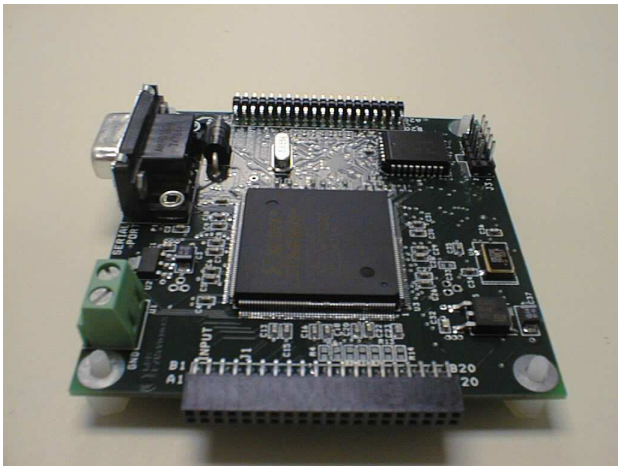
COM-1027 FSK/MSK/GFSK/GMSK DIGITAL DEMODULATOR

Key Features

- Demodulator for continuous phase FSK (CPFSK) and its derivatives:
  - Minimum shift keying (MSK)
  - Gaussian frequency shift keying (GFSK)
  - Gaussian minimum shift keying (GMSK)
- Programmable 2-, 4-, 8-ary FSK
- Programmable modulation index h [0.125 to 4]
- Programmable data rates up to 30/20/10 Mbps. (8-, 4-, 2-ary FSK).
- Coherent demodulator for better BER performances.
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right). Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.



Typical Applications

- GSM:
  - GMSK, modulation index h=0.5, BT = 0.3, bit rate: 270.833 Kbps, channel spacing: 200 KHz
- Bluetooth:
  - GFSK, modulation index h = 0.32, BT = 0.5
- DECT:
  - GFSK, BT = 0.5, bit rate: 1.152 Mbps, channel spacing: 1.728 MHz

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1027.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

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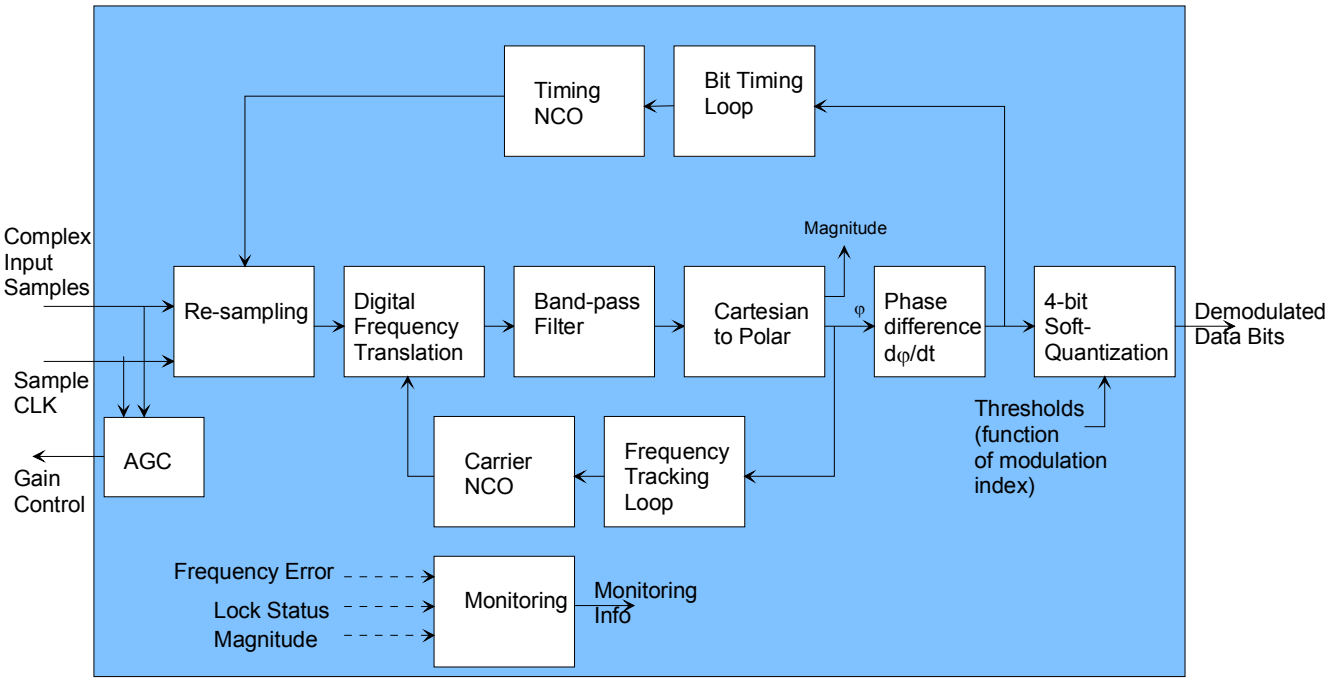
Block Diagram



Electrical Interface

Input Module Interface	Definition
DATA_I_IN[9:0]	Modulated input signal, real axis. 10-bit precision. Format: 2's complement or unsigned. Unused LSBs are pulled low.
DATA_Q_IN[9:0]	Modulated input signal, imaginary axis. 10-bit precision. Same format as DATA_I_IN. Unused LSBs are pulled low.
SAMPLE_CLK_IN	Input signal sampling clock. One CLK-wide pulse. Read the input signal at the rising edge of CLK when SAMPLE_CLK_IN = '1'. The minimum input sampling rate is 8 samples per symbol. Sampling above 16 samples per symbol may cause aliasing whereby adjacent channels may interfere with the main signa. Samples can be consecutive. For example, SAMPLE_CLK_IN can be fixed at '1' to indicate that new input samples are provided once per CLK_IN clock period. Signal is pulled-up.
AGC_OUT	Output. When this demodulator is connected directly to an analog receiver, it generates a pulse-width modulated signal to control the analog gain prior to A/D conversion. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3V is the minimum gain.
CLK_IN	Input reference clock for synchronous I/O. DATA_x_IN and SAMPLE_CLK_IN are read at the rising edge of CLK_IN. Maximum 40 MHz.

Two basic types of output connections are available for user selection:

- direct connection between demodulator and data destination.

- Shared data bus connecting multiple demodulators to a single data destination (for signal diversity combining)

Output Module Interface Direct connection between two ComBlocks, REG8(4) = '0'	**Definition**
DATA_OUT[3:0]	4-bit soft-quantized demodulated bits. The most significant bit DATA_OUT(3) represents the demodulated information bit while the lower 3-bit represent the demodulated bit quality for use by a subsequent error correction decoder. Unsigned representation: 0000 for maximum amplitude '0', 1111 for maximum amplitude '1'.
BIT_CLK_OUT	Demodulated bit clock. One CLK-wide pulse. Read the output signal at the rising edge of CLK when BIT_CLK_OUT = '1'.
RX_LOCK	'1' when the demodulator is locked, '0' otherwise.
CLK_OUT	40 MHz output reference clock. Generated by dividing the internal processing clock: f_{clk} /2

Output Module Interface Shared bus, REG8(4) = '1'	**Definition**
BUS_CLK_IN	40 MHz input reference clock for use on the synchronous bus.
BUS_ADDR[3:0]	Bus address. Input (since this module is a bus slave). Designates which slave module is targeted for this read transaction. Read at the rising edge of BUS_CLK_IN
BUS_RWN	Read/Write#. Input (since this module is a bus slave). Indicates whether a read (1) or write (0) transaction is conducted. Read at the rising edge of BUS_CLK_IN. Read and Write refer to the bus master's perspective.
BUS_DATA[15:0]	Bi-directional data bus. Input when BUS_RWN='0'. Output when BUS_RWN='1'. Read latency is 2 BUS_CLK_IN periods. Minimum read cysle is 3 BUS_CLK_IN periods. Reading can be continuous. Functional definition during read: • bit 0 BIT_CLK_OUT. '1' when DATA_I_OUT is available • bits(4:1) DATA_I_OUT[3:0] demodulated data stream. • bit 5 RX_LOCK. • bits(15:6) undefined.

Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the symbol clock rate (f_{symbol_clk}). The maximum power consumption is 650mA.

Important: I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- Asynchronous serial (DB9)

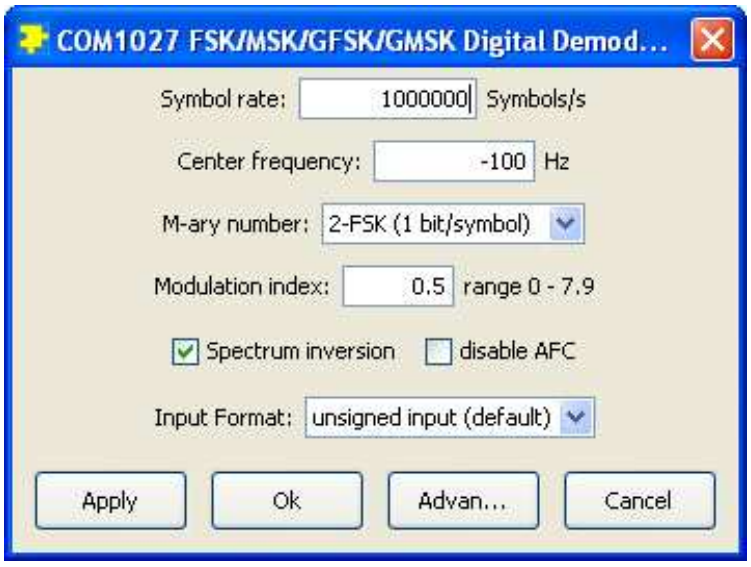
or connections via adjacent ComBlocks:

- USB
- TCP-IP/LAN,
- Asynchronous serial (DB9)
- PC Card (CardBus, PCMCIA).

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1027 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1027 module to be configured, next click the *Settings* button to display the *Settings* window shown below.



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center "Advanced" configuration or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

This module operates at an internal processing clock rate $\mathbf{f_{clk}}$ of 80 MHz.

Most processing is done at the sampling rate / $\mathbf{f_{sample\_clk}}$ = 8 * symbol rate.

In the definition below, a few control register bits may be undefined to maintain backward compatibility with previous versions. They can be ignored by the user when using the latest firmware release.

Parameters	Configuration
Symbol rate (f_{symbol_clk})	24-bit signed integer expressed as fsymbol rate * 2^{24} / $\mathbf{f_{clk}}$. The maximum symbol rate is 10 Msymbols/s (0x1FFFFF). The data rate is 1x, 2x or 3x the symbol rate depending on the M-ary number set in REG8. REG0 = bit 7-0 (LSB) REG1 = bit 15 – 8 REG2 = bit 23 – 16 (MSB)
Center frequency ($\mathbf{f_c}$)	Nominal center frequency. This value is substracted from the received signal actual center frequency. 24-bit signed integer (2's complement representation) expressed as $\mathbf{f_c}$ * 2^{24} / (8*f_{symbol_clk}) Safe range to avoid aliasing: +/- 2 * f_{symbol_clk} Note: the definition of the center frequency is different for the COM-1028 modulator and this demodulator. REG3 = bits 7 – 0 REG4 = bits 15 – 8 REG5 = bits 23 – 16

Inverse Modulation Index **1/h**	1/(Modulation index **h**). Format 8.8 Thus, 0x0200 represents the inverse of a modulation index of 0.5. (MSK or GMSK modulation imply h = 0.5). Valid range for **1/h**: 0.125 – 4 REG6: bits 7:0 LSB REG7: bit 15:8: MSB
M-ary number	Size of the symbol alphabet: 00 = 2-ary, 2-FSK, M=2 01 = 4-ary, 4-FSK, M=4 10 = 8-ary, 8-FSK, M=8 REG8 bits 1-0
Input sample format	0 = 2's complement 1 = unsigned In particular, all COM-300x receivers generate samples with unsigned format. REG8 bit 2
Spectrum inversion	Whenever the received spectrum has been inverted during the frequency up and down-conversions, this bit should be set. In particular, spectrum inversion occurs in most COM-300x receiver modules. 0 = off, 1 = on REG8 bit 3
Point-to-point vs shared bus output	Controls whether the output connection is point-to-point or multipoint-to-point over a shared data bus (via a COM-9003 multiplexing connector for example). The J4 output connector pinout is affected by this control bit. 0 = direct connection. Point to point. 1 = shared data bus. REG8 bit 4
Disable AFC	New in Rev 8 Disabling the AFC may be needed in some cases (e.g. when the bit stream is not balanced between zeros and ones). 0 = AFC is on 1 = AFC is disabled REG8 bit 5
Squelch enable	New in Rev 8 The squelch circuit forces the demodulator output to '1' (UART stop bit) when the demodulated signal is too weak. This feature is useful when demodulating a good-quality 2-FSK signal carrying asynchronous UART characters. 0 = Squelch is disabled 1 = Squelch is enabled REG8 bit 6
Freeze monitoring data	As the monitoring data is constantly changing, it is important to be able to prevent changes while reading a multi-byte parameter. Write a zero in bit 7 to freeze the monitoring data prior to reading it. Write a one to re-enable the update. REG8 bit 7
Bus address	Unique 4-bit address identifying this module on the output bus (if the output bus is enabled in REG8 bit 4). Ignore otherwise. This module acts as bus slave: it performs the read transaction requested by the bus master if and only if the bus address matches its own address defined here. This address must be unique among modules connected to the same bus in order to avoid conflicts. REG9 bits 3-0

Baseline configurations can be found at www.comblock.com/tsbasic_settings.htm and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

Status Registers

Digital status registers are read-only.

Parameters	Monitoring
Carrier frequency offset (fcdelta)	Residual frequency offset with respect to the nominal carrier frequency. 24-bit signed integer (2's complement) expressed as fcdelta * 2^{24} / (8*fsymbol rate). REG12 = bit 7 – 0 REG13 = bit 15 – 8 REG14 = bit 23 – 16
Received signal magnitude after channel filtering	8-bit unsigned REG15 bit 7-0.
AFC lock status	0 = unlocked 1 = locked REG16 bit 0
Signal power detection	0 = below threshold 1 = signal power detection REG16 bit 1

Test Points

Test points are provided for easy access by an oscilloscope probe at the J4 male connector.

Test Point	Definition
J4/A7	AFC lock status (1 = locked, 0 = unlocked)
J4/B7	Signal power detection (1 = signal power presence detected , 0 = signal power below threshold)
J4/A8	Recovered carrier (carrier NCO output MSB)
J4/B8	Recovered bit timing Compare with modulator bit timing.
J4/A9	Saturation condition detected at input samples DATA_I_IN or DATA_I_Q.
J4/B9	Internal 80 MHz clock

ComScope Monitoring

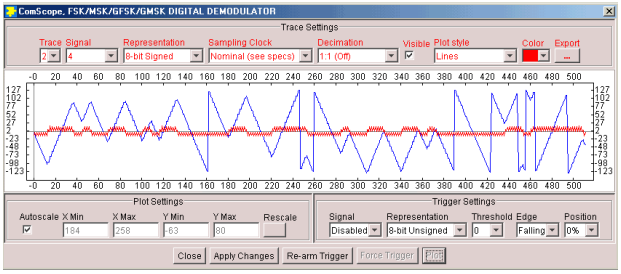
Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-1027 signal traces and trigger are defined as follows:

Trace 1 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Input I signal	8-bit signed or unsigned. (8MSB/10)	Input sampling rate	512
2: Cartesian-to-Polar conversion: phase	8-bit signed (8MSB/10)	8 samples /symbol	512
3: Cartesian-to-Polar conversion: magnitude	8-bit signed (8MSB/14)	8 samples /symbol	512
4: Filtered Phase difference at optimum sampling instant	8-bit signed (8MSB/13)	1 sample /symbol	512
5: Recovered carrier frequency offset. Resolution is fsymbol/32.	8-bit signed (8MSB/24)	8 samples /symbol	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: Input Q signal	8-bit signed or unsigned. (8MSB/10)	Input sampling rate	512
2: front-end AGC	8-bit unsigned (8MSB/10)	f_{clk} (80 MHz)	512
3: I signal after elastic buffer, interpolation and resampling at 8 samples/symbol	8-bit signed (8MSB/12)	8 samples /symbol	512
4: Phase difference	8-bit signed (8MSB/10)	8 samples /symbol	512
5: Recovered phase, after scaling for modulation index (i.e. prior to soft quantization)	8-bit signed (8MSB/14)	1 samples /symbol (optimum sampling instant)	512
Trigger Signal	**Format**		
1: AFC lock status	Binary		
2: Signal power detection	Binary		

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the $\mathbf{f_{clk}}$ processing clock as real-time sampling clock.

In particular, selecting the $\mathbf{f_{clk}}$ processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope Window Sample: showing GMSK demodulated phase (blue) and reconstructed unfiltered symbols (red).

Operation

FSK Modulation

The FSK modulation and its derivatives (CPFSK, MSK, GMSK, GFSK) are best described by the following equations for the modulated signal s(t). The first equation describes a phase modulator, with the modulated centered around the center frequency f_c.

$$s(t) = \sqrt{\frac{2E_s}{T}}.\cos(2\pi f_c t + \theta(t) + \theta_0)$$

where

- E_s is the energy per symbol
- T is the symbol period
- f_c is the center frequency
- $\theta(t)$ is the phase modulation

The COM-1027 implements a continuous phase FSK demodulator. It assumes that there are no phase discontinuities between symbols. The CPFSK phase modulation can be described as:

$$\theta(t) = \frac{\pi h}{T}\int_0^t a_i(t)dt$$

where:

- h is the modulation index. A modulation index of 0.5 yields a maximum phase change of $\pi/2$ over a symbol.

a_i are the symbols. With 2-FSK, the binary data is represented as –1 (for '0') and +1 (for '1').

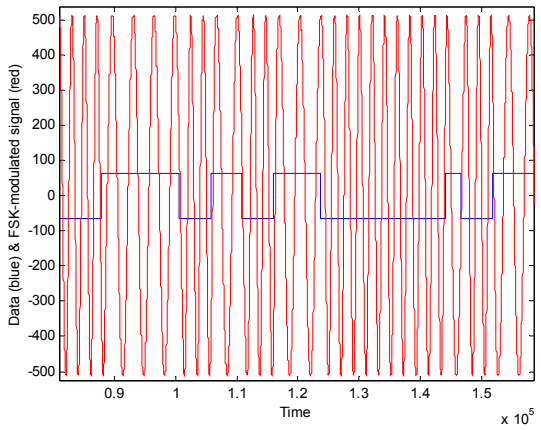
M-ary Number M

The transmitted data is grouped into symbols of size 1, 2, or 3 consecutive bits. The size of the symbol alphabet is thus M = 2, 4 or 8. The symbol MSB is sent first to the DATA_OUT output.

The mapping between modulation symbol a_i and symbol alphabet is described in the table below:

Modulation symbol a_i	Symbol alphabet
-1	2-FSK '0'
+1	2-FSK '1'
-3	4-FSK "00"
-1	4-FSK "01"
+1	4-FSK "10"
+3	4-FSK "11"
-7	8-FSK "000"
-5	8-FSK "001"
-3	8-FSK "010"

-1	8-FSK “011”
+1	8-FSK “100”
+3	8-FSK “101”
+5	8-FSK “110”
+7	8-FSK “111”



Continuous FSK modulated signal example

FSK modulation is sometimes characterized by the frequency separation between symbols. The relationship between modulation index h and frequency separation is $f_{separation} = 0.5\ h\ f_{symbol\_clk}$

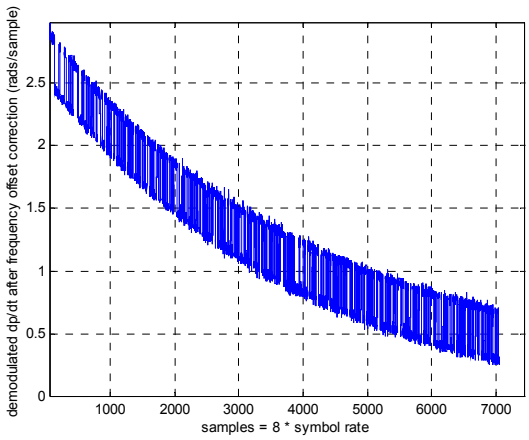
Frequency Acquisition and Tracking

The demodulator comprises an automatic frequency control (AFC) loop to acquire and track the residual frequency offset of the modulated signal.

The tracking range $f_{tracking}$ is bound by the following constraints:
$abs(\mathbf{f_{tracking}}/(4* \mathbf{f_{symbol\_clk}})) + \mathbf{h}/8 < 1$

For example, if the modulation index **h** is 0.5, the maximum tracking range is ± 3.75 $\mathbf{f_{symbol\_clk}}$. We recommend an additional 10% implementation margin.

The AFC response time is illustrated below for an initial frequency offset of (3.37* $\mathbf{f_{symbol\_clk}}$) and modulation index h = 0.5.



AFC response to input frequency step

An AFC lock status is provided in status register REG16 and at a test point. AFC lock is declared when the residual frequency error is below 1/16th of the symbol rate.

Bit Timing Tracking

A first order loop is capable of acquiring and tracking bit timing differences between the transmitter and the receiver, up to ± 500 ppm.

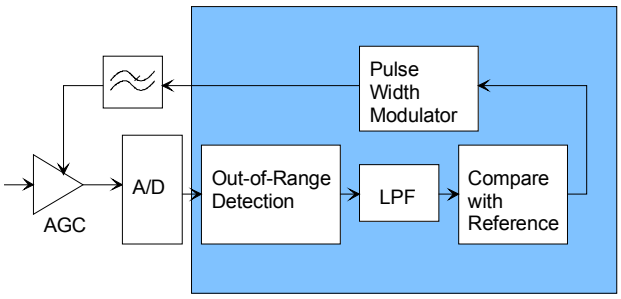
AGC

The purpose of this AGC is to prevent saturation at the external A/D converter(s) while making full use of the 10-bit A/D converter dynamic range. The principle of operations is outlined below:

(a) out-of-range at the A/D converter is detected. An out-of-range condition occurs if the quantized A/D samples are equal to either “1111111111” or “0000000000”.

(b) The AGC will adjust the analog circuitry gain so that out-of-range conditions do not occur more than 1 in 64 samples in the average.

(c) The resulting gain control signal is a pulse-width modulated (PWM) signal with 10-bit precision.



AGC principle

The analog circuit shall filter this 3.3V low-voltage TTL PWM signal with a low-pass filter prior to controlling the analog gain. The PWM is randomized and its spectral distribution shifted to the higher frequencies so as facilitate the analog low-pass filter design.

The AGC loop bandwidth is typically 1 Hz when used in conjunction with COM-30xx receivers and a 40 MHz processing clock. The loop response time is assymetrical: it responds faster to a saturation condition than to a 'low signal' condition.

The gain control signal will increase if too many out-of-range conditions occur.

Implementation

The incoming samples are first stored in an elastic buffer to switch between the input clock (CLK_IN, up to 40 MHz) and the internal processing clock (CLK, $\mathbf{f_{clk}}$ = 80 MHz). All subsequence signal processing is performed at a clock rate $\mathbf{f_{clk}}$ of 80 MHz.

The incoming In-phase (I) and quadrature (Q) samples are subsampled at a rate of 8 samples per symbol under the control of the bit timing NCO.

The signal center frequency is then translated to zero to compensate for known ($\mathbf{f_c}$) and unknown frequency offsets. The known frequency offset $\mathbf{f_c}$ is under user control by means of the control registers REG3/4/5. Unknown frequency offsets are detected by the carrier tracking loop.

The resulting signal undergoes channel filtering to reject the out-of-band noise.

The coordinates for the filtered complex signal are converted from Cartesian (I,Q) to Polar (|A|, φ).

Differentiation dφ/dt reveals the modulated symbols and any residual frequency offset .

The Automatic Frequency Control (AFC) loop accumulates the differentiated phase dφ/dt. The resulting sum is used to control the carrier NCO as a first order loop. The key underlying assumption is that the transmitted data is random and balanced, i.e. contains an equal number of 0's and 1's.

Timing

Clocks

An 80 MHz internal clock $\mathbf{f_{clk}}$ is generated by frequency doubling of the 40 MHz oscillator installed on the COM-1027 board. $\mathbf{f_{clk}}$ is <u>not</u> related to the CLK_IN clock. $\mathbf{f_{clk}}$ is used for internal processing and for generating the output clock CLK_OUT = $\mathbf{f_{clk}}$ /2.

Input data DATA_IN is first written into an input elastic buffer at the rising edge of CLK_IN when SAMPLE_CLK_IN = '1'.

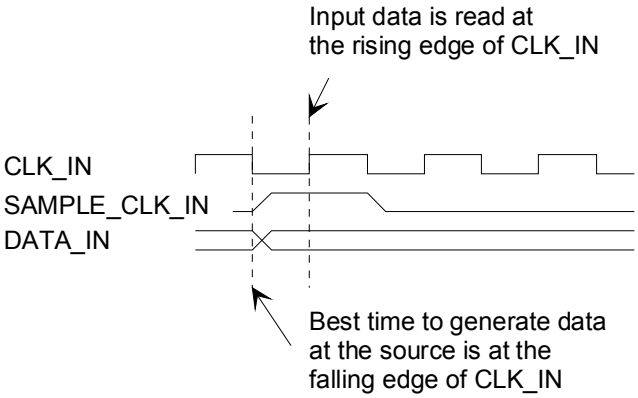
The data is read out of the input elastic buffer at the symbol rate * 1 (2-ary FSK), * 2 (4-ary FSK) or * 3 (8-ary FSK).

The input buffer size is 256 symbols.

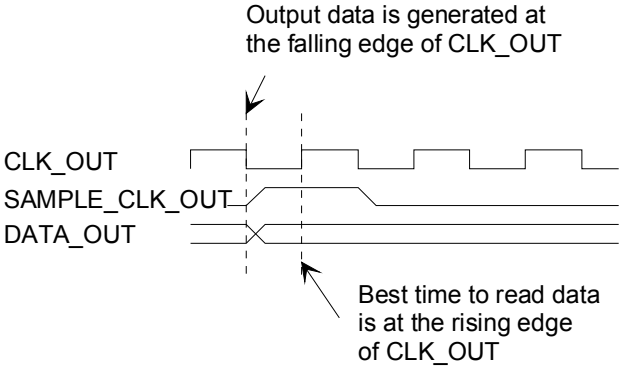
I/Os

All I/O signals are synchronous with the rising edge of the reference clock CLK_IN or CLK_OUT (i.e. all signals transitions always occur after the rising edge of clock). The maximum frequency for CLK_IN is 40 MHz. The frequency for CLK_OUT is fixed at 40 MHz ($\mathbf{f_{clk}}$ /2) .

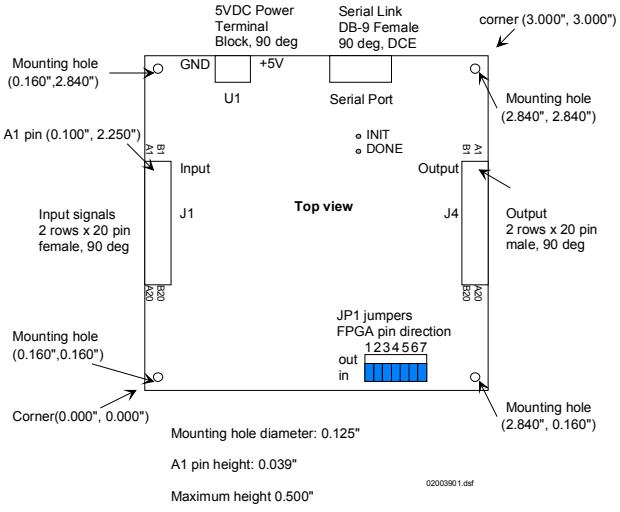
Input



Output



Mechanical Interface

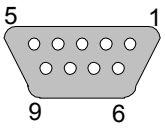


Note: All seven JP1 jumpers must be in the 'IN' location.

Pinout

Serial Link P1

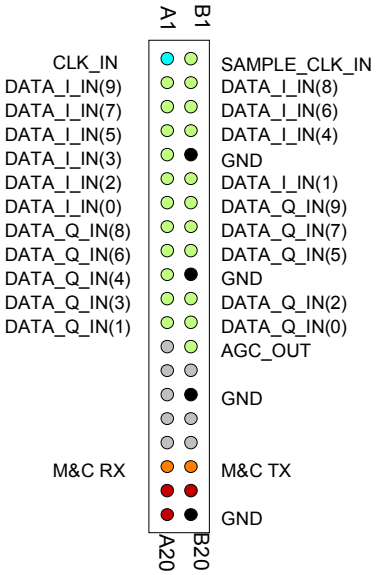
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



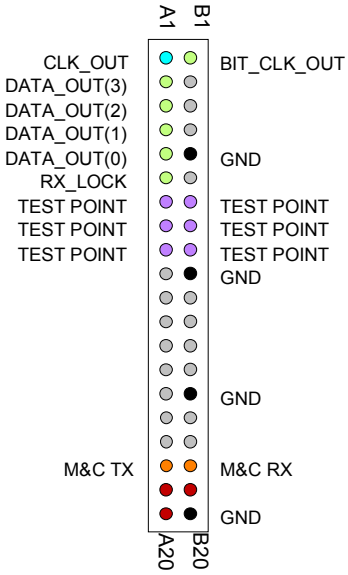
DB-9 Female

2 Transmit
3 Receive
5 Ground

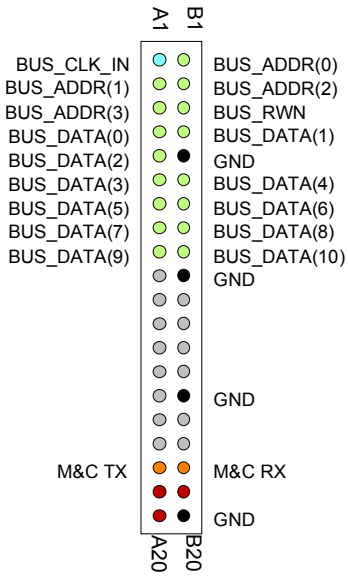
Input Connector J1



Output Connector J4



This connector is used for point-to-point (i.e. direct) connection between two ComBlocks when control register REG8(4) = '0'.



This connector is used for multipoint-to-point connection over a shared data bus when control register REG8(4) = '1'. COM-1027 is a bus slave. It always listens to BUS_CLK_IN, BUS_ADDR, BUS_RWN.

I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-300x RF receivers	COM-1005 Bit Error Rate Measurement
COM-1008 variable decimation	COM-7001 Turbo code decoder
COM-1028 FSK/MSK/GFSK/GMSK digital modulator (back to back)	COM-1009 Convolutional decoder K=7, 5
COM-1023 BER generator, AWGN generator	COM-1209 LDPC + long BCH error correction decoder
COM-1024 Multipath simulator.	COM-5003 TCP-IP / USB Gateway

Configuration Management

This specification is to be used in conjunction with VHDL software revision 8.

It is possible to read back the option and version of the FPGA configuration currently active. Using the ComBlock Control Center, highlight the COM-1027 module, then go to the advanced settings. The option and version are listed at the bottom of the configuration panel.

ComBlock Ordering Information

COM-1027
FSK/MSK/GFSK/GMSK digital demodulator

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