



# COM-1027 FSK/MSK/GFSK/GMSK DIGITAL DEMODULATOR VHDL SOURCE CODE OVERVIEW

## Overview

The COM-1027 ComBlock Module comprises two pieces of software:

- VHDL code to run within the FPGA for all signal processing functions.
- C/Assembly code running within the Atmel AT90S8515 or ATmega8515L microprocessor for non application-specific monitoring and control functions.

The VHDL code interfaces to the monitoring and control functions by exchanging byte-wide registers on the Atmel microcontroller 8-bit data bus. The control and monitoring registers are defined in the specifications [1].

The COM-1027 VHDL code runs on the generic COM-8000 hardware platform. The schematics [2] for this platform are available in this CD.

The Atmel microprocessor code is generic (i.e. non application specific), not user-programmable and functionally transparent to the user. It is thus not described here.

## Reference documents

[1] specifications: com1027.pdf

[2] hardware schematics: com\_8000schematics.pdf

[3] VHDL source code in directory  
com-1027\_003\src

[4] .ucf constraint file  
com-1027\_003\src\root\_demod.ucf

[5] .mcs FPGA bit file  
com-1027\_003\com1027\_003.mcs

[6] Xilinx project file  
com-1027\_003\com1027.npl

## Configuration Management

The current software revision is 3.

## Configuration Options

No option.

## VHDL development environment

The VHDL software was developed using the Xilinx ISE 4.1 development environment. The synthesis tool is FPGA Express 3.6.

## Target FPGA

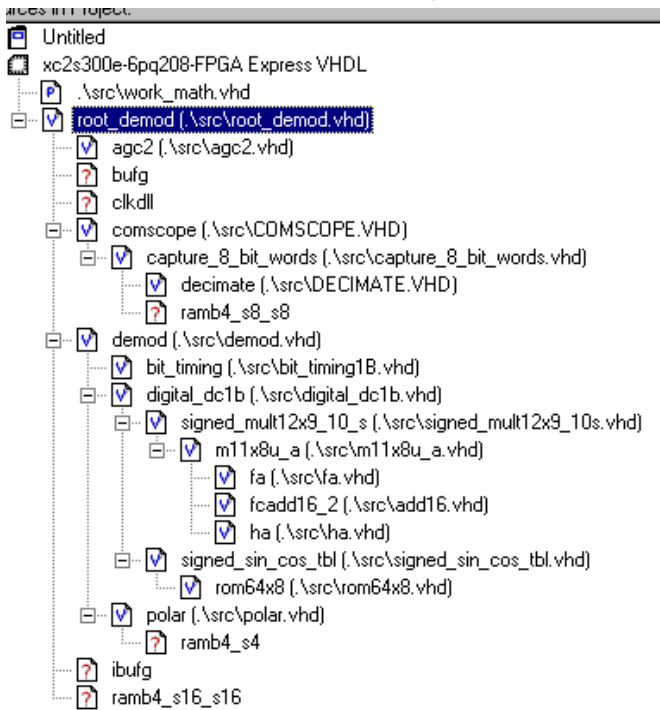
The VHDL code was synthesized for the Xilinx Spartan-IIe XC2S300E-6PQ208 FPGA.

## Xilinx-specific code

The VHDL source code was written in generic VHDL with few Xilinx primitives. No Xilinx CORE is used. The Xilinx primitives are:

- BUFG
- IBUFG
- CLKDLL
- RAMB4\_S8\_S8
- RAMB4\_S16\_S16
- RAMB4\_S4

# VHDL software hierarchy



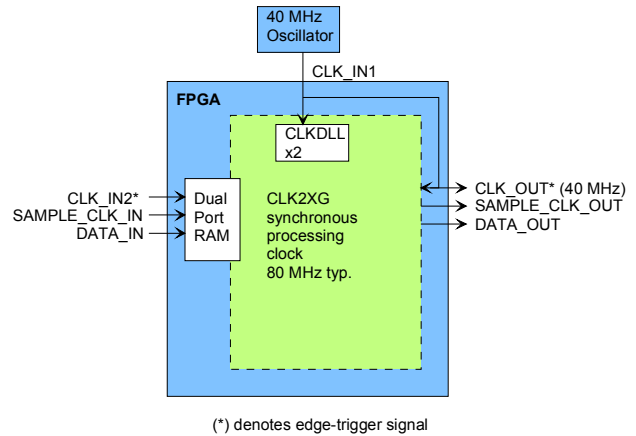
The code is stored with one, and only one, entity per file as shown above.

The root program (highlighted) is *root\_demod.vhd*.

## Clock / Timing

The software uses two different clocks:

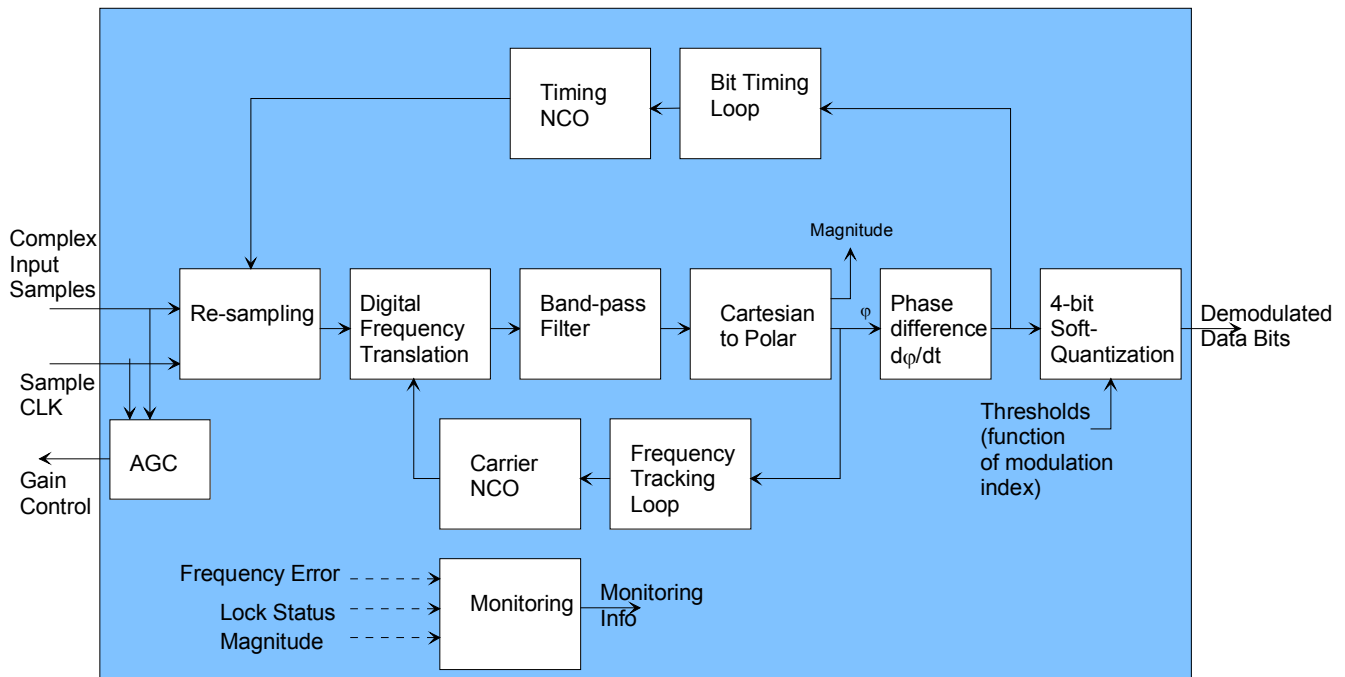
- external clock CLK\_IN2 which serves synchronous clock for the input data stream.
- CLK\_IN1 is generated by a 40 MHz oscillator on the COM-1027 module. It is used as reference for the output clock and for the double-frequency processing clock. The code is written to meet the timing requirements on the target FPGA at a speed of at least 80 MHz.



The hierarchical nature of the VHDL code reflects the block diagram below:

- *root\_demod* is the root program which includes the demodulator *demod*, the analog AGC *agc2* to prevent saturation at the external A/D converters and ancillary functions such as monitoring and control functions (interface with microprocessor) and *comscope* to capture and display internal signals.
- the main FSK demodulation functions are encapsulated within *demod*.
- the frequency translation is implemented within *digital\_dc1b*. The frequency translation is realized in the form of a complex vector rotation, using sine/cosine lookup tables (*signed\_sin\_cos\_tbl*) and pipeline multipliers (*signed\_mult12x9\_10\_s*) made of half adders *ha* and full adders *fa*.
- the Cartesian to polar coordinates conversion is implemented in the *polar* component.

## Demodulator Block Diagram



## FPGA Occupancy

### Design Summary

```

Number of errors:      0
Number of warnings:   18
Number of Slices:     1,682 out of 3,072  54%
Number of Slices containing
  unrelated logic:    0 out of 1,682  0%
Number of Slice Flip Flops:  1,758 out of 6,144  28%
Total Number 4 input LUTs:  2,450 out of 6,144  39%
  Number used as LUTs:      2,362
  Number used as a route-thru: 88
Number of bonded IOBs:    49 out of 142  34%
  IOB Flip Flops:         34
Number of Block RAMs:    8 out of 16  50%
Number of GCLKs:         4 out of 4  100%
Number of GCLKIOBs:     4 out of 4  100%
Number of DLLs:         1 out of 4  25%
Total equivalent gate count for design: 171,620
Additional JTAG gate count for IOBs: 2,544
  
```

## Contact Information

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