COM-1028 FSK/MSK/GFSK/GMSK DIGITAL MODULATOR

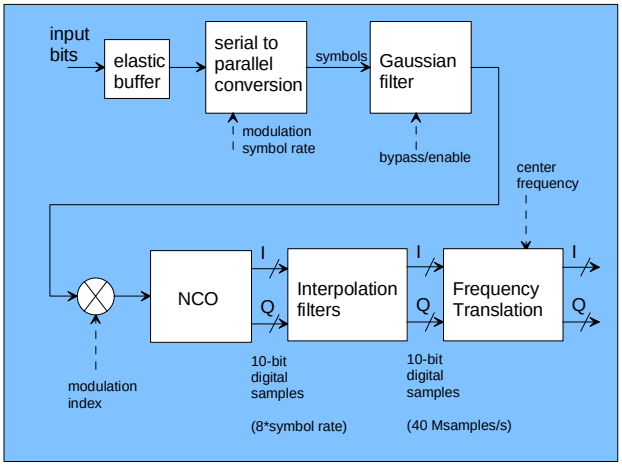
Key Features

- Modulations:
  - Continuous phase FSK (CPFSK)
  - Minimum shift keying (MSK)
  - Gaussian frequency shift keying (GFSK)
  - Gaussian minimum shift keying (GMSK)
- Programmable 2-, 4-, 8-ary FSK
- Programmable modulation index h.
- Two selectable Gaussian filter BT product: 0.5 and 0.3.
- Programmable data rates up to 30/20/10 Mbps. (8-, 4-, 2-ary FSK)
- Internal generation of pseudo-random bit stream and unmodulated carrier for test purposes.
- On-board or external clock selection.
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right). Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1028.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.html .

Block Diagram



Typical Applications

- GSM:
  - GMSK, modulation index h=0.5, BT = 0.3, bit rate: 270.833 Kbps, channel spacing: 200 KHz
- Bluetooth:
  - GFSK, modulation index h = 0.32, BT = 0.5
- DECT:
  - GFSK, BT = 0.5, bit rate: 1.152 Mbps, channel spacing: 1.728 MHz

MSS • 18221-A Flower Hill Way • Gaithersburg, Maryland 20879 • U.S.A.
Telephone: (240) 631-1111 Facsimile: (240) 631-1676 www.ComBlock.com
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Electrical Interface

Two basic types of input connections are available for user selection:

- direct connection between data source and modulator.
- single data source to multiple modulators over a shared bus.

Input Module Interface Direct connection between two ComBlocks, REG10(7) = '0'	**Definition**
DATA_IN	Input data stream.
SAMPLE_CLK_IN	Input bit clock. One CLK-wide pulse. Read the input signals at the rising edge of CLK when SAMPLE_CLK_IN = '1'.
SYMBOL_CLK_IN	Optional input symbol clock. '1' identifies the first bit in a symbol. If not used, the symbol boundaries are automatically (internally) generated every 1 (2-FSK), 2 (4-FSK) or 3 (8-FSK) bits.
SAMPLE_CLK_IN_REQ	Output. One CLK-wide pulse. Requests a data bits from the module upstream. For flow-control purposes.
CLK_IN	Input reference clock for synchronous I/O. DATA_IN, SAMPLE_CLK_IN and SYMBOL_CLK_IN are aread at the rising edge of CLK_IN. Maximum 40 MHz.

Input Module Interface Bus connection, REG10(7) = '1'	**Definition**
BUS_CLK_IN	40 MHz input reference clock for use on the synchronous bus.
BUS_ADDR[3:0]	Bus address. Input (since this module is a bus slave). Designates which slave module is targeted for this read or write transaction. All 1's indicates that the write data is to be broadcasted to all receiving slave modules. Read at the rising edge of BUS_CLK_IN
BUS_RWN	Read/Write#. Input (since this module is a bus slave). Indicates whether a read (1) or write (0) transaction is conducted. Read at the rising edge of BUS_CLK_IN. Read and Write refer to the bus master's perspective.
BUS_DATA[15:0]	Bi-directional data bus. Input when BUS_RWN='0'. Output when BUS_RWN='1'. Read data latency is 2 clock periods after the read command. Functional definition during write: • bit 0 SAMPLE_CLK_IN. '1' when DATA_IN is available • bit 1 DATA_IN data stream to modulator. • bit 2 SYMBOL_CLK_IN • bits(15:3) undefined Functional definition during read: • bit 0 SAMPLE_CLK_IN_REQ requests data from the source. Used for flow control. • bits(15:1) undefined

Output Module Interface (Output data pushed out)	**Definition**
DATA_I_OUT[9:0]	Modulated output signal, real axis. 10-bit precision. Format: 2's complement or unsigned, selected by configuration bit 1.
DATA_Q_OUT[9:0]	Modulated output signal, imaginary axis. 10-bit precision. Same format as DATA_I_OUT.
SAMPLE_CLK_OUT	Output signal sampling clock. Read the output signal at the rising edge of CLK when SAMPLE_CLK_OUT = '1'. SAMPLE_CLK_OUT is fixed at '1' when the modulator is enabled. Fixed at '0' otherwise.
DAC_CLK_OUT	Output sampling clock for Digital to Analog Converters. DAC reads the output sample at the rising edge.
CLK_OUT	40 MHz output reference clock. Generated by dividing the internal processing clock: f_{clk} /2

Output Module Interface (Output data pulled)	Definition
SAMPLE_CLK_REQ_IN	Input. 100 MHz clock requesting output samples.
DATA_OUT[13:0]	Output. Quadrature baseband samples, 14-bit precision, 2's complement format. Bit 13 is the most significant bit. The in-phase (I) and quadrature (Q) samples alternate. Output samples are synchronous with the falling edge of SAMPLE_CLK_REQ_IN.
TX_ENABLE	Output. Transmit enable. Active high. The first sample after TX_ENABLE becomes active is an in-phase (I) sample.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption is 650mA.

Important: I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- Asynchronous serial (DB9)

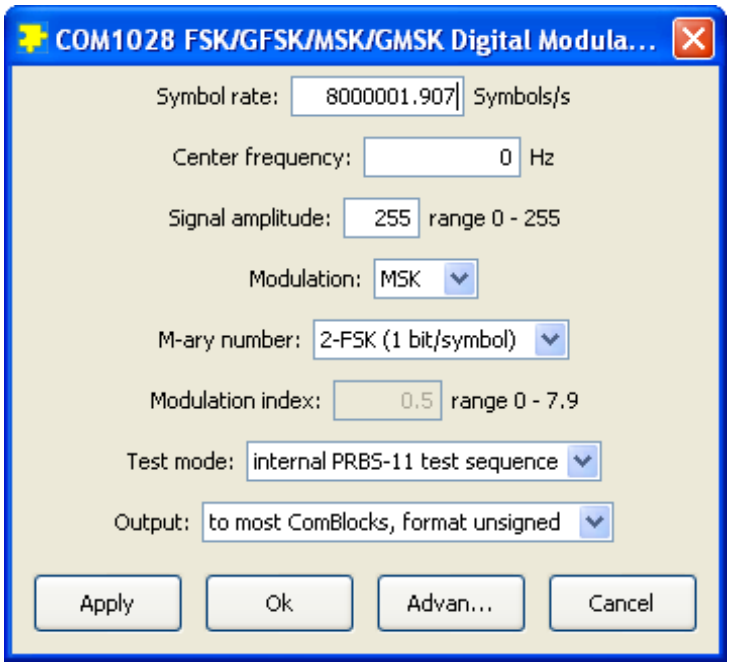
or connections via adjacent ComBlocks:

- USB
- TCP-IP/LAN,
- Asynchronous serial (DB9)
- PC Card (CardBus, PCMCIA).

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1028 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1028 module to be configured, next click the *Settings* button to display the *Settings* window shown below.



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center "Advanced" configuration or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Definitions for the Control registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

This module operates at an internal processing clock rate $\mathbf{f_{clk}}$ of 80 MHz.

Most processing is done at the sampling rate / $\mathbf{f_{sample\_clk}}$ = 8 * symbol rate.

In the definition below, a few control register bits may be undefined to maintain backward compatibility with previous versions. They can be ignored by the user when using the latest firmware release.

Parameters	Configuration
Symbol rate (f_{symbol_clk})	24-bit signed integer expressed as fsymbol rate * 2^{24} / $\mathbf{f_{clk}}$. The maximum symbol rate is 10 Msymbols/s (0x1FFFFF). The data rate is 1x, 2x or 3x the symbol rate depending on the M-ary number set in REG9. REG0 = bits 7-0 (LSB) REG1 = bits 15 – 8 REG2 = bits 23 – 16 (MSB)
Center frequency (f_c)	24-bit signed integer (2's complement representation) expressed as f_c * 2^{24} / $\mathbf{f_{clk}}$. Valid range: +/- 20 MHz. (+/- 10 MHz for flat gain with COM-2001 D/A converter). REG3 = bits 7 – 0 REG4 = bits 15 – 8 REG5 = bits 23 - 16
Signal gain	Signal level. 8-bit unsigned integer. Applies equally to the I and Q channels. We recommend a maximum settings of 0x80 to avoid saturation in the subsequent digital-to-analog conversion module (COM-2001, COM-4004, etc). REG6 = bits 7-0
Modulation Index h	Modulation index h. Format 3.8 Thus, 0x0080 represents an index of 0.5. Ignored if MSK or GMSK modulation is selected (MSK implies h = 0.5). Valid range: 0 – 7.996 REG7: bits 7:0 LSB REG8: bits 10:8: MSB
M-ary number	Size of the symbol alphabet: 00 = 2-ary, 2-FSK, M=2 01 = 4-ary, 4-FSK, M=4 10 = 8-ary, 8-FSK, M=8 REG9 bits 1-0
Modulation	000 = FSK 001 = MSK 010 = GFSK 011 = GMSK REG9 bits 6-4
Internal / External reference clock selection	This control bit selects the reference clock source. For most applications, a 40 MHz reference clock is supplied externally by other ComBlocks (set bit to '1'). Two notable exceptions are: ■ Reference clock selection must be 'internal' when this module is the first in the transmission chain and when using the internally generated test sequences (see Test mode below). ■ Reference clock selection must also be 'internal' when user-supplied input data is synchronous with a CLK_IN clock frequency other than the recommended 40 MHz. 0 = internal clock 1 = external clock REG10 bit 0
Output sample format	0 = 2's complement 1 = unsigned See also REG10 bit 2 for additional settings. REG10 bit 1
Output data flow	0 = output data is pushed to the next module (for example to COM-2001, or COM-1027) 1 = output data is pulled by next module (for example by the COM-4004) REG10 bit 2

Test mode	00 = disabled 01 = internal generation of 2047-bit periodic pseudo-random bit sequence as modulator input. (overrides external input bit stream). 10 = unmodulated carrier. (overrides external input bit stream) REG10 bit 5 – 4
Input bus enabled	Controls whether the input connection is point-to-point or point-to-multipoint over a data bus (via a COM-9004 demultiplexing connector for example). The J1 input connector pinout is affected by this control bit. 0 = direct connection. Point to point. 1 = input data bus enabled. REG10 bit 7
Bus address	Unique 4-bit address identifying this module on the input bus (if the input bus is enabled in REG10 bit 7). Ignore otherwise. This module acts as bus slave: it performs the read/write transaction requested by the bus master if and only if the bus address matches its own address defined here. This address must be unique among modules connected to the same bus in order to avoid conflicts. REG11 bits 3-0

Configuration example:

COM-1028 FSK modulator -> COM-2001 baseband D/A converters

In this setup, the COM-1028 generates a 2047-bit pseudo-random data stream at a rate of 1 Mbit/s. The modulation is 2-FSK with a modulation index of 0.5. The center frequency is 2 MHz. Mid-amplitude setting.

Settings:
COM-1028: 33 33 03 66 66 06 80 80 00 00 12 00
COM-2001: n/a

Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
J1connector pin B7	Symbol clock
J1 connector pin B8	Bit clock
J1 connector pin B9	Sample clock
J1 connector pin A9	PRBS11 start of 2047-bit period
TP1	FPGA DONE pin. High indicates proper download of the FPGA configuration file.

ComScope Monitoring

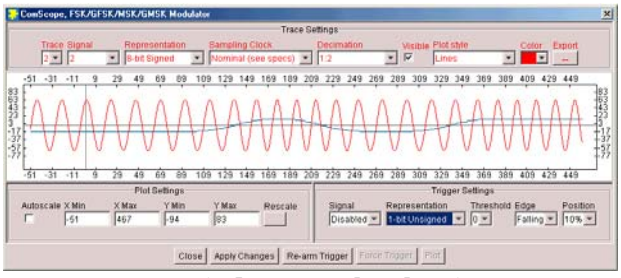
Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-1028 signal traces and trigger are defined as follows:

Trace 1 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Data symbols before Gaussian filter	8-bit signed	8 samples /symbol	512
2: Data symbols after Gaussian filter	8-bit signed	8 samples /symbol	512
3: Frequency modulator phase	8-bit signed	8 samples /symbol	512
4: Modulated Signal I-channel	8-bit signed	f_{clk}	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: Internal PRBS-11 test sequence	Binary	1 sample / bit	4096
2: Modulated Signal Q-channel	8-bit signed	f_{clk}	512
Trigger Signal	**Format**		
1: Start of internal PRBS11 test sequence	binary		

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk} processing clock as real-time sampling clock.

In particular, selecting the f_{clk} processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope Window Sample: showing GMSK modulator output (red) and Gaussian filter output (blue).

Operation

FSK Modulation

The FSK modulation and its derivatives (CPFSK, MSK, GMSK, GFSK) are best described by the following equations for the modulated signal s(t). The first equation describes a phase modulator, with the modulated centered around the center frequency f_c.

$$s(t) = \sqrt{\frac{2E_s}{T}}.\cos(2\pi f_c t + \theta(t) + \theta_0)$$

where

- E_s is the energy per symbol
- T is the symbol period
- f_c is the center frequency
- $\theta(t)$ is the phase modulation

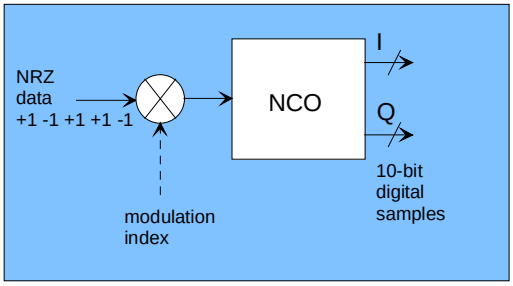
The COM-1028 implements a continuous phase FSK modulator. There are no phase discontinuities between symbols. The CPFSK phase modulation can be described as:

$$\theta(t) = \frac{\pi h}{T}\int_0^t a_i(t)dt$$

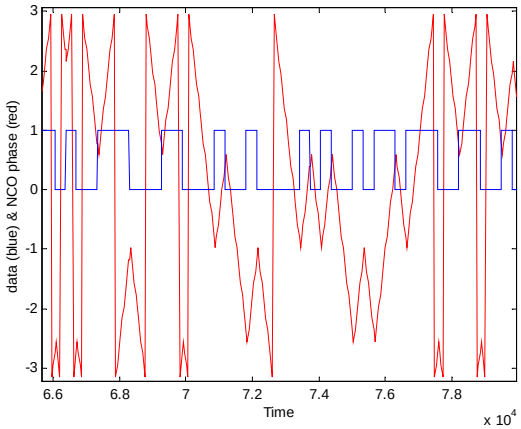
where:

- h is the modulation index. A modulation index of 0.5 yields a maximum phase change of π/2 over a symbol.
- a_i are the symbols. With 2-FSK, the binary data is represented as –1 (for '0') and +1 (for '1').

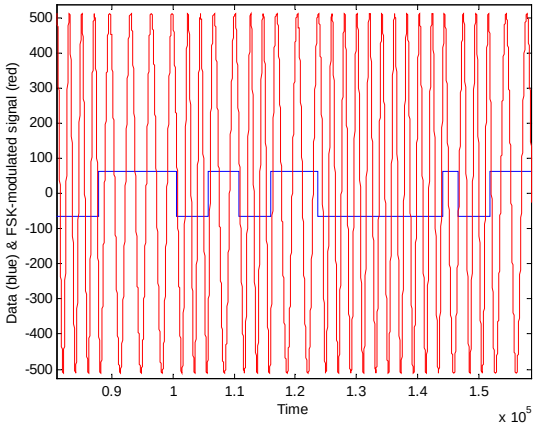
The generic implementation of a CPFSK modulator is based on the use of a numerically controlled oscillator (NCO) as shown in the block diagram below:



CPFSK modulator



NCO phase, continuous phase FSK 2-FSK, center frequency fc = 0, modulation index h = 0.5



Continuous FSK modulated signal example

FSK modulation is sometimes characterized by the frequency separation between symbols. The relationship between modulation index h and frequency separation is $f_{separation} = 0.5\ h\ f_{symbol\_clk}$

M-ary Number M

Transmitted data is grouped into symbols of size 1, 2, or 3 consecutive bits. The size of the symbol alphabet is thus M = 2, 4 or 8. The packing of serial data bits into alphabet symbols is such that the MSB is received first at the DATA_IN serial input.

The mapping between symbol alphabet and modulation symbol a_i is described in the table below:

Symbol alphabet	Modulation symbol a_i
2-FSK '0'	-1
2-FSK '1'	+1
4-FSK "00"	-3
4-FSK "01"	-1
4-FSK "10"	+1
4-FSK "11"	+3
8-FSK "000"	-7
8-FSK "001"	-5
8-FSK "010"	-3
8-FSK "011"	-1
8-FSK "100"	+1
8-FSK "101"	+3
8-FSK "110"	+5
8-FSK "111"	+7

Gaussian Filter

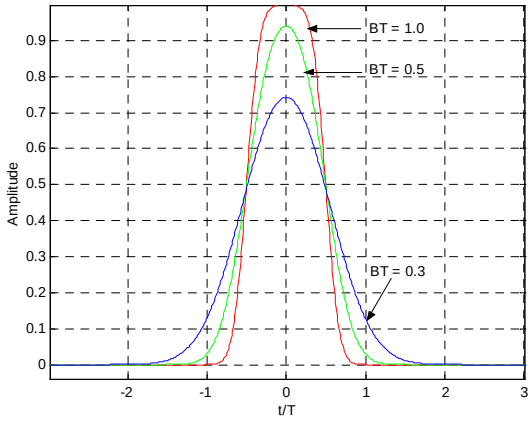
A filter with Gaussian impulse response can be used as pre-filtering of the symbols prior to the continuous phase modulation. Its purpose is to control the modulated signal bandwidth.

The Gaussian filter is characterized by its BT product (B is the –3 dB bandwidth, T is the symbol period = $1/f_{\text{symbol rate}}$). The lower the BT product, the narrower the modulation bandwidth and the higher the inter-symbol interference.

The filter impulse response is expressed analytically as: $h(t) = \frac{1}{\sqrt{2\pi}\sigma T}\exp\left(\frac{-t^2}{2\sigma^2 T^2}\right)$

where $\sigma = \frac{\sqrt{\ln(2)}}{2\pi BT}$

The impulse response h(t) is further convoluted with the rectangular waveform representing the symbol width T. The resulting impulse is illustrated below for BT = 0.3, 0.5 and 1.0.



Shaping pulses for BT = 0.3, 0.5 and 1.0 (Gaussian convoluted with rectangle window)

Configuration Files

This module is configured at installation with a BT = 0.3 Gaussian filter. The BT product can be selected as either 0.3 or 0.5. Changing the BT product requires loading additional firmware once using the ComBlock control center, then switching between up to two stored firmware versions (it takes 5 seconds).

All firmware versions can be downloaded from www.comblock.com/download.

COM-1028-**A** FSK/MSK/GFSK/GMSK modulator, Gaussian filter BT = 0.3 .

COM-1028-**B** FSK/MSK/GFSK/GMSK modulator, Gaussian filter BT = 0.5.

To verify which firmware is currently installed, open the settings window and click on the "Advanced" button. The firmware option is listed at the bottom of the advanced settings window.

Input Elastic Buffer

An input elastic buffer is used to provide independence between the user-supplied input clock CLK_IN (up to 40 MHz) and the internal processing clock $\mathbf{f_{clk}}$.

Input data DATA_IN is written into the input elastic buffer at the rising edge of CLK_IN when SAMPLE_CLK_IN = '1'.

The data is read out of the input elastic buffer at the symbol rate * 1 (2-ary FSK), * 2 (4-ary FSK) or * 3 (8-ary FSK).

The input buffer size is 256 symbols.

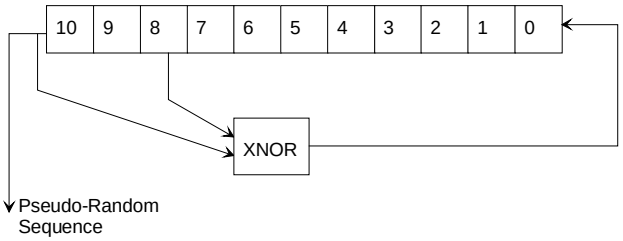
For continous-mode applications, the data source must provide enough data to prevent an 'empty buffer' (or buffer underflow) condition. The SAMPLE_CLK_IN_REQ signal acts as a conventional Clear To Send (CTS) signal: a '1' tells the data source that the elastic buffer is less than half full and thus can accept at least 128 FSK symbols.

When the input buffer is empty (for example at the end of a burst), the modulator output is disabled. One word of caution: as the output enable/disable signal is immediate, the last few symbols in a burst may be truncated while undergoing signal processing.

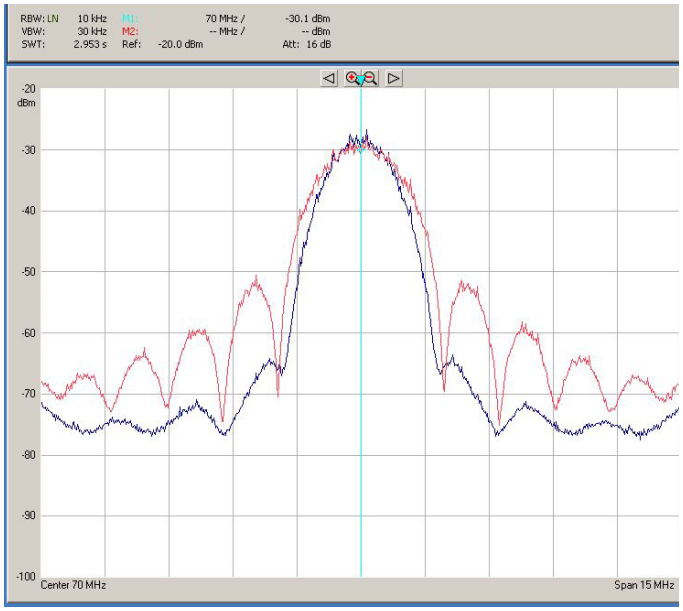
Note: The FIR filters are not reset at the end of a burst.

Pseudo-Random Bit Stream (PRBS-11)

A periodic pseudo-random sequence can be used as modulator source instead of the input data stream. A typical use would be for end-to-end bit-error-rate measurement of a communication link. The sequence is 2047-bit long maximum length sequence generated by a 11-tap linear feedback shift register:



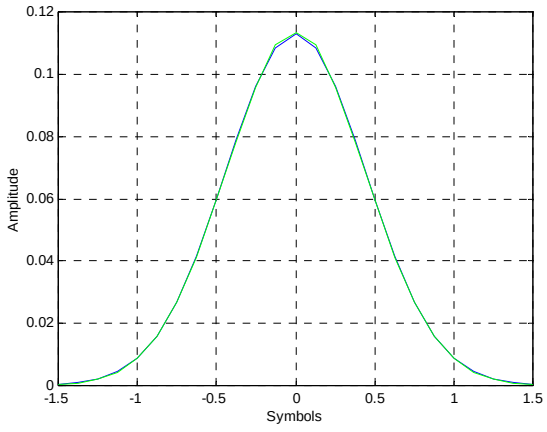
The first 100 bits of the PN sequence are as follows:
0000000000 0111111111 0011111110 0001111100 1100111000 0000010011 1111010001 1110110100 1101001100 0011000001



MSK(red) vs GMSK(blue) spectrum
Using COM-1028 & COM-4004
2.6Msymbols/s, 0.5 modulation index, 70 MHz center frequency, GMSK BT 0.3

Implementation

Gaussian Filter Response BT = 0.3 (-A)

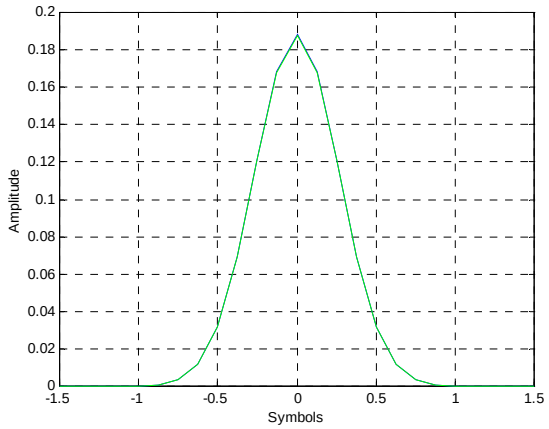


Filter impulse response. 8 samples/symbol ideal (blue), implemented (green).

The gaussian filter with BT=0.3 is a 25-tap FIR filter with the following impulse response:
Coeff(0) = 3/1024
Coeff(1) = 7/1024
Coeff(2) = 17/1024
Coeff(3) = 36/1024
Coeff(4) = 72/1024
Coeff(5) = 130/1024
Coeff(6) = 220/1024

Coeff(7) = 336/1024
Coeff(8) = 488/1024
Coeff(9) = 640/1024
Coeff(10) = 784/1024
Coeff(11) = 896/1024
Coeff(12) = 928/1024
Coeff(j=13:24) = coeff(24-j);

Gaussian Filter Response BT = 0.5 (-B)



Filter impulse response. 8 samples/symbol ideal (blue), implemented (green).

The gaussian filter with BT=0.5 is a 17-tap FIR filter with the following impulse response:
Coeff(0) = 1/1024
Coeff(1) = 6/1024
Coeff(2) = 28/1024
Coeff(3) = 95/1024
Coeff(4) = 258/1024
Coeff(5) = 568/1024
Coeff(6) = 992/1024
Coeff(7) = 1376/1024
Coeff(8) = 1536/1024
Coeff(j=9:16) = coeff(16-j);

Timing

Clocks

An 80 MHz internal clock f_{clk} is generated by frequency doubling of the internal or external 40 MHz clock. f_{clk} is used for internal processing and for generating the output clock CLK_OUT = f_{clk} /2.

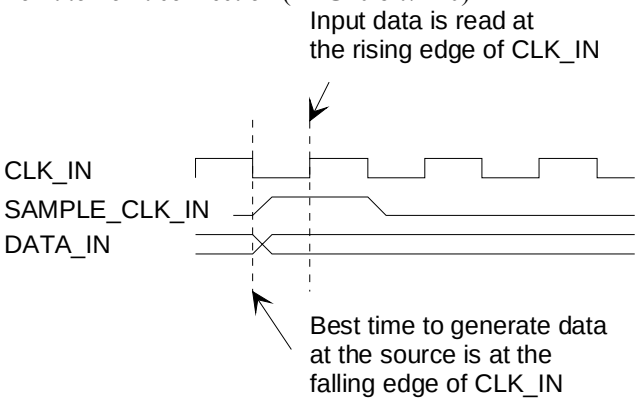
I/Os

In general, the I/O signals are synchronous with the rising edge of the reference clock CLK_IN or CLK_OUT (i.e. all signals transitions always occur after the rising edge of clock). The maximum frequency for CLK_IN is 40 MHz. The frequency for CLK_OUT is fixed at 40 MHz (f_{clk} /2) .

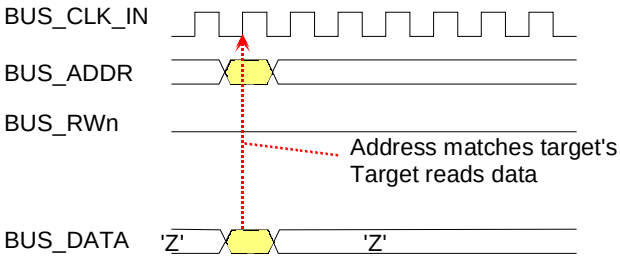
A special case is when the output is connected to the COM-4004 70 MHz IF modulator. The data samples are then pulled out by a 100 MHz clock. The complex I and Q samples are time-multiplexed for a maximum throughput of 50 Msamples/s. For timing details, please refer to the COM-4004 specifications.

Input

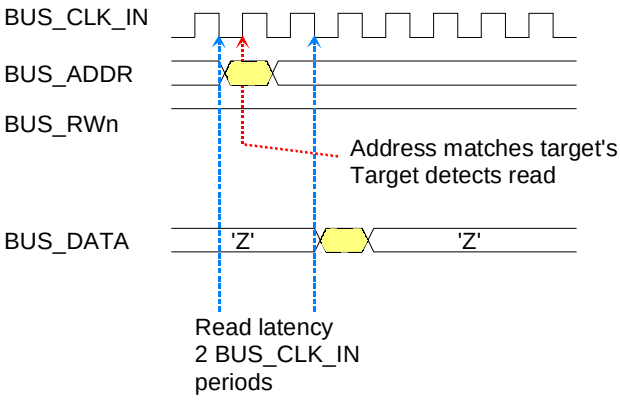
Point to Point connection (REG10 bit7 = 0)



Point to Multi-points connection (REG10 bit7 = 1).
COM-1028 is a bus slave. It always listens to BUS_CLK_IN, BUS_ADDR, BUS_RWN.



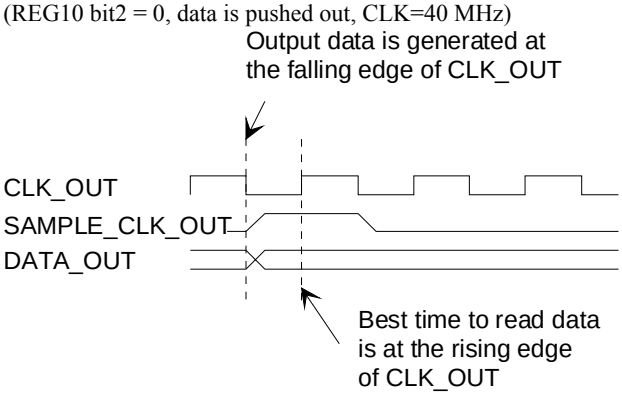
Master writes data streams to COM-1028 target(s)



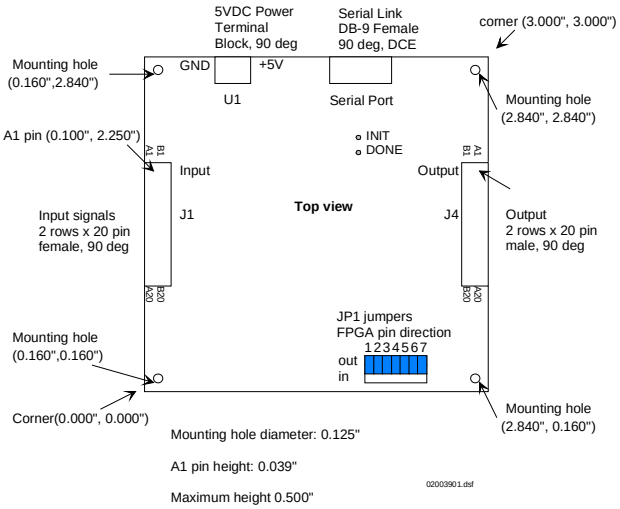
Master reads flow control from COM-1027 target

Output

(REG10 bit2 = 0, data is pushed out, CLK=40 MHz)



Mechanical Interface

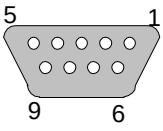


Note: All seven JP1 jumpers must be in the 'OUT' location.

Pinout

Serial Link P1

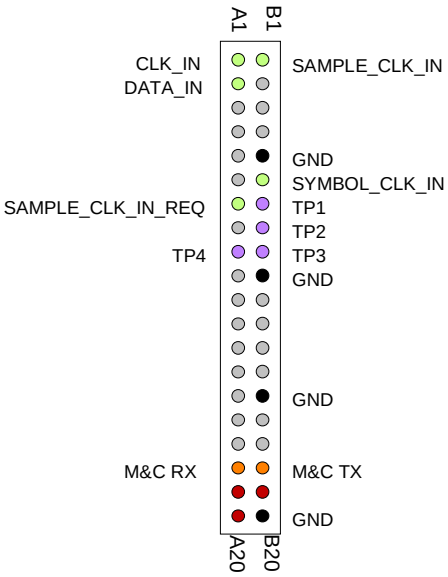
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



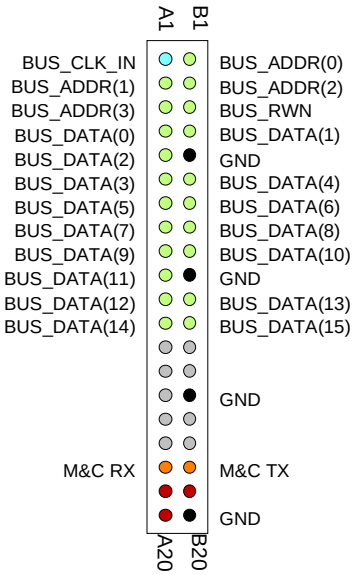
DB-9 Female

2 Transmit
3 Receive
5 Ground

Input Connector J1

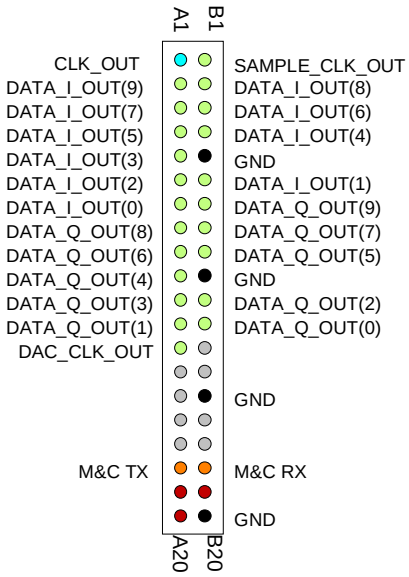


This connector is used for point-to-point input, i.e. direct connection between two ComBlocks when control register REG10(7) = '0'.

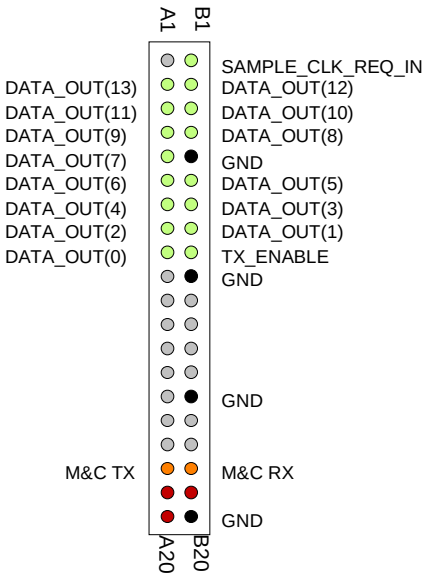


This connector is used for point-to-multipoint (bus) connection when control register REG10(7) = '1'. COM-1028 is a bus slave. It always listens to BUS_CLK_IN, BUS_ADDR, BUS_RWN.

Output Connector J4



This connector is used when output data is pushed out (configuration REG10 bit2 = 0).



This connector is used when output data is pulled out by the next module (configuration REG10 bit 2 = 1).

I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-1010 Convolutional encoder	COM-1027 FSK/GFSK Demodulator (back to back)
COM-7001 Turbo Code Error correction encoder	COM-2001 digital-to-analog converter (baseband).
COM-1410 LDPC + long BCH code error correction encoder	COM-4004 70 MHz IF modulator
COM-8001 Arbitrary waveform generator 256MB	COM-1024 Multi-path simulator
COM-8004 Signal diversity splitter	COM-1023 BER generator, Additive White Gaussian Noise Generator
COM-5003 TCP-IP / USB Gateway	

Configuration Management

This specification is to be used in conjunction with VHDL software revision 9.

ComBlock Ordering Information

COM-1028
FSK/MSK/GFSK/GMSK modulator

MSS • 18221-A Flower Hill Way •
Gaithersburg, Maryland 20879 • U.S.A.
Telephone: (240) 631-1111
Facsimile: (240) 631-1676
E-mail: sales@comblock.com