COM-1028 FSK/MSK/GFSK/GMSK DIGITAL MODULATOR VHDL SOURCE CODE OVERVIEW

Overview

The COM-1028 ComBlock Module comprises two pieces of software:

- VHDL code to run within the FPGA for all signal processing functions
- C/Assembly code running within the Atmel ATMega8515L microprocessor for non application-specific monitoring and control functions.

The VHDL code interfaces to the monitoring and control functions by exchanging byte-wide registers on the Atmel microcontroller 8-bit data bus. The control and monitoring registers are defined in the specifications [1].

The COM-1028 VHDL code runs on the generic COM-8000 hardware platform. The schematics [2] for this platform are available in this CD.

The Atmel microprocessor code is generic (i.e. non application specific), not user-programmable and functionally transparent to the user. It is thus not described here.

Reference documents

[1] specifications: com1028.pdf

[2] hardware schematics: com_8000schematics.pdf

[3] VHDL source code in directory
com-1028_006\src

[4] .ucf constraint file
com-1028_006\src\root_mod.ucf

[5] .mcs FPGA bit files (-A and –B options)
com-1028_006\com1028A_006.mcs
com-1028_006\com1028B_006.mcs

[6] Xilinx ISE project file
com-1028_006\com-1028.npl

Configuration Management

The current software revision is 6.
Two software options (-A and –B) can be created:

- COM-1028-A for Gaussian filter BT product 0.3
- COM-1028-B for Gaussian filter BT product 0.5
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The option can be selected by:

(a) selecting the gaussian_fil_05.vhd or the gaussian_fil_03.vhd files in the project.
(b) Replacing the name gaussian_fil_xx in the fsk_modulator.vhd program (two occurrences: a component declaration, and component instantiation).
(c) Changing the 'OPTION' constant (x41 for 'A', x42 for 'B') in the com1028.vhd root source file.

VHDL development environment

The VHDL software was developed using the Xilinx ISE 4.1 development environment. The synthesis tool is FPGA Express 3.6.

Target FPGA

The VHDL code was synthesized for the Xilinx Spartan-IIE XC2S300E-6PQ208 FPGA.

Xilinx-specific code

The VHDL source code was written in generic VHDL with few Xilinx primitives. No Xilinx CORE is used. The Xilinx primitives are:

- BUFG
- IBUFG
- CLKDLL (x2)
- RAMB4_S1_S1
- RAMB4_S1_S2
- RAMB4_S4_S4

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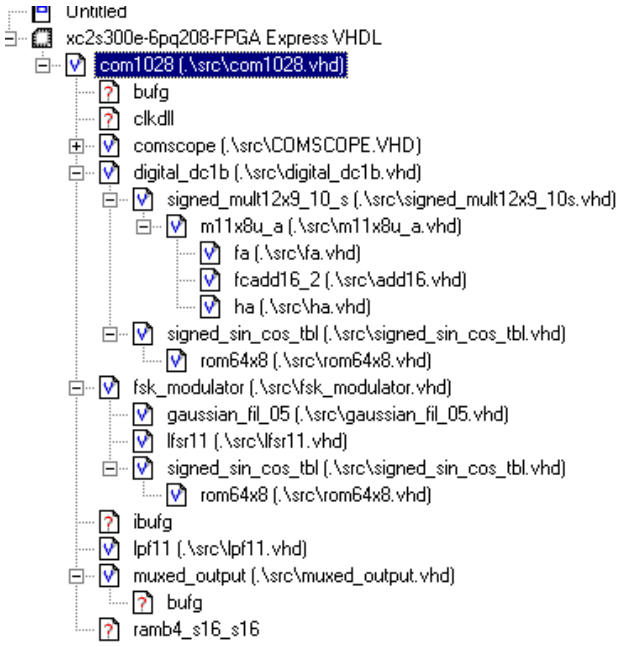
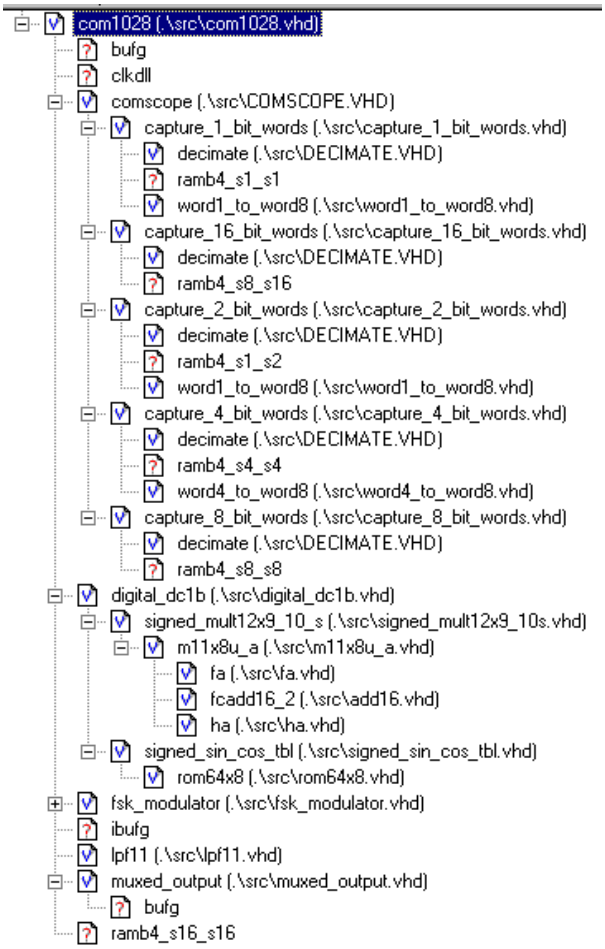
- RAMB4_S8_S8
- RAMB4_S8_S16
- RAMB4_S16_S16

VHDL software hierarchy



(Comscope is not expanded)



(fsk_modulator is not expanded)

The code is stored with one, and only one, entity per file as shown above.

The root program (highlighted) is *com1028.vhd*.

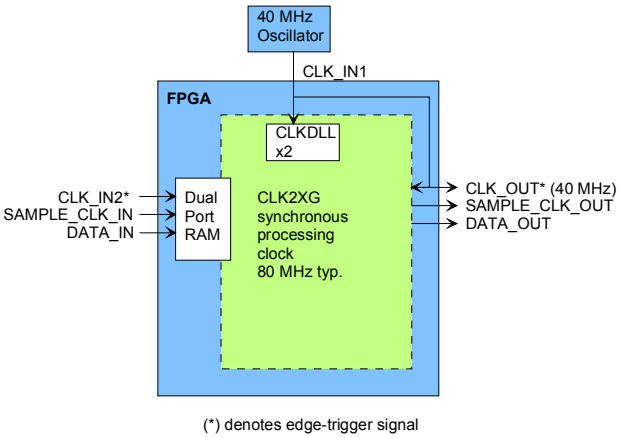
Due to the relatively large size of the project, it is recommended to synthesize components into individual EDIF files first (synthesize with the I/O pads option disabled). Then remove the .vhd source file reference from the project. Be sure to keep the .edf EDIF file in the directory where it was created. The root file should be synthesized with the I/O pads option enabled.

Clock / Timing

The software uses two different clocks:

- an external clock CLK_IN2 which serves synchronous clock for the input data stream.

- CLK_IN1 is generated by a 40 MHz oscillator on the COM-1028 module. It is used as reference for the output clock and for the double-frequency processing clock. The code is written to meet the timing requirements on the target FPGA at a speed of at least 80 MHz.



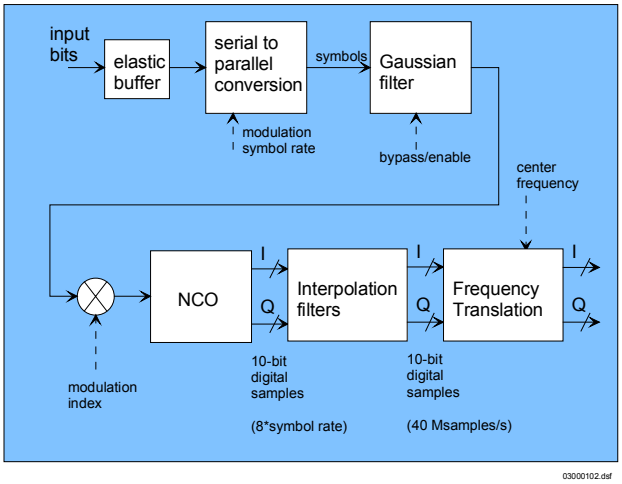
The hierarchical nature of the VHDL code reflects the block diagram below:

- *com1028* is the root program which includes the modulator *fsk_modulator*, the frequency translation *digital_dc1b, comscope* to capture and display internal signals and ancillary monitoring and control functions (interface with microprocessor).
- the basic FSK modulation functions are encapsulated within *fsk_modulator*. The modulated signal is over-sampled at 8 times per symbol in order to get an accurate representation of the Gaussian filter in the time domain.
- After modulation, the samples can be interpolated up to 40 Msamples/s.

Interpolation is performed by successive stages of oversampling and low-pass filtering (*lpf11*). Up to three x4 interpolation stages can be activated, depending on the modulation rate.

- After modulation, the digital sampled signal can be translated in frequency using *digital_dc1b*. The frequency translation is realized in the form of a complex vector rotation, using sine/cosine lookup tables (*signed_sin_cos_tbl*) and pipeline multipliers (*signed_mult12x9_10_s*) made of half adders *ha* and full adders *fa*. The frequency translation is implemented at the maximum speed of one complex sample per processing clock.
- the PRBS-11 pseudo-random test pattern is generated within the *lfsr11* entity.

Block Diagram



FPGA Usage

```
Design Summary
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   Number of errors:      0
   Number of warnings:   19
   Number of Slices:              2,738 out of  3,072   89%
   Number of Slices containing
```

```
      unrelated logic:                0 out of  2,738    0%
   Number of Slice Flip Flops:    3,441 out of  6,144   56%
   Total Number 4 input LUTs:     3,310 out of  6,144   53%
      Number used as LUTs:                    3,182
      Number used as a route-thru:              128
   Number of bonded IOBs:            45 out of    142   31%
      IOB Flip Flops:                          18
   Number of Block RAMs:              4 out of     16   25%
   Number of GCLKs:                   4 out of      4  100%
   Number of GCLKIOBs:                4 out of      4  100%
   Number of DLLs:                    1 out of      4   25%
Total equivalent gate count for design:  128,647
Additional JTAG gate count for IOBs:  2,352
```

Contact Information

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