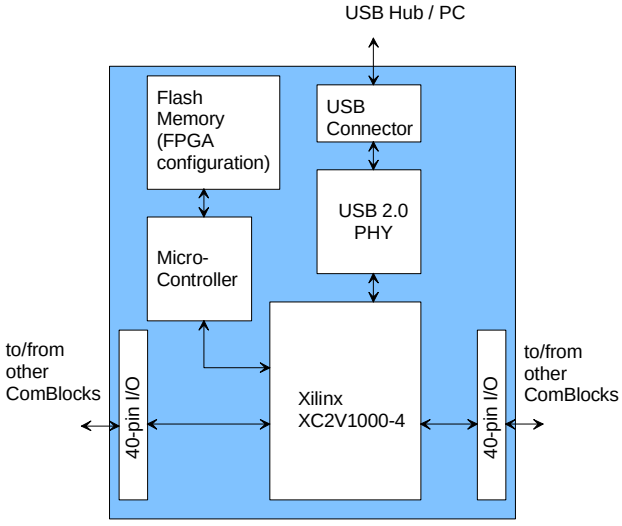
COM-1100
FPGA DEVELOPMENT PLATFORM
& USB 2.0 HIGH-SPEED INTERFACE

Key Features

- Develop custom signal processing applications on FPGA using this generic development platform.
- Xilinx Virtex-II XC2V1000-4 FPGA features 1 million system gates, 720Kbit of dual port memory, 40 18x18 multipliers.
- USB 2.0 interface supports signaling rates of 480 Mbits/s (High Speed) and 12 Mbits/s (Full Speed). Typical sustained data throughputs are 85 Mbit/s (HS) and 6.5 Mbit/s (FS).
- Modules can be stacked for large design development.
- FPGA configuration remains in non-volatile flash memory and is automatically reloaded at power up.
- Graphical User Interface is used for remote monitoring and control over simple serial link. This includes loading FPGA configuration file into flash. No special cable nor serial EPROM is needed.
- This module is interface compatible with other pre-programmed ComBlock modules.
- 120 MHz maximum clock rate (typ.).
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Single 5V supply with reverse voltage and overvoltage protection. Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom).



Block Diagram

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1100.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

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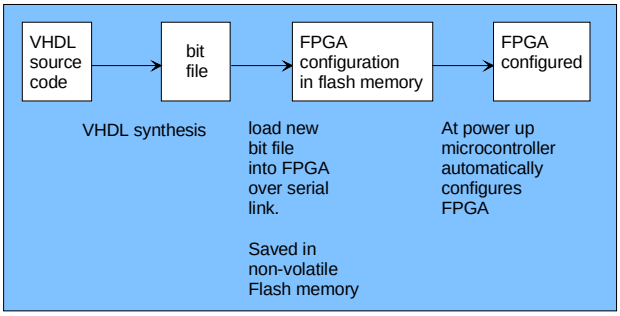
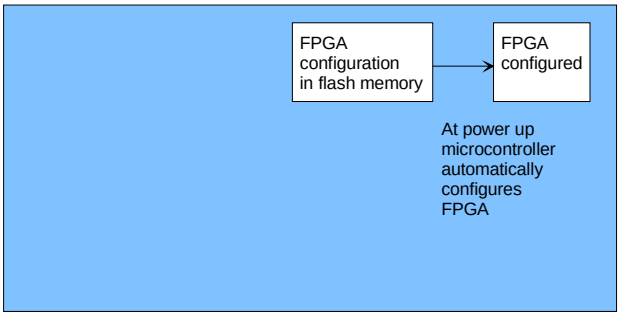
Application Development Process



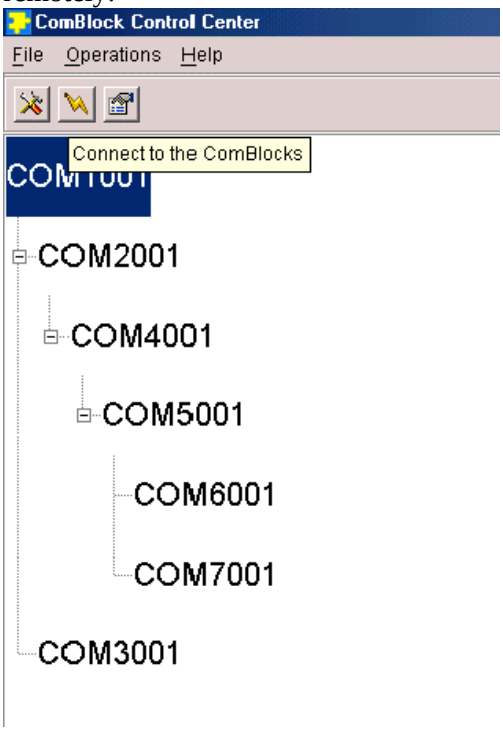
Development environment



Run-time environment

Graphical User Interface

When activated, the GUI enumerates the ComBlock modules within the assembly. The modules are identified by their name in a tree-like structure. Each module can be configured and monitored remotely.

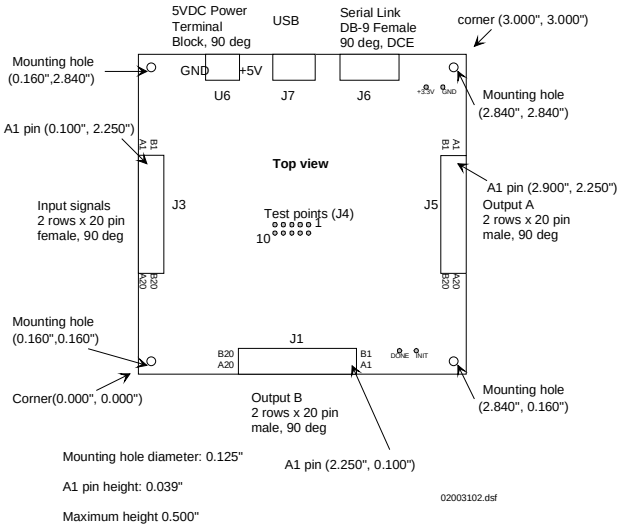


The ComBlock Control Center software is provided with all ComBlock modules. The user's manual can be found at www.comblock.com/download/ccchelp.pdf

Electrical Interface

Interfaces	Definition
J3(34:1)	J3 connector (left). Mostly used for input signals.
J1(34:1)	J1 connector (bottom). Mostly used for output signals. J3(1) plays a special role as external clock, an alternative to the internal 40 MHz clock reference.
J5(34:1)	J5 connector (right). Mostly used for output signals.
TEST_POINTS(10:1)	Ten test points are provided in the form of a dual-row 0.1" spacing header for easy access by an oscilloscope probe.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 120 MHz is TBDmA.

Mechanical Interface



Schematics

The board schematics are available on-line at www.comblock.com/download/com_1100schematics.zip

VHDL code template

A VHDL template project is available from the ComBlock CD or on-line at www.comblock.com/download/com1100template_007.zip
The template project includes:

- the VHDL source code (.vhd)
- the constraint file (.ucf) listing all pin assignments
- The Xilinx ISE project with the synthesis and implementation settings
- The resulting bit file (.mcs) ready to be loaded into flash memory

This code template describes how the application interfaces with the ComBlock Control Center graphical user interface through control and monitoring registers. Monitoring and control messages and syntax are described in www.comblock.com/download/m&c_reference.pdf

It also describes how to capture key internal signals in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center.

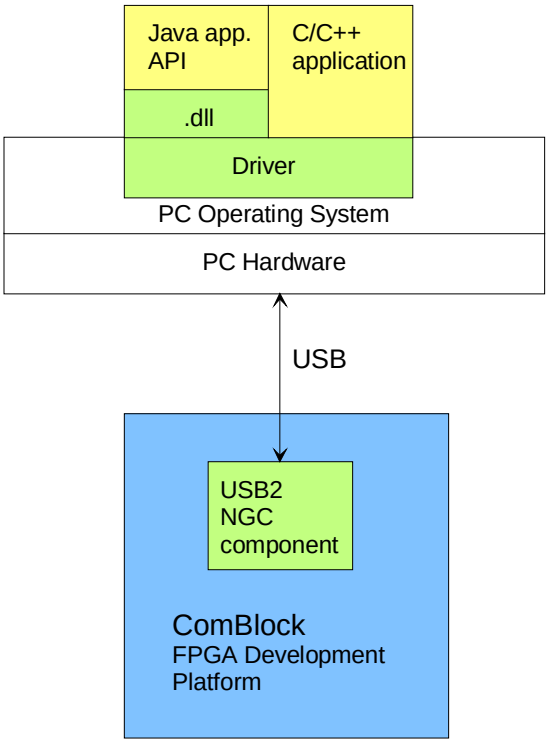
The ComScope user manual is available at www.comblock.com/download/comscope.pdf.

USB 2.0 Driver

Software to help developers create USB high-speed communication between the COM-1100 platform and a host PC is provided. The **USB 2.0 software package** includes the following:

- USB20 NGC component for integration within the VHDL code
- VHDL top-level code template
- Windows device driver for XP/2000 (.sys, .inf files)
- Java API, .dll and application sample code
- C/C++ application sample code

The **USB 2.0 software package** is available in the ComBlock CD and can also be downloaded from www.comblock.com/download/usb20.zip .
The user manual is available at www.comblock.com/download/USB20_UserManual.pdf



Blue: supplied hardware
Green: supplied ready-to-use software
Yellow: Source code examples.

I/Os

Important: The I/O signals connected directly to the FPGA are NOT 5V tolerant!

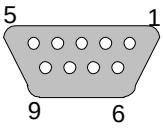
Pinout

USB

USB type B receptacle, as the COM-1100 is a USB device.

Serial Link

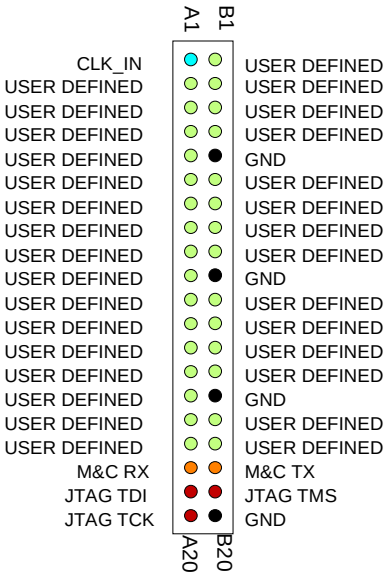
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



DB-9 Female

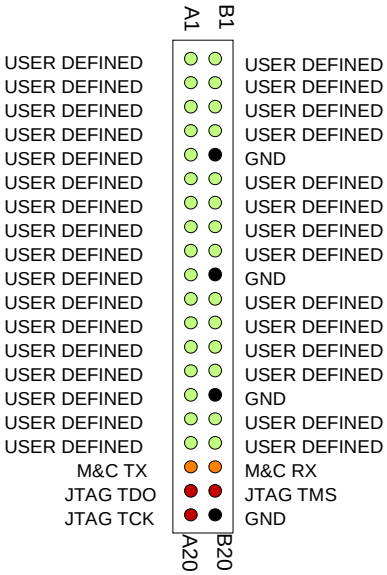
2 Transmit
3 Receive
5 Ground

(Input) Connector J3



Note: although the J3 connector is generally referred to as 'Input', individual user-defined pins can be configured as 'IN', 'OUT', or 'INOUT' in the user VHDL source code.

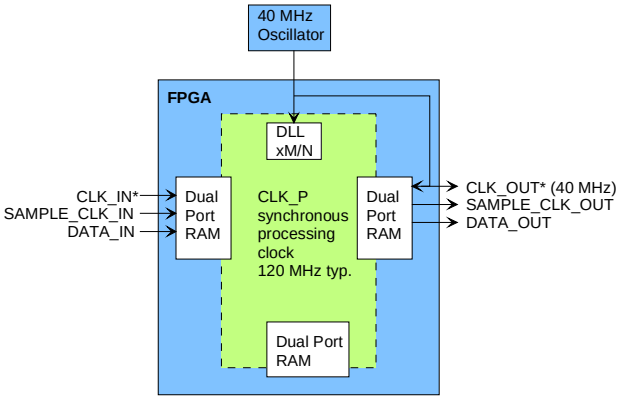
(Output) Connectors J1,J5



Note: although the J1/J5 connectors are generally referred to as 'Output, individual user-defined pins can be configured as 'IN', 'OUT', or 'INOUT' in the user VHDL source code.

Clock Architecture

The clock distribution scheme embodied in the VHDL source code template is illustrated below.



(*) denotes edge-trigger signal

Baseline clock architecture
Green = 120 MHz processing zone
Blue = 40 MHz I/O zone

The core signal processing performed within the FPGA is synchronous with the CLK_P processing clock. The processing clock frequency is programmable as 40 MHz * M/N at the time of VHDL synthesis by settings the M/N ratio in the DCM attribute of the VHDL source code. In practice, a processing frequency around 120 MHz is consistent with the Virtex-II technology (i.e. timing constraints are met without resorting to excessive pipelining/reclocking). In order to minimize clock jitter, the CLK_P processing clock is derived from a 40 MHz oscillator with low-jitter.

The signals at the digital input connector J3 are synchronous with the CLK_IN signal at J3/A1. This clock is typically 40 MHz.

The signals at the digital output connectors J1/J5 are synchronous with the 40 MHz CLK_OUT signal derived from the 40 MHz oscillator.

Dual-port RAM elastic buffers are used at the boundaries between I/Os and internal processing area.

Other clock architectures are possible by changing the VHDL source code.

Configuration Management

This specification is to be used in conjunction with VHDL code template software revision 7, and the ComBlock Control Center revision 2.31 or above.

ComBlock Ordering Information

COM-1100 FPGA development platform & USB 2.0 interface

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