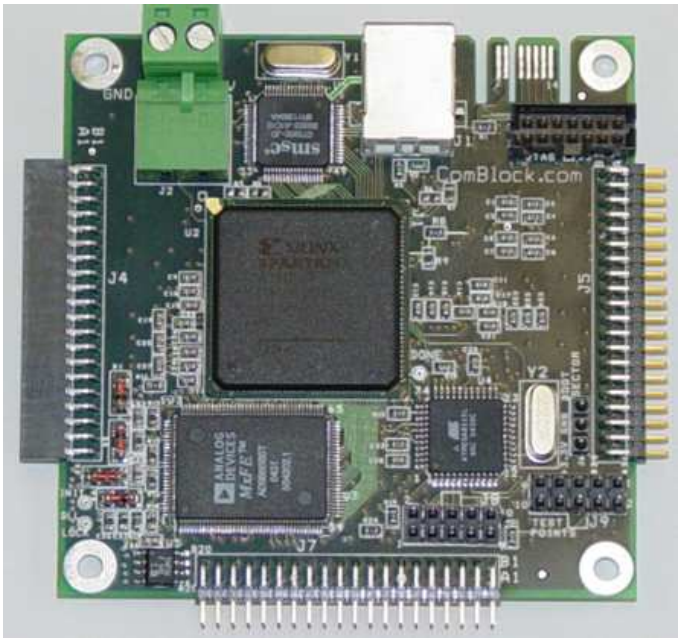
COM-1200 FPGA DEVELOPMENT PLATFORM (Spartan-3 2000), TX/RX ANALOG FRONT-END & USB 2.0

Key Features

- Develop custom signal processing applications on FPGA using this generic development platform.
- Xilinx Spartan-3 XC3S2000-4 FPGA (**-B** option) features 2 million system gates, 720Kbit of dual port memory, 40 dedicated 18x18 multipliers.
- Analog front end (AD9860) features
  2 10-bit high-speed ADCs 64Msamples/s
  2 12-bit high-speed DACs 64Msamples/s[1]
  2 10-bit ADCs and
  3 8-bit DACs
- USB 2.0 interface supports signaling rates of 480 Mbits/s (High Speed) and 12 Mbits/s (Full Speed). Typical sustained data throughputs are 85 Mbits/s (HS) and 6.5 Mbits/s (FS).
- Temperature sensor.
- 32Mb non-volatile flash memory stores up to 4 distinct FPGA configurations (3 custom + 1 fixed baseline). The selected configuration is automatically reloaded at power up or upon command within 2.2 seconds.
- Graphical User Interface is used for remote monitoring and control over USB. This includes loading FPGA configuration file into flash (non-volatile). FPGA configuration can also be loaded via a JTAG cable (volatile).
- This module is interface compatible with other pre-programmed ComBlock modules.
- 120 MHz maximum practical FPGA processing clock rate (typ.)
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Includes NGC components (software drivers) for USB 2.0/1.1 and AD9860 mixed-signals front-end.
- Single 5V supply with reverse voltage and overvoltage protection. Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom).

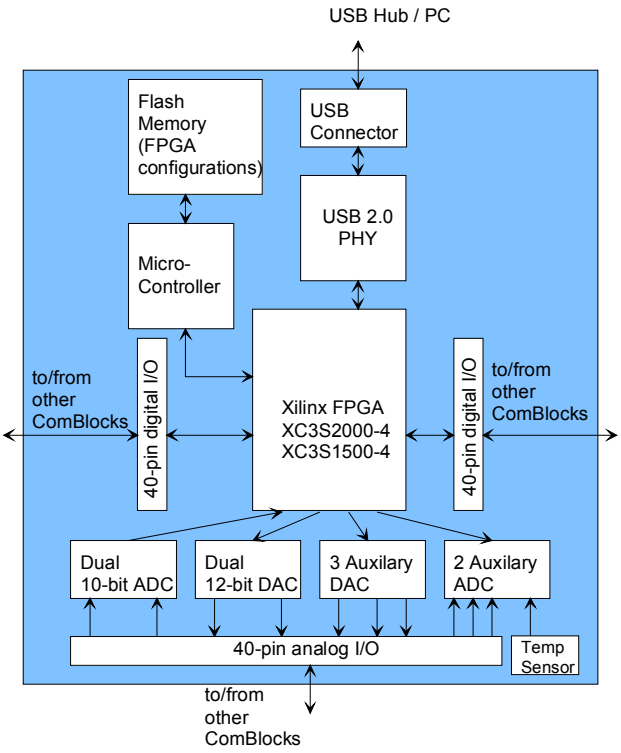


For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1200.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

[1] 128 MSamples/s after fixed x2 interpolation

MSS • 18221-A Flower Hill Way • Gaithersburg, Maryland 20879 • U.S.A.
Telephone: (240) 631-1111 Facsimile: (240) 631-1676 www.ComBlock.com
 Issued 5/13/2010

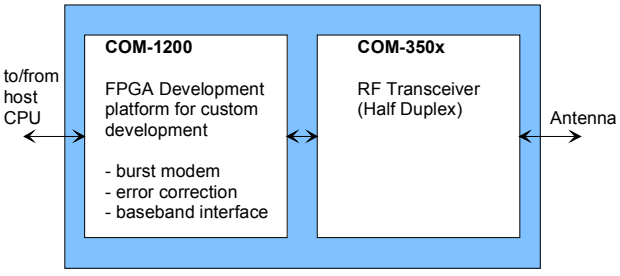


Block Diagram

Typical Application

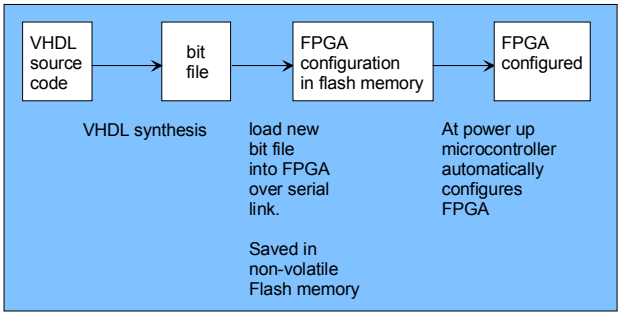
Half-Duplex RF Transceiver

The COM-1200 is ideally suited as a digital development platform for developing custom wireless applications. A two-way (half-duplex) RF transceiver consisting of only two ComBlock modules can be built when using the COM-1200 digital/baseband analog platform in conjunction with the COM-350x RF transceivers.

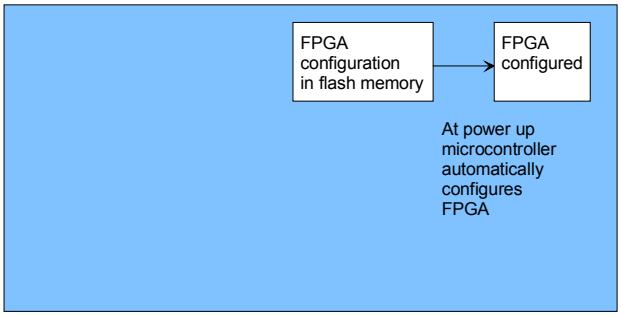


The COM-1200 platform analog interface (J7) is fully compatible with the COM-3501 UHF transceiver.

Application Development Process



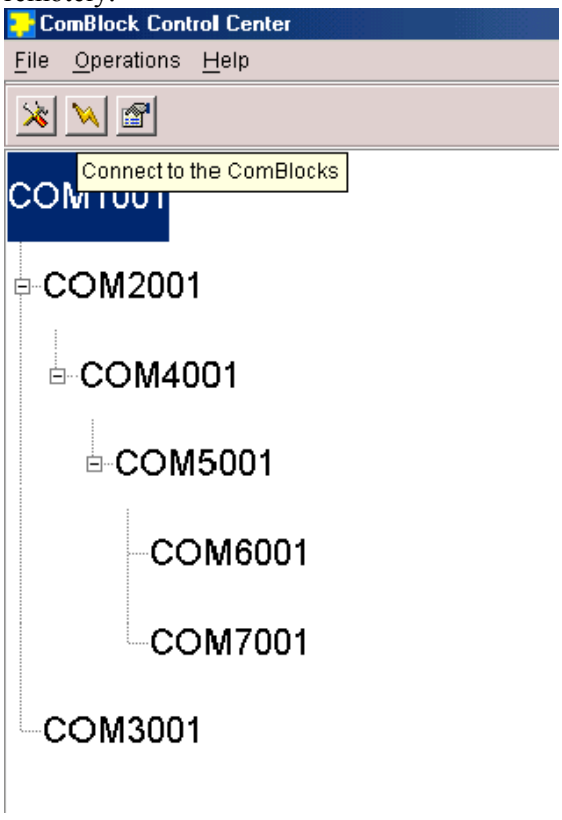
Development environment



Run-time environment

Graphical User Interface

When activated, the GUI enumerates the ComBlock modules within the assembly. The modules are identified by their name in a tree-like structure. Each module can be configured and monitored remotely.



The ComBlock Control Center software is provided with all ComBlock modules. The user's manual can be found at
www.comblock.com/download/ccchelp.pdf

Electrical Interface

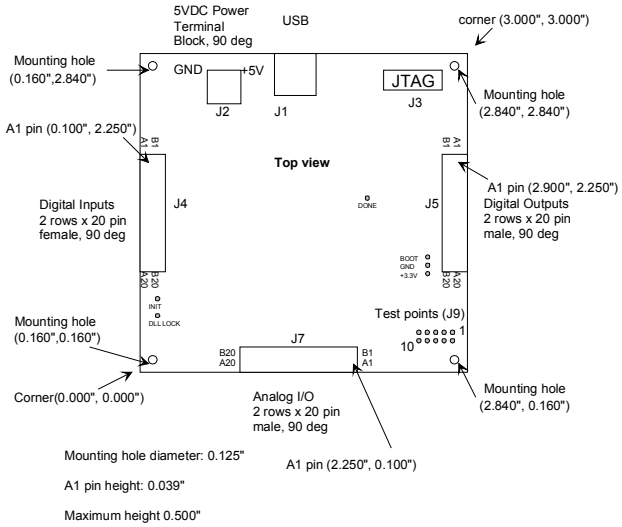
Analog I/O (J7)	**Definition**
RX_I_P / RX_I_N	I-channel differential inputs. (_P for +, _N for -). 200 Ohm input impedance. 2Vpp differential (1Vpp on each RX_I_P and RX_I_N signal) for full scale 10-bit ADC conversion. Common-mode voltage is approximately 2.3V. It is recommended that the input be AC coupled.
RX_Q_P / RX_Q_N	Q-channel differential inputs. (_P for +, _N for -). Same electrical characteristics as above.
TX_I_P / TX_I_N	I-channel differential outputs. (_P for +, _N for -). Full range 2Vpp differential (1Vpp on each TX_I_P and TX_I_N signal). Common mode voltage is approximately 1V. Output impedance 100 Ohm.
TX_Q_P / TX_I_N	Q-channel differential outputs. (_P for +, _N for -). Same electrical characteristics as above.
AUX_DAC_A AUX_DAC_B AUX_DAC_C	Analog output signals. Range: 0 – 3.3V. Typically used for controlling the gain of external RF front-end transmitter and/or receiver.
AUX_ADC_A1/A2 AUX_ADC_B1	Three analog input signals, multiplexed into two auxiliary ADCs. Range: 0 – 3.3V. Typically used for monitoring the levels of external RF front-end transmitter and/or receiver.
D_CNTRL(6:1)	Digital control signals. LVTTL 0 – 3.3V. Typically used for controlling the real-time operation of an external RF front-end transmitter and/or receiver. Note: D_CNTRL[3-6] share the same FPGA pins as
Digital I/O	**Definition**
J4(34:1)	J4 connector (left). Mostly used for input signals. J4(1) plays a special role as external clock, an alternative to the internal 40 MHz clock. LVTTL signals (0 – 3.3V) as default I/O standard. Differential LVDS signals also available after minor board modifications.
J5(34:1)	J5 connector (right). Mostly used for output signals. LVTTL signals (0 – 3.3V) as default I/O standard. Differential LVDS signals also available after minor board modifications.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.5 – 5.5VDC. Terminal block. Power consumption is approximately proportional to the sampling clocks and FPGA internal processing clocks. The maximum power consumption at 64 Msamples/s / 120 MHz is 800mA. **Please use a power supply with voltage transients below 6.6V at power up and power down.**

Absolute Maximum Ratings

Supply voltage	-0.5V min, +6V max
RX_I_P/RX_I_N/RX_Q_P/RX_Q_N inputs	-0.5V min, +3.8V max

Important: The I/O signals connected directly to the FPGA are NOT 5V tolerant!

Mechanical Interface



Test Points

Ten test points are provided in the form of a dual row 0.1" spacing header for easy access by an oscilloscope probe or logic analyzer.

The analog front-end DLL lock information is available as a test point labeled DLL_LOCK.

Schematics

The board schematics are available on the ComBlock CD-ROM supplied with the module and on-line at http://www.comblock.com/download/com_1200schematics.zip

VHDL code template

A VHDL template project is available from the ComBlock CD or on-line at www.comblock.com/download/com1200template_003.zip
The template project includes:

- the VHDL source code (.vhd)
- the constraint file (.ucf) listing all pin assignments.
- Synthesized (NGC) components for the USB 2.0 and AD9860 analog front-end drivers.
- The Xilinx ISE project with the synthesis and implementation settings.
- The resulting bit file (.mcs) ready to be loaded into flash memory.

The sample code describes how the application interfaces with the ComBlock Control Center graphical user interface through control and monitoring registers. Monitoring and control messages and syntax are described in www.comblock.com/download/m&c_reference.pdf

It also describes how to capture key internal signals in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.

Analog Front-End

The COM-1200 receives and transmits analog signals through the Analog Devices AD9860 mixed signal front-end.

A ready-to-use NGC component (driver) is supplied to provide the user access to the following AD9860 features:

- 64 Msamples/s 10-bit complex input samples.
- 64 Msamples/s 12-bit complex output samples.
- Fixed x2 transmit interpolation to 128 Msamples/s.
- Programmable fine tuning transmit frequency offset in the range +/- 64 MHz, by steps of 1.9 Hz.
- Programmable receive channel A/B gain. min 0 = 0 dB, max 20 dB gain set at power-up.
- three 8-bit DACs (AUX_DAC_A/B/C) with a typical setup time of 2 µsecs.
- Four 10-bit ADCs sampled every 24 µsecs.

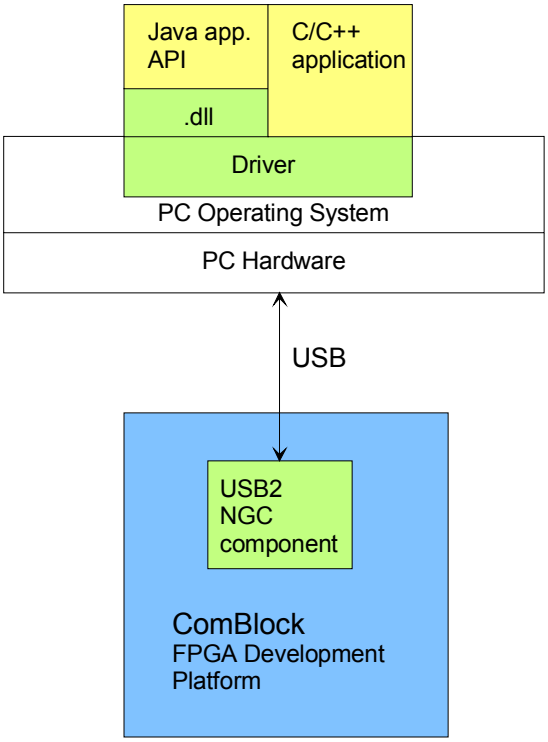
The NGC component can be instantiated by the application developer. The component interface is described in the VHDL code template.

USB 2.0 Driver

Software to help developers create USB high-speed communication between the COM-1100 platform and a host PC is provided. The **USB 2.0 software package** includes the following:

- USB20 NGC component for integration within the VHDL code
- VHDL top-level code template
- Windows device driver for XP/2000 (.sys, .inf files)
- Java API, .dll and application sample code
- C/C++ application sample code

The **USB 2.0 software package** is available in the ComBlock CD and can also be downloaded from www.comblock.com/download/usb20.zip .
The user manual is available at www.comblock.com/download/USB20_UserManual.pdf



Blue: supplied hardware
Green: supplied ready-to-use software
Yellow: Source code examples.

Temperature Sensor

The built-in temperature sensor has the following specifications:

- temperature range –40°C to +120°C [2]
- accuracy over temperature ±2°C (typ.)
- 8-bit quantization steps: 1.2°C

FPGA Configuration

Flash Memory

The FPGA configuration is stored in non-volatile (Flash) memory. The ComBlock Control Center graphical user interface includes the utility to (re)write the FPGA .mcs prom file into the flash memory over the selected communication link.

Communication links: the COM-1200, when used as stand-alone, communicates with the ComBlock Control Center exclusively over USB. When part of larger ComBlock assembly, the COM-1200 can communicate over any other communication link supported by the assembly, namely asynchronous serial, USB, LAN/TCP-IP, PCMCIA or CardBus.

The FPGA is automatically configured after power-up or reset with the configuration file stored in Flash memory. The configuration file size for the XC3S2000 is 7,673,000 bit. Configuration time is typically 2.2sec.

JTAG

During the development phase, rapid (3 seconds) FPGA configuration can be achieved by using a JTAG cable (for example Xilinx parallel cable IV (DLC7)) between the COM-1200 JTAG header (J3) and a host computer. This is the fastest method to load the FPGA but the configuration is lost when power is turned off.

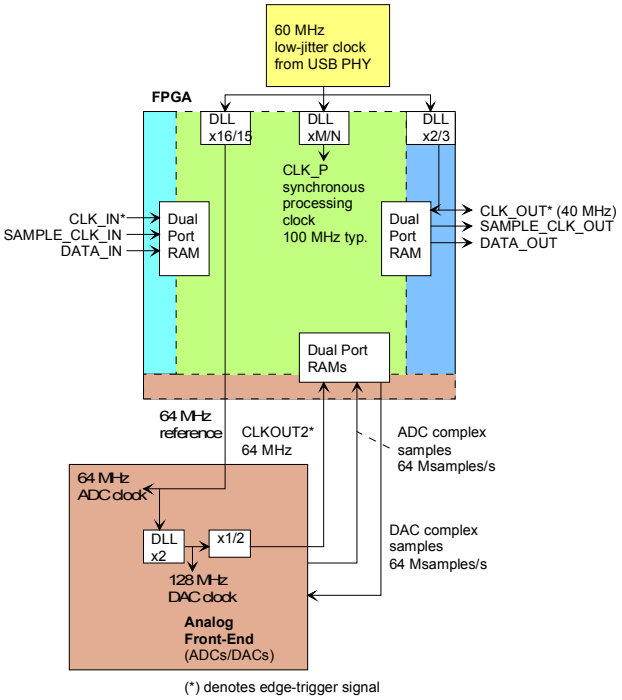
Accidental FPGA file corruption

The COM-1200 is protected against corruption by an invalid FPGA configuration file. To recover from such occurrence, connect the BOOT pin to the nearby ground pin using a jumper and power-up the COM-1200. The COM-1200 will be automatically configured with a default FPGA configuration which restores USB communication. This boot file is inerasable. Once this is done, the user can safely re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center GUI.

[2] The COM-1200 nominal operating range is 0 to 70°C.

Clock Architecture

The clock distribution scheme embodied in the VHDL source code template is illustrated below.



Baseline clock architecture
Yellow = 60 MHz reference clock
Green = 120 MHz (typ) processing zone
Dark Blue = 40 MHz output clock
Light Blue = 40 MHz external input clock
Brown = 64 MHz I/O zone

The core signal processing performed within the FPGA is synchronous with the CLK_P processing clock. The processing clock frequency is programmable as 60 MHz * M/N at the time of VHDL synthesis by settings the M/N ratio in the DCM attribute of the VHDL source code. In practice, a processing frequency around 120 MHz is consistent with the Spartan-3 technology (i.e. timing constraints are met without resorting to excessive pipelining/reclocking). In order to minimize clock jitter, the CLK_P processing clock is derived from a 60 MHz low-jitter reference clock originating from the USB 2.0 PHY integrated circuit.

The signals at the digital input connector J5 are synchronous with the CLK_IN signal at J5/A1. This clock is typically 40 MHz.

The signals at the digital output connector J6 are synchronous with the 40 MHz CLK_OUT signal derived from the 60 MHz reference clock.

The signals at the analog front-end interface are synchronous with the 64 MHz reference clock generated by the FPGA.

16Kbit dual-port RAM elastic buffers are used at the boundaries between I/Os and internal processing area.

Other clock architectures are possible by changing the VHDL source code.

I/O Standards

The digital signals on connectors J5 and J6 are LVTTL (0 – 3.3V) signals by default. However, the COM-1200 is designed to be easily transformed to support LVDS differential signals for higher speed interconnections. The transformation involves moving a surface mount 0603 zero ohm resistor to change the VCCO voltage from 3.3V to 2.5V. 15 LVDS pairs are connected to the FPGA on each connector.

Switching between LVTLL and LVDS I/O standards must be implemented for all signals on a given connector. The Xilinx ISE will detect as illegal the coexistence of the LVTTL and LVDS I/O standards for signals declared on the same connector (i.e. FPGA I/O bank).

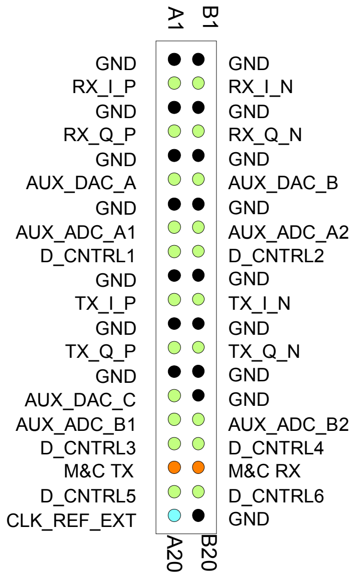
For best performances with LVDS, the internal termination must be enabled by enabling the digitally controlled impedance (DCI) in the Xilinx ISE project.

Pinout

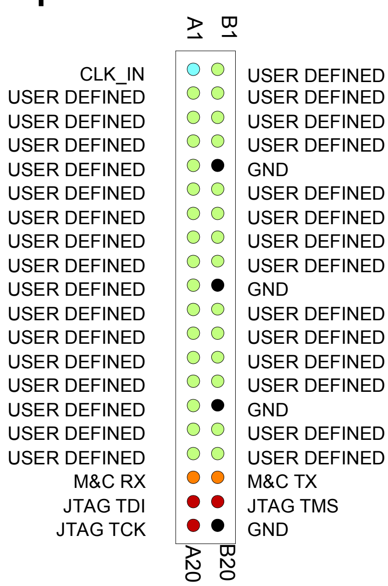
USB

USB type B receptacle, as the COM-1200 is a USB device.

Analog I/O Connector J7

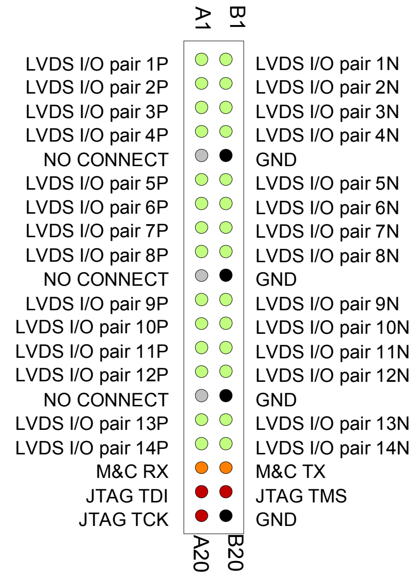


Digital Input Connector J4



(Default LVTTL)

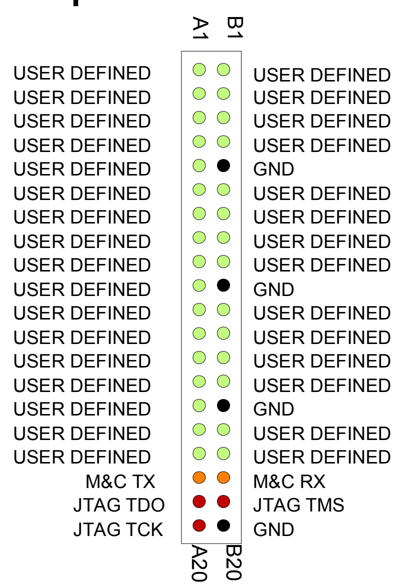
Note: although the J4 connector is generally referred to as ‘Input’, individual user-defined pins can be configured as ‘IN’, ‘OUT’, or ‘INOUT’ in the user VHDL source code.



(Differential LVDS)

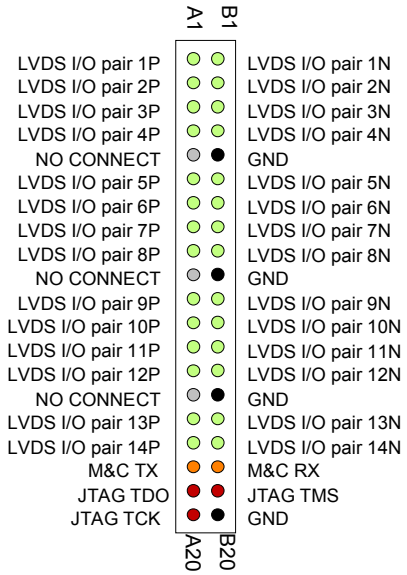
Note: LVDS support requires board modification (soldering a resistor for switching the FPGA VCCO supply voltage).

Digital Output Connector J5



(Default LVTTL)

Note: although the J5 connector is generally referred to as ‘’Output’, individual user-defined pins can be configured as ‘IN’, ‘OUT’, or ‘INOUT’ in the user VHDL source code.



(Differential LVDS)

Note: LVDS support requires board modification (soldering a resistor for switching the FPGA VCCO supply voltage).

I/O Compatibility List

(not an exhaustive list)

Analog I/O
COM-3501 UHF transceiver
Digital Input
COM-3001/2/3/4/5/6/7/8/9/10 RF/IF/Baseband receivers.
COM-8001 Arbitrary waveform generator, 256MB/1GB, 40 Msamples/s
Digital Output
COM-8002 High-speed data acquisition. 256MB/1GB, 40 Msamples/s.
Baseband Interface
COM-5003 LAN 10Base-T/100Base-TX / IP network interface
COM-5004 IP router
COM-1200/1300/1400 FPGA development platforms

Configuration Management

This specification is to be used in conjunction with VHDL code template software revision 1, and the ComBlock Control Center revision 2.36 or above.

ComBlock Ordering Information

COM-1200-**B** FPGA development platform (Spartan-3 2000), , Tx/Rx Analog front end & USB 2.0

MSS • 18221-A Flower Hill Way •
Gaithersburg, Maryland 20879 • U.S.A.
Telephone: (240) 631-1111
Facsimile: (240) 631-1676
E-mail: sales@comblock.com