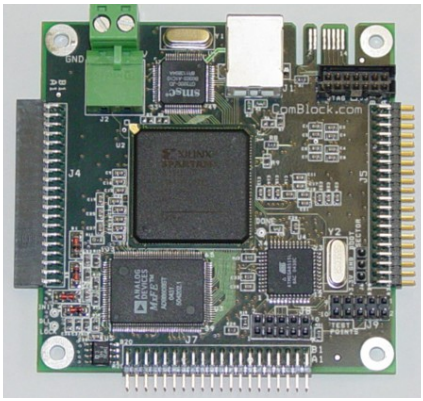
COM-1202/1203 PSK / QAM / APSK modem USB 2.0 / TCP-IP

Key Features

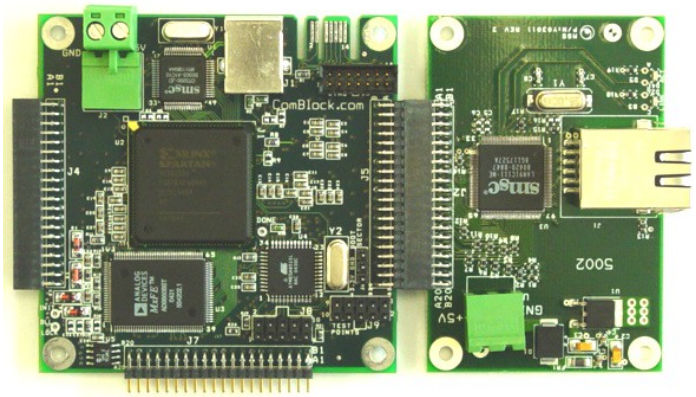
- Flexible modem configuration:
  - Modulation: BPSK, QPSK, OQPSK, π/4 DQPSK, 8-PSK, 16QAM, 16APSK, 32APSK.
  - Variable data rates up to 22 Msymbols/s.
  - Center frequency: +/- 10 MHz.
  - Designed for continuous mode applications. Fast re-acquisition after short link interruption.
  - Modulator and demodulator are independently configured.
  - Phase ambiguity removal capability when transmitting a periodic synchronization sequence
- Demodulator inputs:
  - Digital (2 * 10-bit complex, up to 105Msamples/s)
  - Analog baseband differential (2 * 10-bit complex, 64 Msamples/s).
- Modulator outputs:
  - Digital (2 * 10-bit complex, up to 90 Msamples/s)
  - Digital (2 * 14-bit complex, up to 50 Msamples/s)
  - Analog baseband differential (2 * 12-bit complex, 64 Msamples/s[1]).
- Modem data I/Os:
  - Two synchronous serial interfaces
  - USB 1.1/2.0.
  - TCP-IP/LAN (**COM-1203**).
- Extensive test & monitoring:
  - BER measurement when transmitting PRBS-11 test sequence or frame sync.
  - PRBS-11 test sequence generator
  - Loopback mode
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom). Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1202.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .



COM-1202



COM-1203 (includes TCP-IP)

[1] 128 MSamples/s after fixed x2 interpolation

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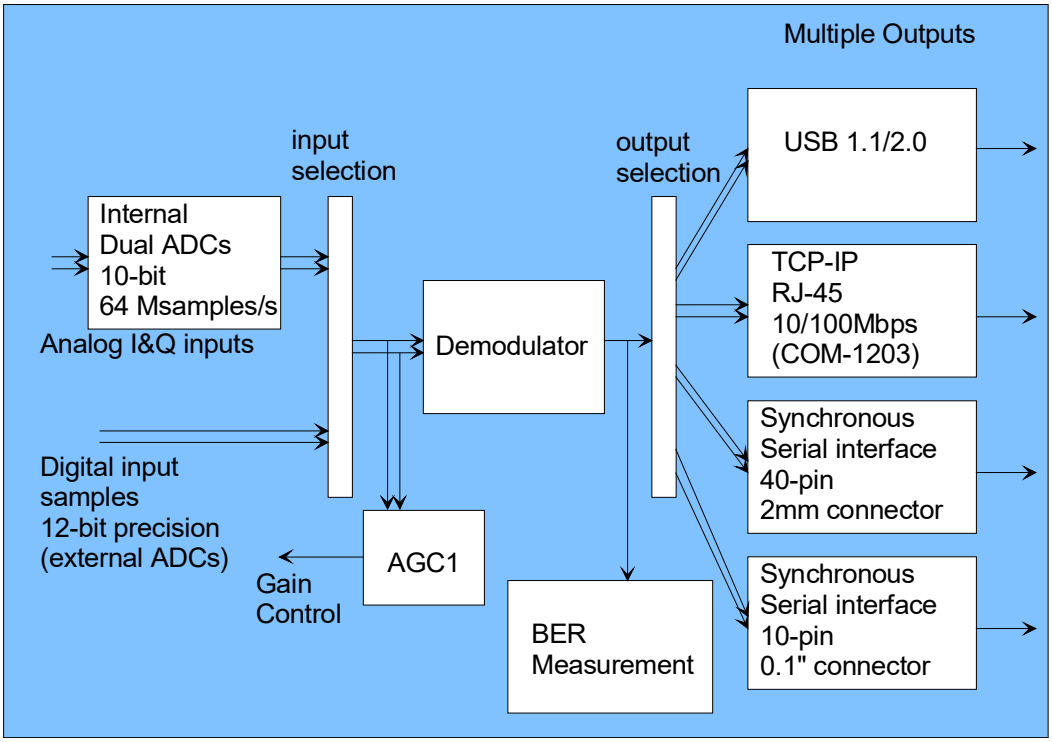
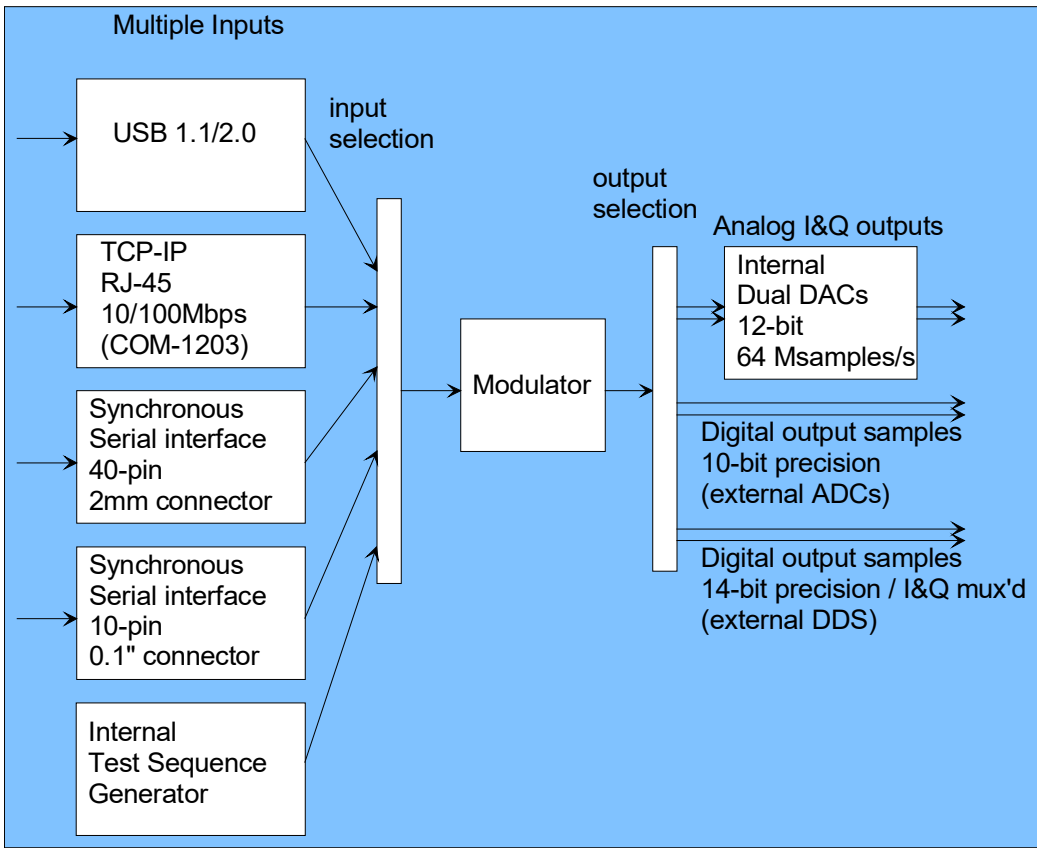
Overall Block Diagram

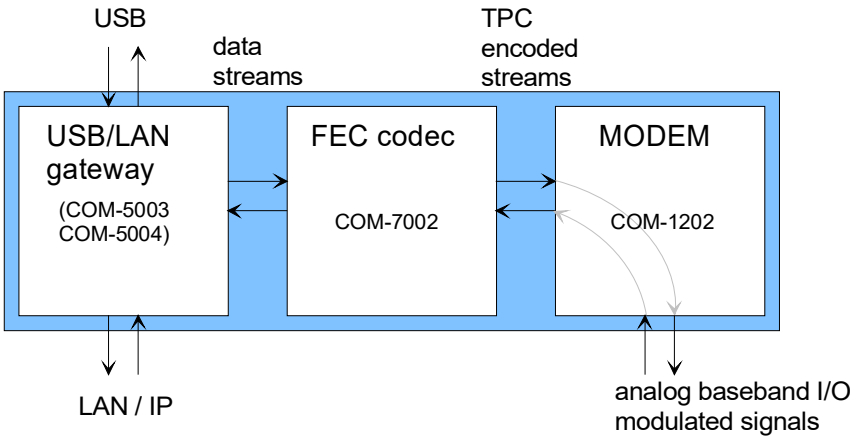


Demodulator block diagram

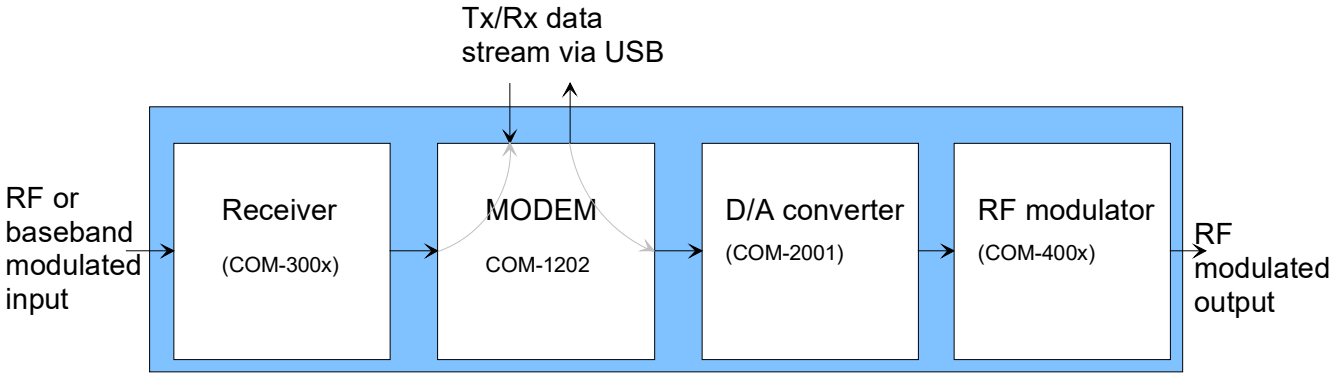


Modulator block diagram

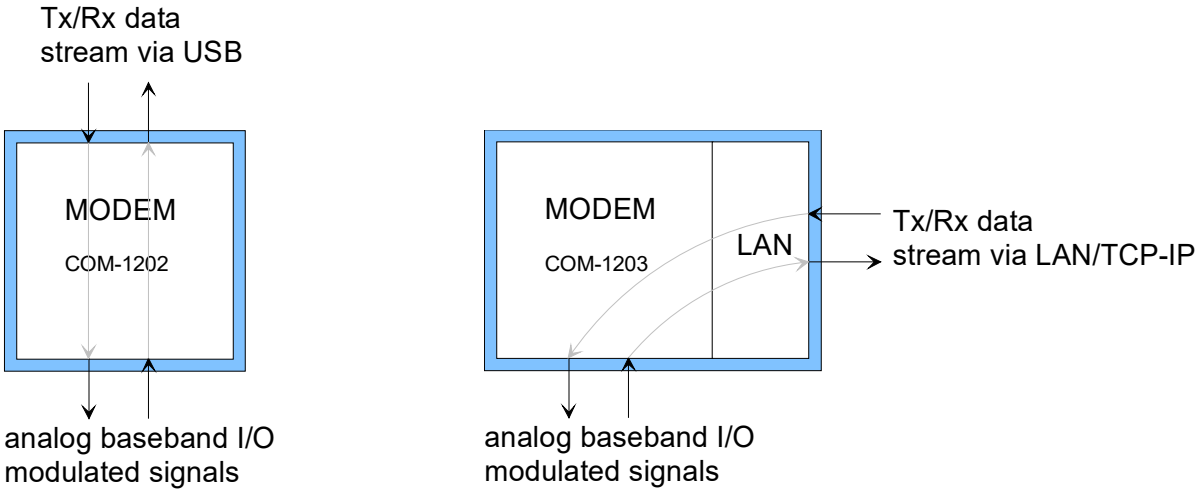
Use example #1 Modulator + Demodulator



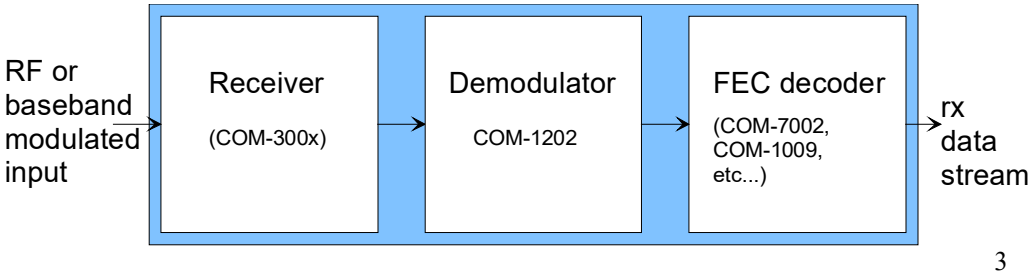
Use example #2 Modulator + Demodulator



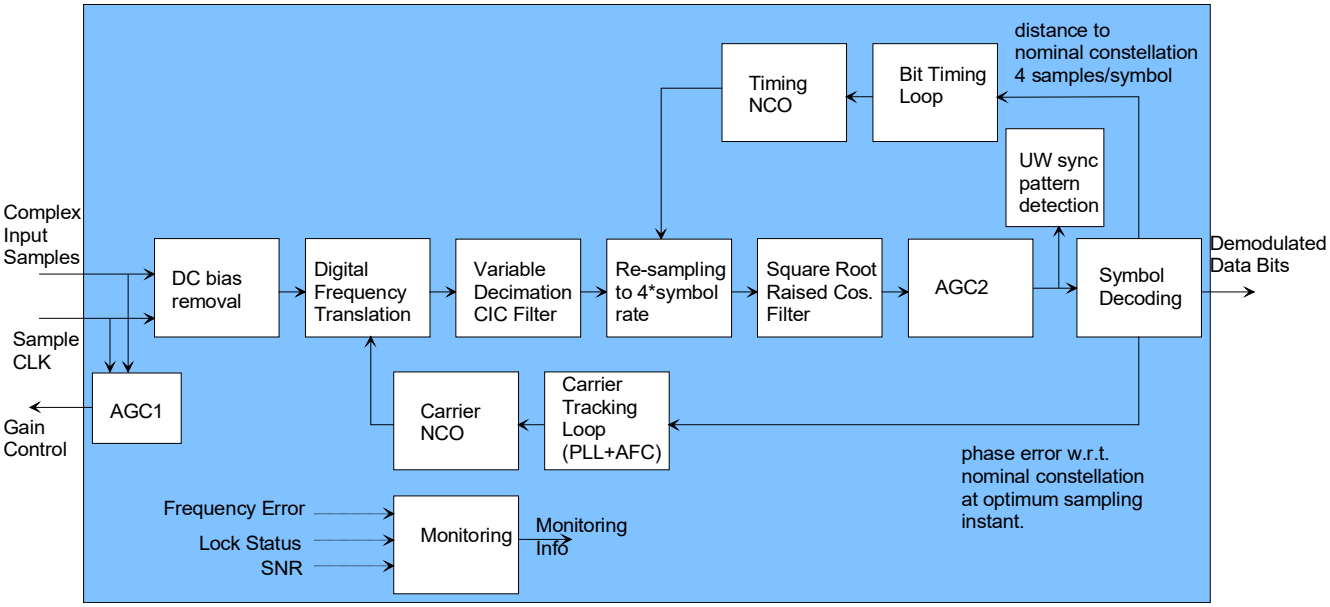
Use example #3 Modulator + Demodulator



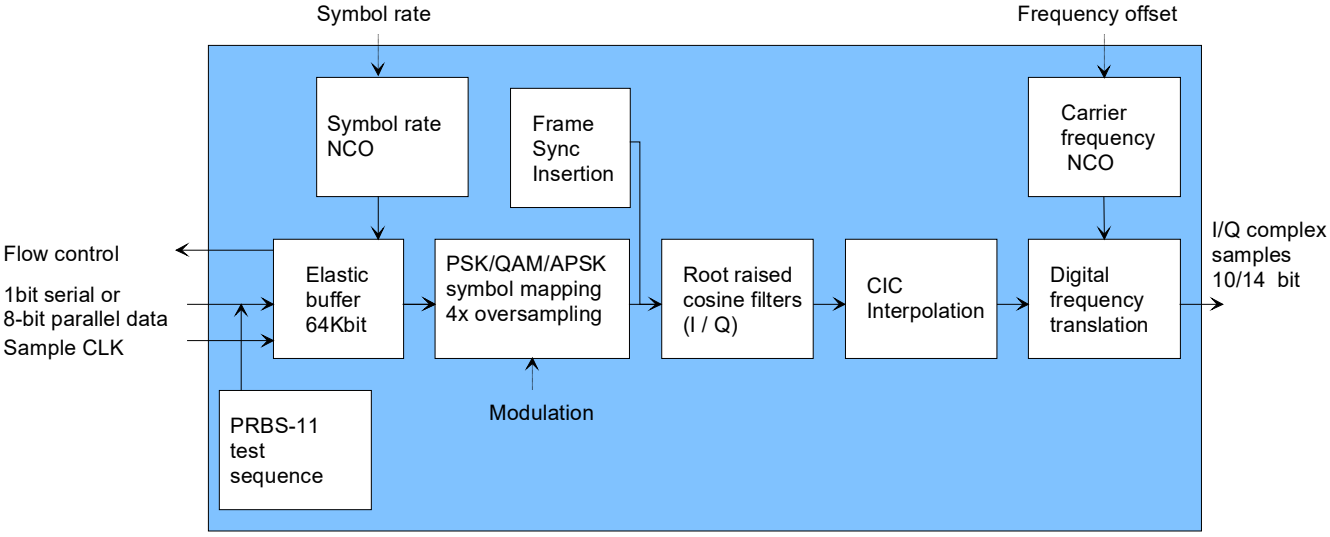
Use example #4 Demodulator-only



Block Diagram (PSK / QAM / APSK Digital Demodulator)



Block Diagram (PSK / QAM / APSK Digital Modulator)



Electrical Interface

Demodulator Digital Input Interfaces (J4)	**Definition**
RX_DATA_I_IN[11:0] RX_DATA_Q_IN[11:0]	Modulated input signal, real and imaginary axes. 12-bit precision. Unsigned format. Unused LSBs are pulled low.
RX_SAMPLE_CLK_IN	Input signal sampling clock $\mathbf{f_s}$. One CLK_IN-wide pulse. Read the input signal at the rising edge of CLK_IN when RX_SAMPLE_CLK_IN = '1'. The minimum input sampling rate is 4 samples/symbol. Samples can be consecutive. For example, RX_SAMPLE_CLK_IN can be fixed at '1' to indicate that new input samples are provided once per CLK_IN clock period. Signal is pulled-up.
CLK_IN	Input reference clock for synchronous I/O. RX_DATA_x_IN and RX_SAMPLE_CLK_IN are read at the rising edge of CLK_IN. Maximum 105 MHz.
AGC_PWM_OUT	Output. When this demodulator is connected directly to an external receiver (COM-300x), it generates an digital pulse-width modulated 0 – 3.3V signal to control the gain prior to A/D conversion. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3.3V is the minimum gain.
Demodulator Analog Input Interfaces (J7)	**Definition**
RX_I_P / RX_I_N	I-channel differential inputs. (_P for +, _N for -). 200 Ohm input impedance. 2Vpp differential (1Vpp on each RX_I_P and RX_I_N signal) for full scale 10-bit ADC conversion. Common-mode voltage is approximately 2.3V. It is recommended that the input be AC coupled.
RX_Q_P / RX_Q_N	Q-channel differential inputs. (_P for +, _N for -). Same electrical characteristics as above.
RX_AGC1	Output. When this demodulator is connected directly to an analog receiver, it generates an analog 0 – 3.3V signal to control the analog gain prior to A/D conversion. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3.3V is the minimum gain. Pin J7/A6.
RX_AGC2	Binary receiver gain control output. Can be used to enable or bypass LNAs for example. '0' to bypass, '1' to enable. LVTTL (0-3.3V) Pin J7/A9
Demodulator Output Interfaces (J5 or J4))	**Definition**
RX_DATA_OUT[3:0]	Demodulator synchronous serial output. Read at the rising edge of CLK_OUT when RX_BIT_CLK_OUT = '1'. 4-bit soft-quantized demodulated bits for use by subsequent error correction decoders. Unsigned representation: 0000 for maximum amplitude '0', 1111 for maximum amplitude '1'. The information bit is the most significant bit RX_DATA_OUT(3).
RX_BIT_CLK_OUT	Demodulator bit clock. One CLK-wide pulse. Read the output signal at the rising edge of CLK_OUT when RX_BIT_CLK_OUT = '1'.
RX_LOCK	'1' when the demodulator is locked, '0' otherwise.
RX_BIT_CLK_OUT_REQ	Flow control input. Demodulator will send demodulated data only if '1'.
CLK_OUT	Output reference clock. Typically 40 MHz.

Modulator Digital Input Interfaces (J4 or J5)	Definition
TX_DATA_IN	Input data stream. Can be configured as one-bit serial, symbol-wide parallel, or 8-bit parallel. When configured as 1-bit serial input, only TX_DATA_IN(0) is used.
TX_SAMPLE_CLK_IN	Input sample clock. One CLK-wide pulse. Read the input signals at the rising edge of CLK when TX_SAMPLE_CLK_IN = '1'.
TX_SAMPLE_CLK_IN_REQ	Output. One CLK_IN-wide pulse. Requests a data bits from the module upstream. For flow-control purposes.
CLK_IN	Input reference clock for synchronous I/O. TX_DATA_IN, and TX_SAMPLE_CLK_IN are aread at the rising edge of CLK_IN. Maximum 105 MHz.
Modulator Digital Output Interfaces (J5) (Output data pushed out)	**Definition**
TX_DATA_I_OUT[9:0]	Modulated output signal, real axis. 10-bit precision. Format: unsigned
TX_DATA_Q_OUT[9:0]	Modulated output signal, imaginary axis. 10-bit precision. Same format as TX_DATA_I_OUT.
TX_SAMPLE_CLK_OUT	Output signal sampling clock. Read the output signal at the rising edge of CLK when TX_SAMPLE_CLK_OUT = '1'. TX_SAMPLE_CLK_OUT is fixed at '1' when the modulator is enabled. Fixed at '0' otherwise.
DAC_CLK_OUT	Output sampling clock for Digital to Analog Converters. DAC reads the output sample at the rising edge.
CLK_OUT	40 MHz output reference clock. Generated by dividing the internal processing clock: f_{clk} /2

Modulator Digital Output Interfaces (J5) (Output data pulled)	Definition
TX_SAMPLE_CLK_REQ_IN	Input. 100 MHz clock requesting output samples.
TX_DATA_OUT[13:0]	Output. Quadrature baseband samples, 14-bit precision, 2's complement format. Bit 13 is the most significant bit. The in-phase (I) and quadrature (Q) samples alternate. Output samples are synchronous with the falling edge of SAMPLE_CLK_REQ_IN.
TX_ENABLE	Output. Transmit enable. Active high. The first sample after TX_ENABLE becomes active is an in-phase (I) sample.
Modulator Analog Output Interfaces (J7)	**Definition**
TX_I_P / TX_I_N	I-channel differential outputs. (_P for +, _N for -). Full range 2Vpp differential (1Vpp on each TX_I_P and TX_I_N signal). Common mode voltage is approximately 1V. Output impedance 100 Ohm.
TX_Q_P / TX_Q_N	Q-channel differential outputs. (_P for +, _N for -). Same electrical characteristics as above.
TX_GAIN_CNTRL1	Transmitter gain control. Analog output in the range 0 – 3.3V. Non-linear scale., see the transceiver specifications. 0V yield the minimum gain.
TX_ENB	Transmitter enable. LVTTL output signal. '1' when the modulator analog output is enabled, '0' otherwise.
RX_TXN	Receive/Transmit# selection. LVTTL output signal. '0' = transmit '1' = receive. Transmit is on when the modulator analog output is enabled.

Other Digital Modem Interfaces	Definition
USB 2.0	Type B receptacle. This interface supports two virtual channels: one for monitoring and control, the other to convey information data between the modem and a host computer.
LAN (COM-1203)	4 wire. 10Base-T/100Base-TX. RJ45 connector. NIC wiring. Use standard category 5 cable for connection to a Hub/Switch. Use crossover cable for connection to a host computer. This interface supports three virtual channels: one for monitoring and control, the two other to convey demodulated data from the two demodulators back to a host computer.

Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the symbol clock rate (f_{symbol_clk}). The maximum power consumption is TBDmA.

Important: Digital I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- USB
- TCP-IP/LAN (COM-1203)

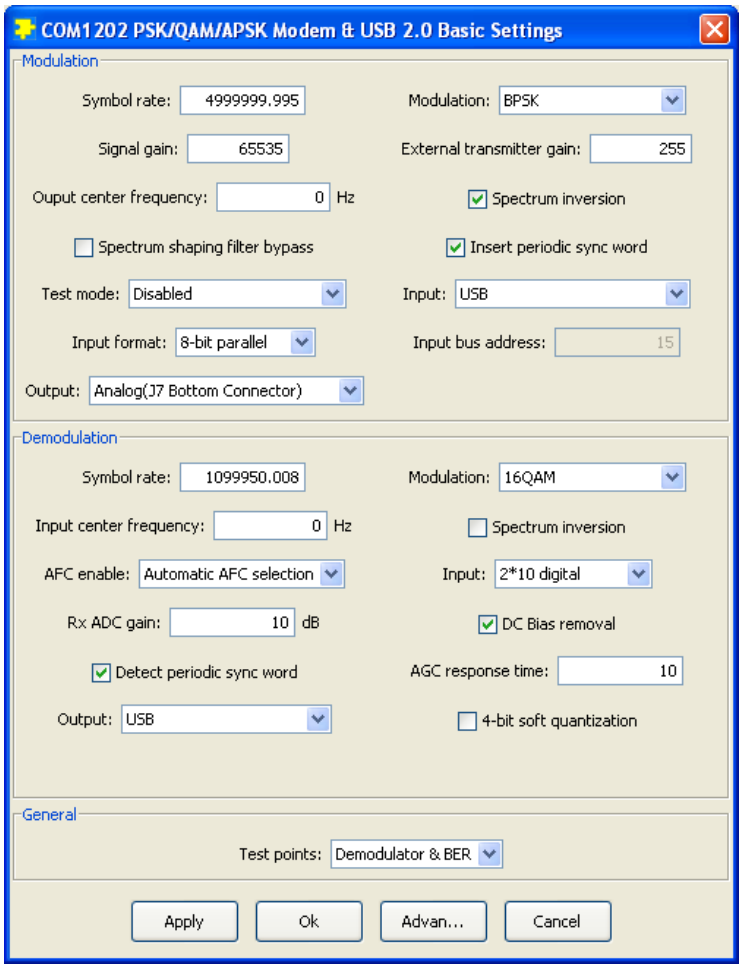
or connections via adjacent ComBlocks:

- USB
- TCP-IP/LAN,
- Asynchronous serial (DB9)
- PC Card (CardBus, PCMCIA).

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1202/3 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1202/3 module to be configured, next click the *Settings* button to display the *Settings* window shown below.



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

This module operates at a fixed internal clock rate f_{clk} of 90 MHz.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

PSK/QAM/APSK Modulator	
Parameters	**Configuration**
Symbol rate (f_{symbol_clk})	32-bit unsigned integer expressed as fsymbol rate * 2^{32} / f_{clk}. The maximum symbol rate is $f_{clk}/4$ (0x3FFFFFFF). However, in practice it is recommended to limit the maximum symbol rate to 0.99*($f_{clk}/4$) to account for possible clock drifts between modulator and demodulator. The data rate is between 1x and 6x the symbol rate depending on the modulation type. REG0 = bits 7-0 (LSB) REG1 = bits 15 – 8 REG2 = bits 23 – 16 REG3 = bits 31 – 23 (MSB)
Modulation type	0 = BPSK 1 = QPSK 2 = OQPSK 3-7 = reserved for future QPSK constellations 8 = 8PSK constellation 8A 9 = 8PSK constellation 8B 10 = 8PSK constellation 8C 11 = 8PSK constellation 8D 12 = π/4 DQPSK (differential QPSK) 13-15 = reserved for future 8PSK constellations 16 = 16QAM 17-23 reserved for future 16QAM constellations. 24 = 16APSK, DVB-S2, γ = 2.85 25-31 reserved for future 16APSK 32 = 32APSK, DVB-S2, γ1 = 2.84, γ2 = 5.27 33-39 reserved for future 32APSK REG4 bits 5-0
Spectrum inversion	Invert Q bit. This is helpful in compensating any frequency spectrum inversion occurring in a subsequent RF frequency translation. 0 = off 1 = on REG4 bit 6
Channel filter enabled	0 = enable the root raised cosine filter (general case) 1 = bypass the root raised cosine filter (special use in applications when a root raised cosine filter is not used in the demodulator.) REG4 bit 7
Test mode	00 = disabled 01 = internal generation of 2047-bit periodic pseudo-random bit sequence as modulator input. (overrides external input bit stream). 10 = unmodulated carrier. (overrides external input bit stream) REG5 bits 1-0
Tx unique word	Insert periodic 32 bit unique word (synchronization sequence) to assist the demodulator in synchronizing and recovering ambiguities. The unique word is 5A 0F BE 66, transmitted MSb first. 2048 data symbols are transmitted between successive unique words. The unique word is using a simplified BPSK modulation, irrespective of the modulation type. 0 = disabled 1 = periodically insert a Unique word. REG5 bit 3
Input format	Input sample width. 00 = 1-bit serial 01 = symbol parallel, where N input bits are read at once. N is the number of bits per symbol (1 for BPSK, 2 for QPSK, 3 for 8-PSK, 4 for 16-QAM and 16-APSK, 5 for 32-APSK, etc). 10 = 8-bit parallel. MSb is to be transmitted first. REG5 bits 5-4
Input selection	Select the origin of the modulator input data stream. 0000 = from left J4 connector, direct point to point connection (most ComBlocks) 0100 = from right J5 connector xx01 = from USB xx10 = from LAN/TCP-IP, port 1024 (**COM-1203**) xx11 = bus interface through left connector (COM-8004 interface) REG5 bits 7-6 (two LSbs) REG9 bits 1-0 (two MSbs)
Signal gain	Signal level. 16-bit unsigned integer. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Therefore, we recommend checking for saturation at test point TP4 (or using ComScope for example) when changing either the symbol rate or the signal gain. REG6 = bits 7-0 (LSB) REG7= bits 15-8 (MSB)

External transmitter gain control	When using an external transmitter such as the COM-350x family, the transmitter gain can be controlled through the J7/TX_GAIN_CNTRL1 analog output signal. Range 0 – 3.3V. REG8 = bits 7-0.
Output Center frequency (fcout)	Frequency translation. 32-bit signed integer (2's complement representation) expressed as fcout * 2^{32} / $\mathbf{f_{clk}}$. Maximum recommended range: ± 10 MHz. REG16 = bits 7-0 (LSB) REG17 = bits 15 – 8 REG18 = bits 23 – 16 REG19 = bits 31 – 23 (MSB)
Output selection	Direct the modulator output to one of several possible interfaces: 000 = analog output (J7 bottom connector). Enables the external transmitter through J7/TX_ENB = '1'. Disable the external receiver through J7/RX_TXN = '0'. 001 = digital 2*10-bit precision unsigned, J5 right connector. Interfaces with COM-2001 dual D/A converter. Sampling rate: 90 Msamples/s. ($\mathbf{f_{clk}}$) 010 = digital, 2*14-bit precision, signed, J5 right connector. Compatible with COM-4004. Note: this field selects whether an analog transceiver connected to J7 will be configured as transmitter (000) or receiver (any other value). REG20 bits 2-0
Input/Output Bus address	Unique 4-bit address identifying this module on the input bus (if the input bus is enabled in REG5 bits 7-6). Ignore otherwise. This module acts as bus slave: it performs the read/write transaction requested by the bus master if and only if the bus address matches its own address defined here. This address must be unique among modules connected to the same bus in order to avoid conflicts. Same field is used for modulator input bus address and demodulator output bus address. REG21 bits 3-0

PSK/QAM/APSK Demodulator	
Parameters	**Configuration**
Nominal symbol rate ($\mathbf{f_{symbol\_clk}}$)	32-bit unsigned integer expressed as $\mathbf{f_{symbol\_clk}}$ * 2^{32} / $\mathbf{f_{clk}}$. The maximum symbol rate is $\mathbf{f_{clk}}$/4 (0x3FFFFFFF). The data rate is between 1x and 6x the symbol rate depending on the modulation type. Max: 22 MSymbols/s. Min: use at symbol rates below 100 KSymbols/s is possible but can be complex because of effects such as of external local oscillator phase noise, frequency acquisition, oscillator stability, microphonics, etc. REG26 = bits 7-0 (LSB) REG27 = bits 15 – 8 REG28 = bits 23 – 16 REG29 = bits 31 – 23 (MSB)
Nominal Center frequency ($\mathbf{f_c}$)	Expected center frequency of the received signal. 32-bit signed integer (2's complement representation) expressed as $\mathbf{f_c}$ * 2^{32} / $\mathbf{f_{clk}}$. Maximum recommended range: ± 10 MHz. REG30 = bit 7-0 (LSB) REG31 = bit 15 – 8 REG32 = bit 23 – 16 REG33 = bit 31 – 23 (MSB)
Modulation type	0 = BPSK 1 = QPSK 2 = OQPSK 3-7 = reserved for future QPSK constellations 8 = 8PSK constellation 8A 9 = 8PSK constellation 8B 10 = 8PSK constellation 8C 11 = 8PSK constellation 8D 12 = π/4 DQPSK (differential QPSK) 13-15 = reserved for future 8PSK constellations 16 = 16QAM 17-23 reserved for future 16QAM constellations. 24 = 16APSK, DVB-S2, γ = 2.85 25-31 reserved for future 16APSK 32 = 32APSK, DVB-S2, γ1 = 2.84, γ2 = 5.27 33-39 reserved for future 32APSK REG34 bits 5-0

Spectrum inversion	Invert Q bit. This is helpful in compensating any frequency spectrum inversion occurring during RF frequency translations. 0 = off 1 = on REG34 bit 6
reserved	00 REG35 bits 1-0
AFC enable	The automatic frequency control circuit extendeds the frequency acquisition over +/- 10% of the symbol rate. When disabled, the receiver only means of carrier acquisition is the carrier frequency tracking loop which is inherently limited to approximately 1% of the symbol rate. The AFC should only be active during acquisition as it interferes with the Costas Loop operation. 00 = automatic AFC selection. 01 = force AFC disabled. Carrier tracking loop only 10 = force AFC enabled. 11 = reserved (test). REG35 bits 3-2
Reset	A one-time write of '1' forces the carrier loops (carrier PLL, AFC) back into acquisition mode. This can be used to get out of any potential false lock condition. There is no need to clear this bit. REG35 bit 7
Input selection	00 = digital 2 * 12-bit unsigned samples, left J4 connector 01 = IF undersampling interface, bottom J7 connector, I-channel only. 10 = baseband analog interface, bottom J7 connector. 11 = loopback mode modulator -> demodulator REG36 bits 1-0
Rx ADC gain	Analog signals prior to the built-in A/D converter can be amplified by steps of about 1 dB. This 5-bit unsigned integer controls the variable gain between 0 and 20 dB. Applies equally to the I and Q channels. When the COM-1202/1203 is used in conjunction with the COM-3501 UHF transceiver, a settings of 16 (x10) is recommended. Please note that setting the gain too low may cause the AGC to stop working. REG36 = bits 6-2

DC bias removal	Enable or disable the DC bias removal circuit at the input. May be helpful in cases where the external analog-to-digital converters introduce unwanted DC bias. Bias is averaged over approximately 1024 symbols. If the modulated data is not random over this averaging period, or if the modulation index is very small, it is recommended to disable the DC bias removal. 0 = disabled/bypassed 1 = enabled REG37 bit 0
Unique Word Synchronization detection	0 = disabled 1 = enabled Enable when the modulator sends a periodic synchronization sequence. The demodulator inherent phase ambiguity can only be removed if this feature is enabled at both modulator and demodulator. REG37 bit 1
AGC1 response time	Users can to optimize AGC1 response time while avoiding instabilities (depends on external factors such as gain signal filtering at the RF front-end and symbol rate). The RX_AGC1 analog gain control signal is updated as follows 0 = every symbol, 1 = every 2 symbols, 2 = every 4 symbols, 3 = every 8 symbols, etc…. 20 = every 1 million symbols. Valid range 0 to 20. REG37 bits 6-2
Output selection	000 = USB 001 = TCP-IP (**COM-1203**) 010 = synchronous serial J5 right connector (**COM-1202**) 011 = synchronous serial J4 left connector 100 = synchronous serial J9 connector used as demodulator output instead of test points. 101 = bus interface through J5 right connector (COM-8003 interface) 110 = demodulated complex (I+Q) baseband signal to J5 right connector. Interface compatible with an external COM-2001 dual D/A converter. Format: 2*10-bit precision, 90 MHz synchronous clock, 4 samples per symbol. REG38 bits 2-0

Output format	Users may have to tradeoff throughput versus soft-quantization when using the USB 2.0 or TCP-IP connection as media to route demodulated data to a host computer. Demodulated data can be transmitted as 1-bit 'hard-quantized or 4-bit soft-quantized samples. Due to throughput limitation on these media, the maximum demodulated data rate may only be available as 1-bit 'hard-quantized' samples. No such limitation exists when using the synchronous serial output format. 0 = 1-bit hard quantized samples 1 = 4-bit soft quantized samples REG38 bit 3
Test Points	In order to help debug a system, the test points can be focused on a specific subsystem: 00 = demodulator & BER measurement 01 = modulator REG38 bits 5-4
IP address (**COM-1203**)	4-byte IP address. Example : 0x AC 10 01 80 designates address 172.16.1.128 The new address becomes effective immediately (no need to reset the ComBlock). REG39: MSB REG40 REG41 REG42: LSB
10Base-T / 100Base-TX LAN selection (**COM-1203**)	00 = 10Base-T 01 = 100Base-TX 10 = Auto negotiation Changes will take effect at the next power up. REG43 bits 1-0
Half / Full duplex LAN link (**COM-1203**)	Half-duplex is a safe configuration which can be used with older networking equipment. Full duplex results in higher throughput but may be incompatible with unswitched hubs. 0 = half-duplex 1 = full duplex. Changes will take effect at the next power up. REG43 bit 2
Reserved	REG44 through 49 are reserved for the LAN MAC address. These registers are set at the time of manufacturing.

(Re-)Writing to control register REG38 is recommended after a configuration change to enact the change (Note: this is done automatically when using the graphical user interface).

Baseline configurations can be found at www.comblock.com/tsbasic_settings.htm and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

Status Registers

Digital status registers are read-only.

PSK/QAM/APSK Demodulator Monitoring	
Parameters	**Monitoring**
Carrier frequency offset (fcdelta)	Residual frequency offset with respect to the nominal carrier frequency. 24-bit signed integer (2's complement) expressed as fcdelta * 2^{24} / fsymbol rate. SREG10 = bit 7 – 0 SREG11 = bit 15 – 8 SREG12 = bit 23 – 16
Received signal magnitude after channel filtering	8-bit unsigned SREG13 bit 7-0.
Carrier tracking loop lock status	Lock is declared if the standard deviation of the phase error is less than 25deg rms. 0 = unlocked 1 = locked SREG14 bit 0
Front-end AGC	8-bit unsigned value prior to DAC conversion to RX_AGC1. SREG15 bits 7-0.
Bit errors	When the transmission of periodic unique words is enabled, the demodulator can count the number of bit errors over 1024 received bits. This BER measurement method works even while transmitting regular payload data (no need to switch the transmitter to the PRBS-11 test mode). This BER may be better than the payload data BER because it is performed on a simpler (BPSK) modulation. SREG16 bits 7-0 (LSB). SREG17 bits 1-0 (MSbs).

BER Measurement	
Parameters	**Monitoring**
Bit Errors	Bit errors can be counted when a PRBS-11 test sequence is transmitted. Number of bit errors in a 1,000,000 bit window. 32 bit unsigned. SREG20: error_count[7:0] SREG21: error_count[15:8] SREG22: error_count[23:16] SREG23: error_count[31:24] The bit errors counter is updated once every periodic measurement window. Reading the value will not reset the counter.
BER Synchronization status	0 = not synchronized. 2047-bit pattern is not detected. 1 = synchronized SREG24 bit 0.
n-PSK Phase ambiguity. Cycle slip detection.	Number indicating the phase offset between modulated and demodulated data streams. A change in phase offset denotes a cycle slip. The phase offset is expressed as 00 = 0 deg 01 = +90 deg 10 = +180 deg 11 = +270 deg SREG24 bits 2-1
TCP-IP Connection Monitoring	
Parameters	**Monitoring**
TCP-IP connection on port 1024 (data stream)	1 = connected, 0 otherwise. SREG30 bit 0
TCP-IP connection on port 1028 (Monitoring & Control)	1 = connected, 0 otherwise. SREG30 bit 2
Number of bytes received from demodulator and forwarded to host over TCP-IP/LAN	32-bit byte count. Counter rolls over when reaching 0xFFFFFFFF. SREG31: bits 7-0 (LSB) SREG32: bits 15-8 SREG33: bits 23-16 SREG34: bits 31-24 (MSB)
MAC address	Unique 48-bit hardware address (802.3). In the form SREG35:SREG36:SREG37:…:SREG40

ComScope Monitoring

Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-1202/1203 signal traces and trigger are defined as follows:

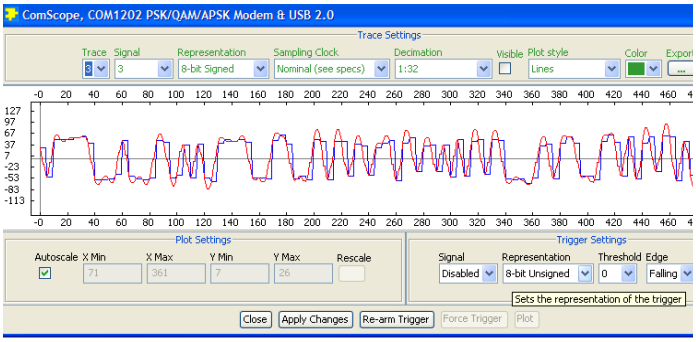
Trace 1 signals (demod)	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: Input I signal	8-bit signed	f_{clk}	512
2: I signal after frequency translation to baseband	8-bit signed	f_{clk}	512
3: I signal after decimation & root raised cosine filtering	8-bit signed	4 samples /symbol	512
4: reserved			
5: Bit Error Rate averaged over 1Mbit window. Range: 0 – 50% by steps of 2.10^{-3}	8-bit unsigned	f_{clk}	512
Trace 2 signals (demod)	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: Input Q signal	8-bit signed	f_{clk}	512
2: Demodulated I signal at optimum sampling instant (compare with Trace 1 Signal 3)	8-bit signed	1 sample /symbol	512
3: cumulative symbol timing error	8-bit signed	symbol rate	512
4: front-end AGC RX_AGC1	8-bit unsigned	AGC update rate	512
5: reconstructed carrier phase	8-bit unsigned	f_{clk}	512
Trace 3 signals (modulator)	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: serial bit stream	8-bit signed	Bit rate	512
2: modulator symbol (I-channel) before	8-bit signed	f_{symbol_clk}	512

channel filter. Ideal constellation			
3: baseband Q-channel modulator output (after channel filter, before frequency translation and interpolation)	8-bit signed	$4*f_{symbol\_clk}$	512
4: modulator output (I-channel) after frequency translation & interpolation	8-bit signed	f_{clk}	512
Trace 4 signals (modulator)	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: symbol stream	8-bit signed	f_{symbol_clk}	512
2: modulator symbol (Q-channel) before channel filter. Ideal constellation	8-bit signed	f_{symbol_clk}	512
3: baseband I-channel modulator output (after channel filter, before frequency translation and interpolation)	8-bit signed	$4*f_{symbol\_clk}$	512
4: modulator output (Q-channel) after frequency translation & interpolation	8-bit signed	f_{clk}	512
Trigger Signal	**Format**		
1: demodulated start of frame (SOF)	1-bit		
2: demodulated start of test PRBS-11 sequence	1-bit		
3: start of PRBS-11 test sequence at modulator	1-bit		
4: Unique word symbol insertion at modulator	1-bit		

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk} processing clock as real-time sampling clock.

In particular, selecting the f_{clk} processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope Window Sample: showing QPSK I-channel after root raised cosine filter, AGCs and phase correction 4x oversampling (red) and sampled at the optimum sampling instant once per symbol (blue).

Digital Test Points

Test points TP1 through TP10 are generally routed to the J9 10-pin 0.1" connector.

Note: Test points are disabled when the user selects the J9 connector to route output data streams to external devices using a ribbon connector. See control register REG38(2:0).

Four sets of test points are multiplexed onto the 10-pin J9 connector, as selected through control register REG38(5:4) .

PSK/QAM/APSK Demodulator Test Points	
TP1	Carrier lock status
TP2	Frame synchronization lock status (most reliable lock status, but valid only if the modulator is configured to send a periodic SOF frame synchronization sequence)
TP3	Recovered carrier (carrier NCO output MSB). Includes the fixed offset defined by the user as Nominal Center Frequency
TP4	Recovered symbol clock. Compare with modulator symbol clock.
TP5	Start of frame (SOF)
TP6	Raw SOF output from matched filter upon detection of the periodic unique word.
TP7	reserved
TP8	BER measurement: Synchronization (BER test points are valid only if a PRBS-11 test sequence is transmitted)
TP9	BER measurement: Bit error
TP10	BER measurement: Start of PRBS-11 periodic test sequence detected with less than 10% bit errors.
PSK/QAM/APSK Modulator Test Points	
TP1	PRBS-11 test sequence
TP2	PRBS-11 periodic start of test sequence
TP3	Modulator Symbol rate.
TP4	Saturation at modulator output. If this condition occurs, please reduce the modulator gain.
TP5 – TP10	undefined
Other test points	
DONE	'1' indicates proper FPGA configuration.
INITB	Reference clock f_{clk} / 8 = 11.25 MHz.

Operation

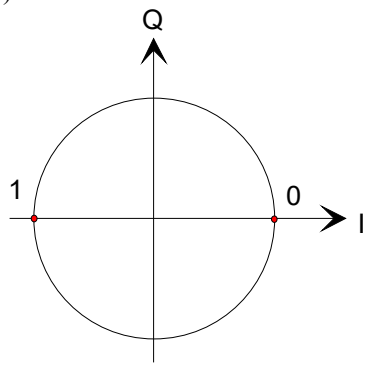
This PSK/QAM/APSK modem is a generic modem. It does NOT comply with the DVB-S2 (ETSI EN 302 307) physical layer specifications.

Constellation: Symbol Mapping

The packing of serial data stream into symbols is done with the Most Significant bit first.

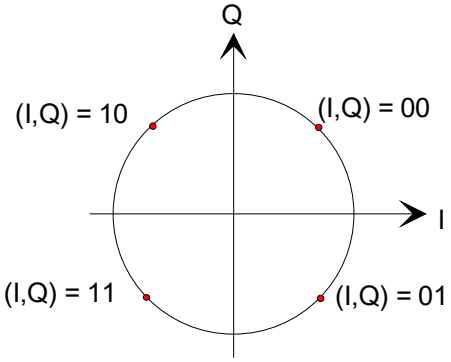
BPSK

REG31(5:0) = 0



QPSK

REG31(5:0) = 1
Gray encoding.



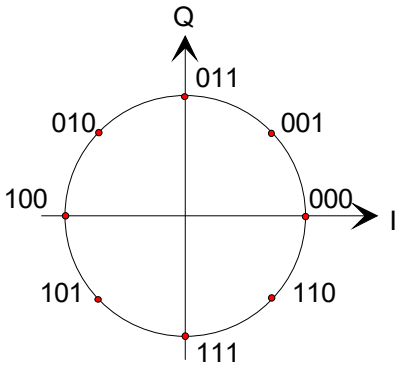
π/4 DQPSK

REG31(5:0) = 12

Input symbol	Phase shift
00	+ π/4
01	+ 3π/4
10	- π/4
11	-3π/4

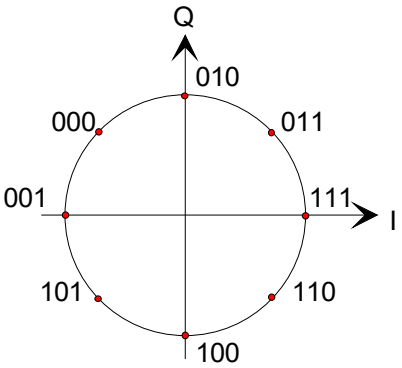
8PSK (1)

REG31(5:0) = 8



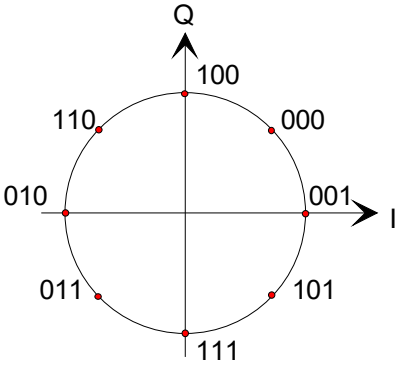
8PSK (2)

REG31(5:0) = 9



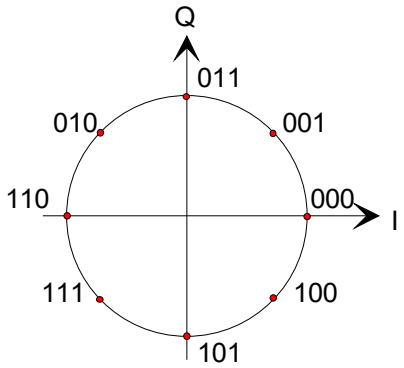
8PSK (3)

REG31(5:0) = 10
Gray encoded.



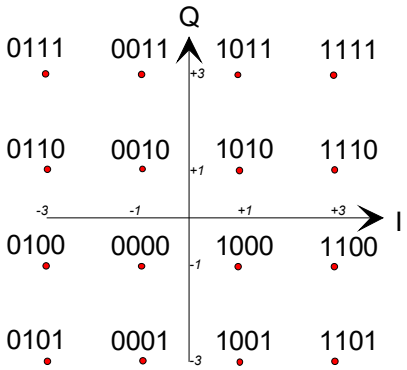
8PSK (4)

REG31(5:0) = 11



16QAM

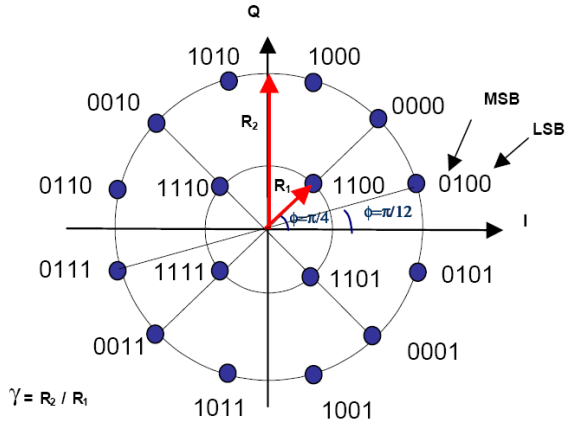
REG31(5:0) = 16



16APSK

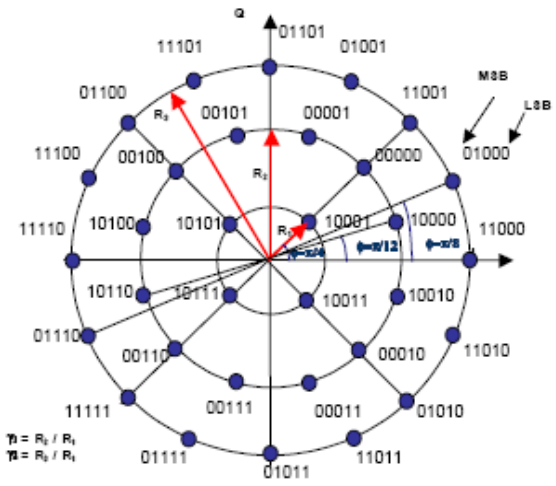
REG31(5:0) = 24

$\gamma = R2 / R1 = 2.85$, best for code rate 3/4



32APSK

REG31(5:0) = 32
γ1 = 2.84, γ2 = 5.27, best for code rate 3/4



Channel Filter Response

The same root raised cosine filter type is used at the modulator for spectral shaping and at the receiver for noise rejection. This filter is used for all modulations types. It is applied to both In-phase and Quadrature signals at baseband. The filters vary slightly by their 'rolloff factor'. In order to minimize intersymbol interferences, the same rolloff factor should be used at both the modulator and demodulator. To this effect, users can select one of several rolloff factors: 20%, 25%, 35% and 40%. Changing the rolloff selection requires loading the firmware once using the ComBlock control center, then switching between up to four stored firmware versions (it takes 2.2 seconds).

The four firmware versions can be downloaded from www.comblock.com/download.

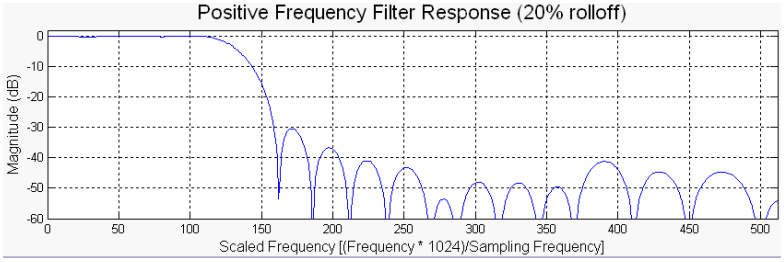
COM-1202-A 20% rolloff

COM-1202-B 25% rolloff

COM-1202-D 35% rolloff

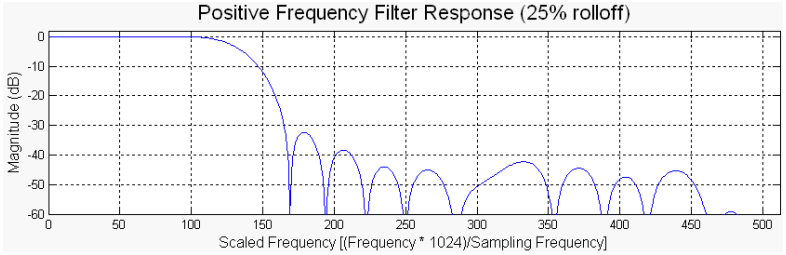
COM-1202-E 40% rolloff

Filter Response (-A 20% rolloff)



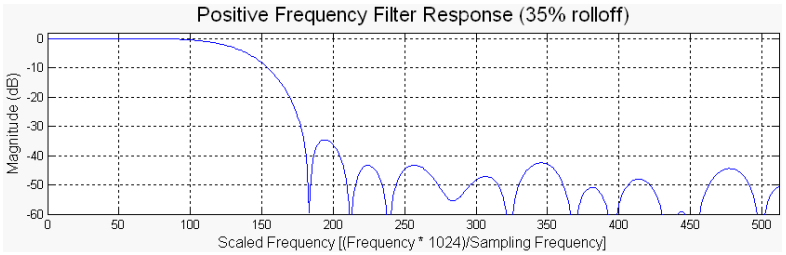
*(filter response normalized. 512 = 2*symbol rate)*

Filter Response (-B 25% rolloff)



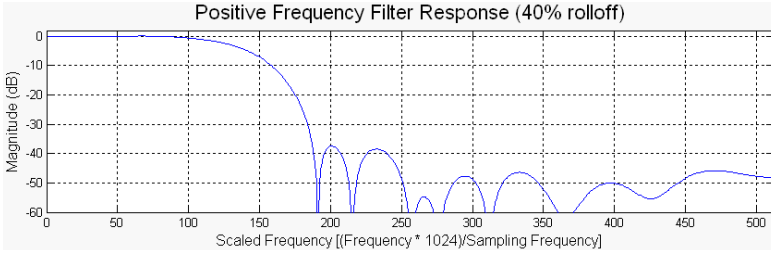
*(filter response normalized. 512 = 2*symbol rate)*

Filter Response (-D 35% rolloff)



*(filter response normalized. 512 = 2*symbol rate)*

Filter Response (-E 40% rolloff)



*(filter response normalized. 512 = 2*symbol rate)*

AGC1

The purpose of this AGC is to prevent saturation at the input signal A/D converters while making full use of the A/D converters dynamic range.

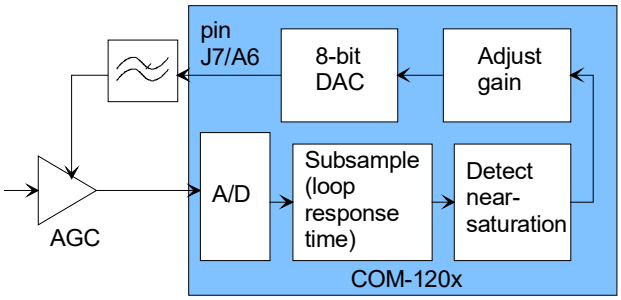
Therefore, AGC1 reacts to the composite input signal which may comprise not only the useful signal but also adjacent channel interferers and noise. The principle of operations is outlined below:

(a) Digital input samples are first subsampled according to the user-defined AGC1 response time.

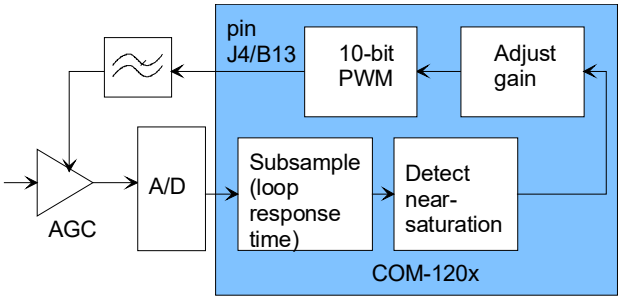
(b) Near-saturation events are detected from the subsampled digital input samples and the AGC gain is adjusted accordingly.

(c) An 8-bit D/A converter generates the analog gain control signal RX_AGC1 for use by the external variable gain amplifiers. (pin J7/A6, bottom connector)

(d) Alternatively, a 10-bit Pulse-Width Modulated digital signal is also routed to pin J4/B13 (left connector) for use by an external variable gain amplifier.



AGC1 principle (analog output)



AGC1 principle (digital output)

Input Signal Pre-Processing

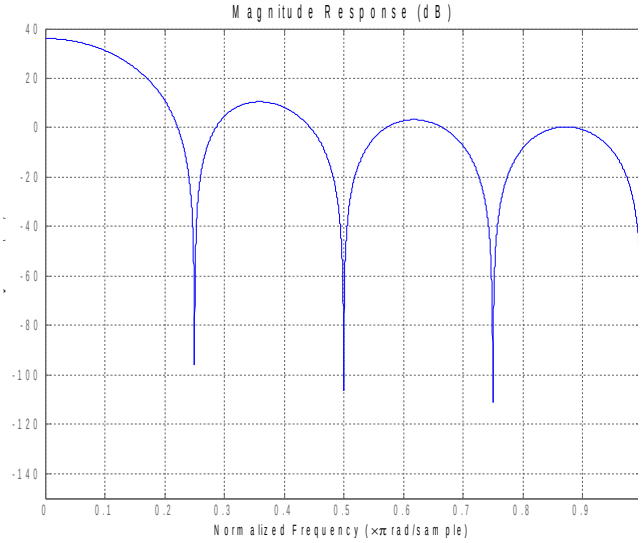
Prior to being routed to the demodulator, the input signal is subject to AGC1, variable decimation, and frequency translation to near-zero frequency.

Variable Decimation (Receiver)

Prior to the Root Raised Cosine channel filter, several other filters are used to reject wideband noise and adjacent channel interferences while decimating the input signal:

- two 10-taps half-band FIR filters in series
- a Cascaded Integrated Comb (CIC) filter The decimation rate R is set automatically as the largest value R such that *R < (input sampling rate) / (8*symbol rate).* The number of stages N and the differential delay M are fixed at 2 and 1 respectively.

An example of CIC filter response is shown below:
X-axis is [0,input sampling frequency/2]
Y-axis is the magnitude response in dB.



N = 2, M = 1, R = 8

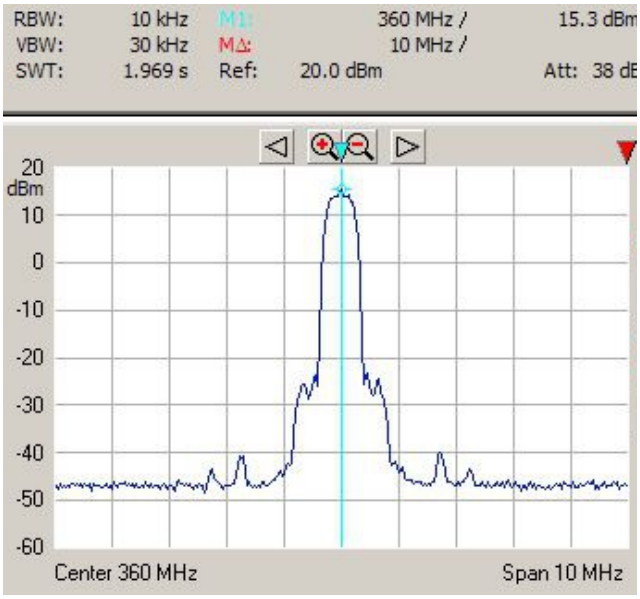
Matlab functions:
hm = mfilt.cicdecim(r,m,n,ibits,obits,bps);
fvtool(hm);

Variable Interpolation (Transmitter)

Following the Root Raised Cosine channel filter at the modulator, several other filters are used to clean the out-of-band output spectrum:

- two 10-taps half-band FIR filters in series
- a CIC interpolation filter.The interpolation factor R is set automatically.

The effect of the interpolation are illustrated below in the case of a 500 KSymbols/s QPSK modulation. The spectrum is captured at the output of a COM-3501 UHF transceiver.

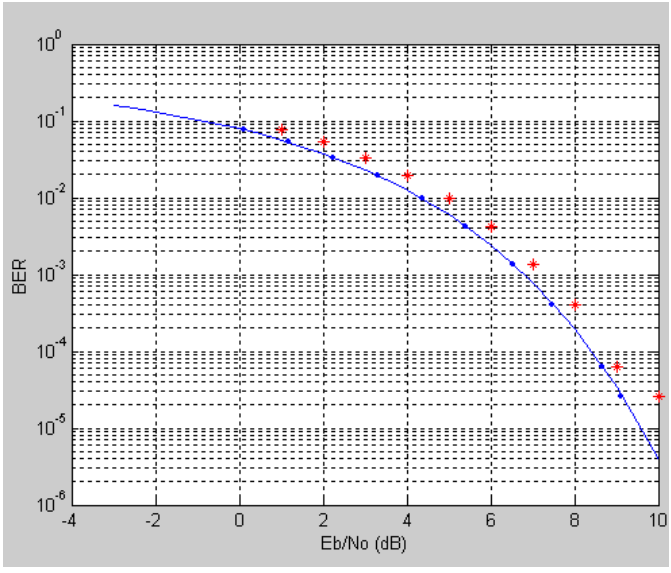


Output spectrum with R = 40 interpolation.
QPSK, 500 KSymbols/s.

Bit Error Rate Performances

The demodulator bit-error-rate performances are within 0.5 dB from the theoretical performances ½ * erfc(E_b/N_o) of PSK demodulators over a wide range of E_b/N_o. Actual measurements (inclusive of the 70 MHz modulator and receiver) are shown below. The test conditions were as follows:

- ComBlock assembly: COM-1202 with 70 MHz modulator (COM-4004) and wideband receiver (COM-3004-B)
- Wideband 100 MHz noise
- QPSK, 4 Mbits/s



BER performance Theory(blue)/Actual(red)

LAN / TCP-IP (*COM-1203*)

Initial Configuration (via Serial Link)

The IP address must first be configured over non-TCP-IP connections such as USB or through other ComBlocks. This network setting is saved in non-volatile memory (see control registers REG38-41). The TCP-IP connection can be used once the correct network setting is configured and after a COM-1203 power cycle.

TCP-IP

As a Server, the module opens the following sockets in listening mode:

Port 1024: modem data streams
Port 1028: monitoring and control port

IP Protocols

This module supports the following IP protocols:

- Ping
- ARP
- TCP-IP

Ping

The module responds to ping requests with size up to 470 bytes. Ping can be used to check the module response over the network. Ping can be used at any time, concurrently with other transmit and receive transactions. For example, on a Windows operating system, open the Command prompt window and type "ping –t –l 470 172.16.1.128" to send pings forever of length 470 bytes to address 172.16.1.128.

Concept

The COM-1203 converts a serial data stream into a TCP-IP socket stream. TCP, IP and Network information, and in particular routing information, are not transmitted from one end to the other.

At the receiving end, the network client must first connect to the COM-1203 to receive data.

A key assumption is that the network client is reading as fast as the demodulator(s) can forward demodulated data. If not, data will be lost. The demodulated data is stored within a 16 Kbit elastic buffer within the COM-1203. This buffer size determines the maximum interruption for which the network client (operating system) can temporarily stop reading data. For example, for a 1 Mbit/s data stream, the maximum interruption allowed is 16.384 ms.

Throughput Benchmarks

The COM-1203 is capable of a sustained (average) throughput of 50 Mbits/s over 100base-Tx. In most cases, the sustained throughput is limited by the TCP-IP client computer and the application running on the client computer as illustrated in the one-way data transfer benchmark below:

Throughput tests conditions	Throughput
Client: Intel Pentium 4 2.6 GHz running winsock-based console application. Connection over LAN switch. No other network connection. No other application running. COM-1203 configured as 'Auto Negotiation". 100Base-Tx connection.	41 Mbits/s min 54.7 Mbits/s max 100 Mbytes received in 16.0 seconds.

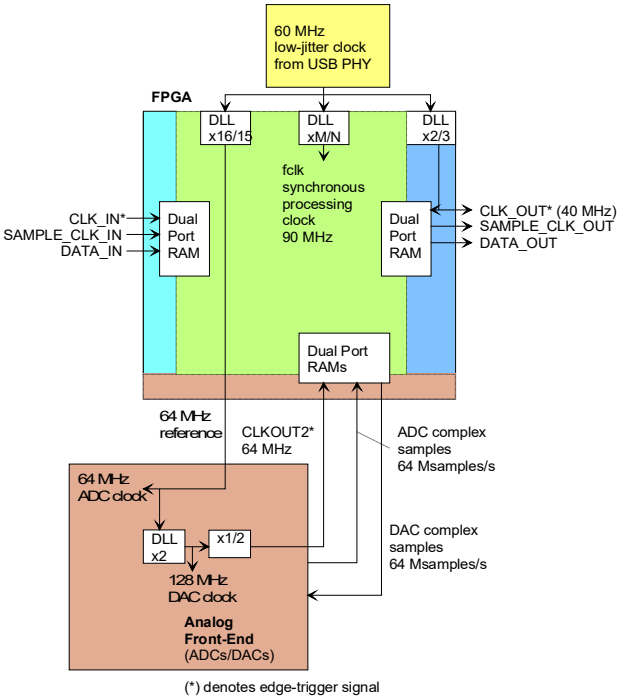
Format Conversion

Serial to parallel conversion occurs when converting the demodulated data stream into 8-bit byte over the TCP-IP link. The key rule is that the first received bit is placed at the MSb position in the byte.

Timing

Clocks

The clock distribution scheme embodied in the COM-1202/1203 is illustrated below.



Baseline clock architecture
Yellow = 60 MHz reference clock
Green = f_{clk} processing zone 90 MHz
Dark Blue = output clock(40/90 MHz)
Light Blue = external input clock
Brown = 64 MHz I/O zone

The core signal processing performed within the FPGA is synchronous with the processing clock $\mathbf{f_{clk}}$. In order to minimize clock jitter, the processing clock is derived from a 60 MHz reference clock with low-jitter. $\mathbf{f_{clk}}$ is not related to the CLK_IN clock. $\mathbf{f_{clk}}$ is used for internal processing and for generating the output clock CLK_OUT.

The signals at the digital input connector J4 are synchronous with the CLK_IN signal at J4/A1.

The signals at the digital output connector J5 are synchronous with the 40 MHz CLK_OUT signal derived from the 60 MHz reference clock.

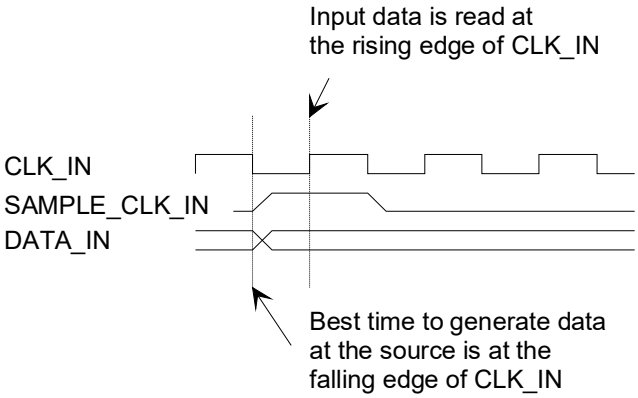
The signals at the analog front-end interface are synchronous with the 64 MHz reference clock generated by the FPGA.

16Kbit dual-port RAM elastic buffers are used at the boundaries between I/Os and internal processing area.

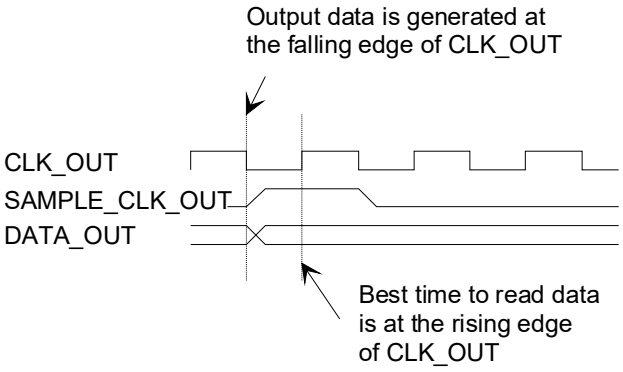
I/Os

All I/O signals are synchronous with a reference clock located on pin A1 of the 40-pin interface connector. The general rule is that the output signals are generated at the falling edge of the synchronous clock while the input signals are read at the rising edge of the synchronous clock, as illustrated in the simplified timing diagrams below.

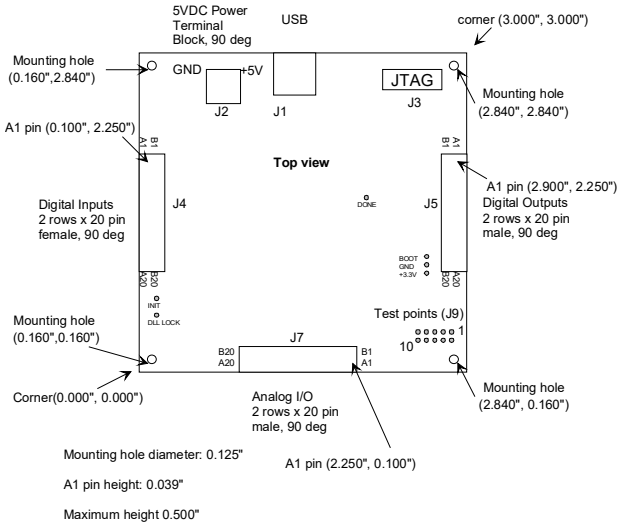
Input



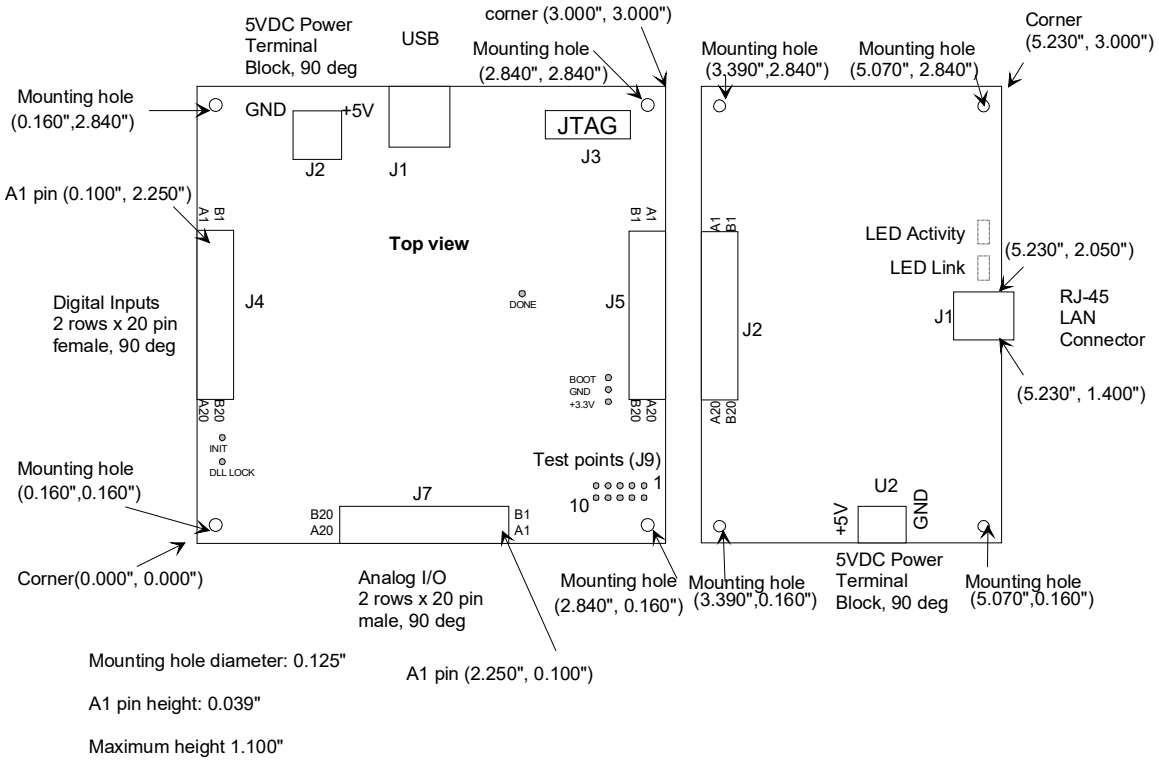
Output



Mechanical Interface



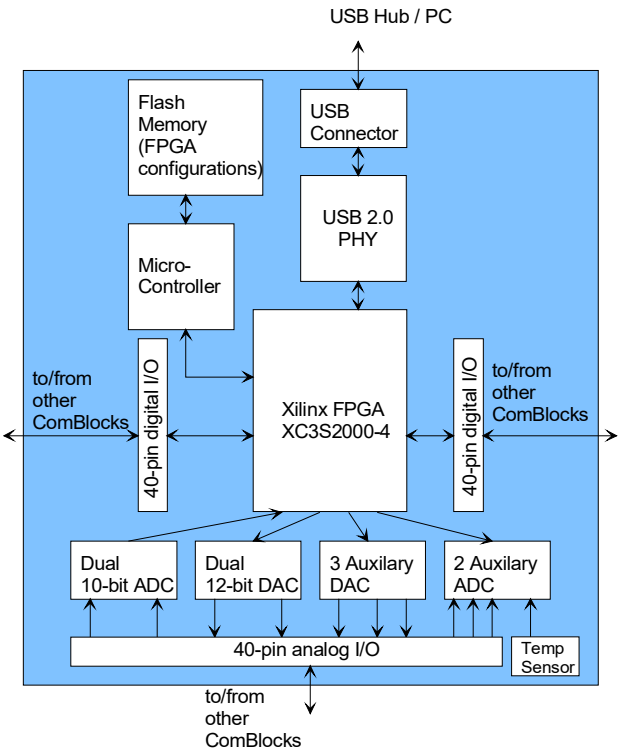
COM-1202



COM-1203

Schematics

The board schematics are available on the ComBlock CD-ROM supplied with the module and on-line at http://www.comblock.com/download/com_1200schematics.zip



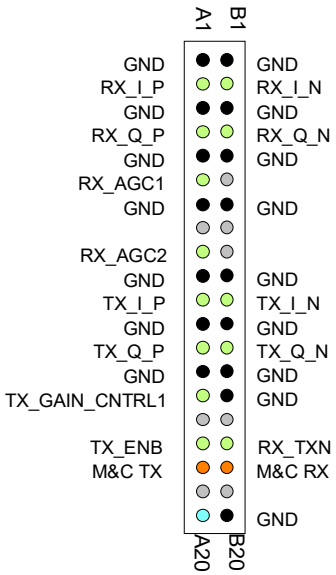
Hardware Block Diagram

Pinout

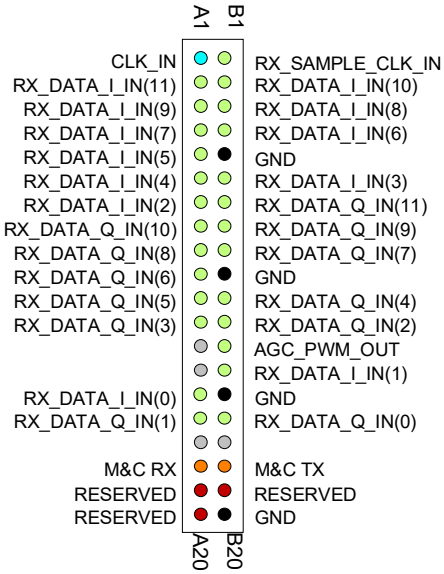
USB

USB type B receptacle, as the COM-1202/1203 is a USB device.

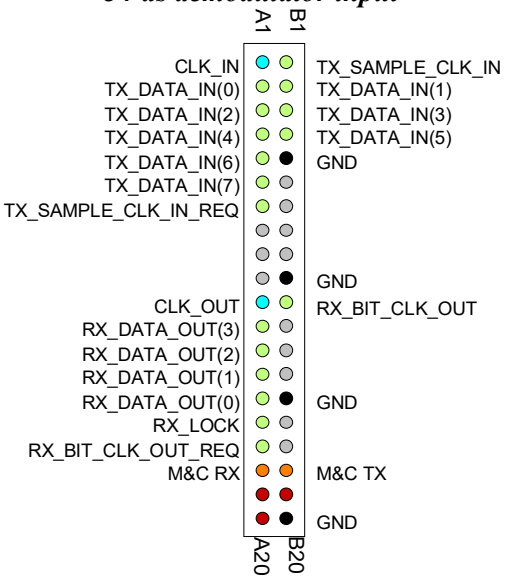
Analog I/O Connector J7



Connector J4

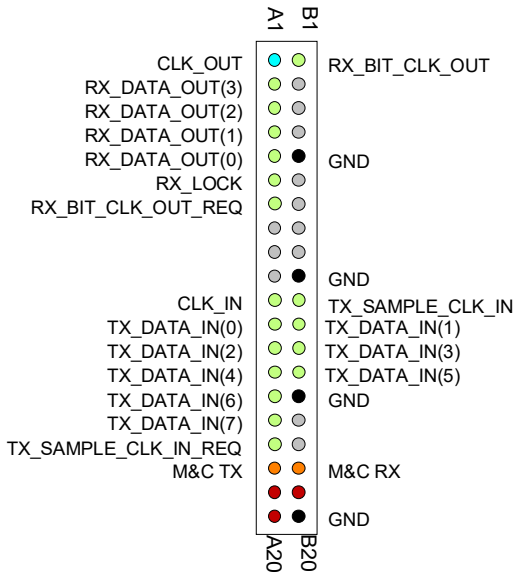


J4 as demodulator input



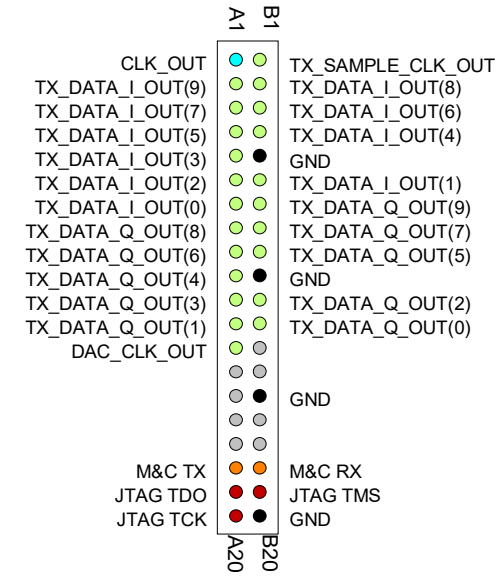
J4 as modulator input / demodulator output

Connector J5



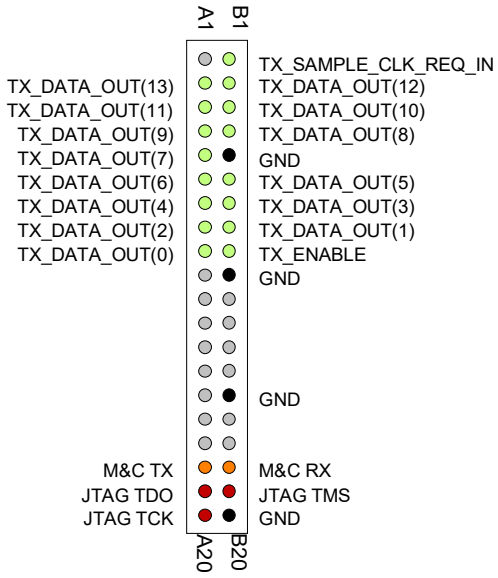
J5 as demodulator output / modulator input

COM-1202 only. Not applicable for COM-1203.



J5 as modulator output (data pushed)

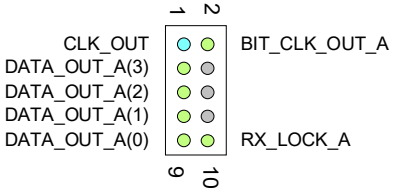
COM-1202 only. Not applicable for COM-1203.



J5 as modulator output (data pulled)

COM-1202 only. Not applicable for COM-1203.

Test/Output Connector J9



The connector pinout shown above is used when a demodulated data streams is routed to the J9 connector (See See Demodulator output selection, REG38(2:0)).

I/O Compatibility List

(not an exhaustive list)

Demodulator Input
COM-300x RF receivers
COM-350x RF transceivers
COM-1023 BER generator, Additive White Gaussian Noise Generator
COM-1024 Multipath simulator.
COM-8001 Arbitrary Waveform Generator, 256 MB/ 1GB, 40 Msamples/s
Demodulator Output
COM-1009 Convolutional decoder K=7
COM-7002 Turbo code encoder/decoder
COM-8002 High-speed data acquisition. 256MB/1GB, 40 Msamples/s.
Host PC via USB 2.0
COM-5003 LAN 10Base-T/100Base-TX / IP network interface
COM-5101 Signal/Power conditioning & RS422 interface

Modulator Input
COM-1010 Convolutional encoder
COM-7002 Turbo code encoder/decoder
Host PC via USB 2.0
COM-5003 LAN 10Base-T/100Base-TX / IP network interface
COM-5101 Signal/Power conditioning & RS422 interface
Modulator Output
COM-2001 Digital-to-Analog Conversion, Baseband
COM-4004 70 MHz IF Modulator
COM-350x RF transceivers
COM-1023 BER generator, AWGN generator
COM-1024 Multipath simulator.
Digital interfaces
COM-1200/1300/1400/8000 FPGA development platforms

Configuration Management

This specification document is consistent with the following software versions:

- COM-1203/1203 FPGA firmware: Version 8 and above.
- ComBlock Control Center graphical user interface: Revision 2.56 and above.

The option and version of the FPGA configuration currently active can be read from the ComBlock Control Center in the configuration panel (advanced).

Troubleshooting

Subpar performance

- Check that the modulator does cause any saturation (saturation causes significant phase errors). Using an oscilloscope, verify that the modulator test point TP4 stays low. If saturation pulses are visible on the oscilloscope, reduce the modulator signal gain until saturation no longer occurs.

  It is a good practice to check for such saturation after changing the symbol rate, the modulation type or the modulator signal gain.
- Check that the receiver gain control loop is stable. The loop stability depends on the symbol rate, on the user-defined AGC1 loop response time and on the external RF receiver. Increase the AGC1 response time until gain oscillations go away.

Comparison with Previous ComBlocks

Key Improvements with respect to COM-1001 BPSK/QPSK/OQPSK demodulator
- Several additional modulations: π/4 DQPSK, 8PSK, 16QAM, 16APSK, 32APSK. - Higher symbol rate (22 versus 10 MSymbols/s). - Built-in digital anti-aliasing filter with variable decimation (no need for COM-1008) - Built-in phase ambiguity removal. - 32-bit numerically controlled oscillators for carrier and symbol timing (versus 24-bit) - Significant increase in center frequency tuning range - Increased frequency acquisition range (to +/- 10% of the symbol rate) by automatic frequency control during acquisition. - Analog or Digital input signals (versus digital-only) - Analog gain control output for fast response (versus slower pulse-width modulated gain control). - User-programmable AGC response time. - Multiple output interfaces: USB2.0, TCP-IP (COM-1203), synchronous serial (versus synchronous serial only) - Built-in BER measurement (no need for COM-1005) - ComScope monitoring of key internal demodulator signals.
Key Improvements with respect to COM-1002 BPSK/QPSK/OQPSK modulator
- Several additional modulations: π/4 DQPSK, 8PSK, 16QAM, 16APSK, 32APSK. - Includes better interpolation filter (CIC).

- 32-bit numerically controlled oscillators for carrier and symbol timing (versus 24-bit)
- Significant increase in center frequency tuning range.
- Analog or Digital output signals (versus digital-only)
- Multiple input interfaces: USB2.0, TCP-IP (COM-1203), synchronous serial, synchronous parallel (versus synchronous only)
- ComScope monitoring of key internal modulator signals.

ComBlock Ordering Information

COM-1202
PSK / QAM / APSK modem with USB2.0 interface

COM-1203
PSK / QAM / APSK modem with USB2.0 / TCP-IP interface

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