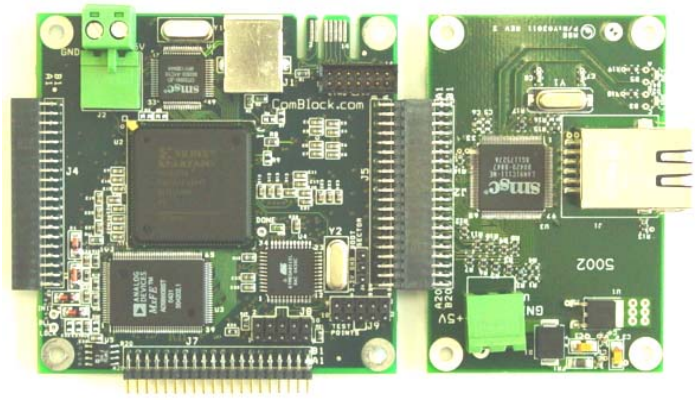
COM-1229/1230 DUAL DEMODULATORS (n-FSK / n-PSK / QAM / APSK) with USB 2.0 / TCP-IP

Key Features

- Dual demodulators
  - Concurrent demodulation
  - Independently programmable data rate and center frequency.
- Demodulator 1: continuous phase FSK (CPFSK) and its derivatives (MSK, GFSK, GMSK, 2-,4-,8-ary FSK).
  - Programmable 2-, 4-, 8-ary FSK
  - Programmable modulation index h [0.125 to 4]
  - Variable data rates up to 10 Msymbols/s = 30/20/10 Mbps. (8-, 4-, 2-ary FSK).
  - Designed for continuous mode applications. Fast re-acquisition after short link interruption.
- Demodulator 2: BPSK, QPSK, OQPSK, 8PSK, 16QAM, 16APSK, 32APSK
  - Variable data rates up to 20 Msymbols/s
- Demodulator complex (I&Q) input can be either
  - digital (2 * 10-bit complex, up to 80 Msamples/s)
  - analog (64 Msamples/s).
- Demodulated data can be routed to
  - two synchronous serial interfaces
  - USB 1.1/2.0.
  - TCP-IP/LAN (**COM-1230**).
- Extensive monitoring:
  - Demodulator lock
  - Frequency error
  - AGC gain
  - SNR measurement.
  - BER measurement when transmitting PRBS-11 test sequence.
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom). Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1229.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .



COM-1230 (includes TCP-IP)

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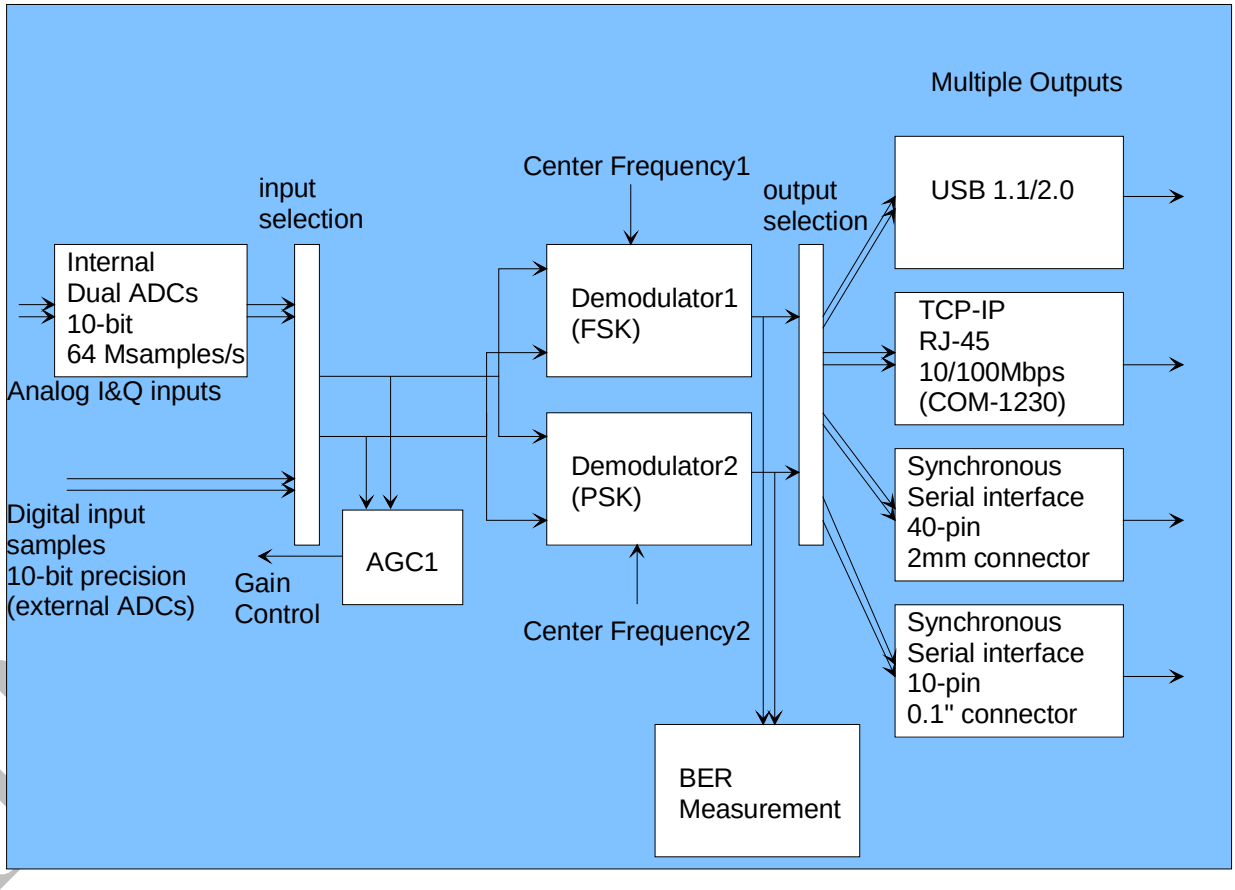
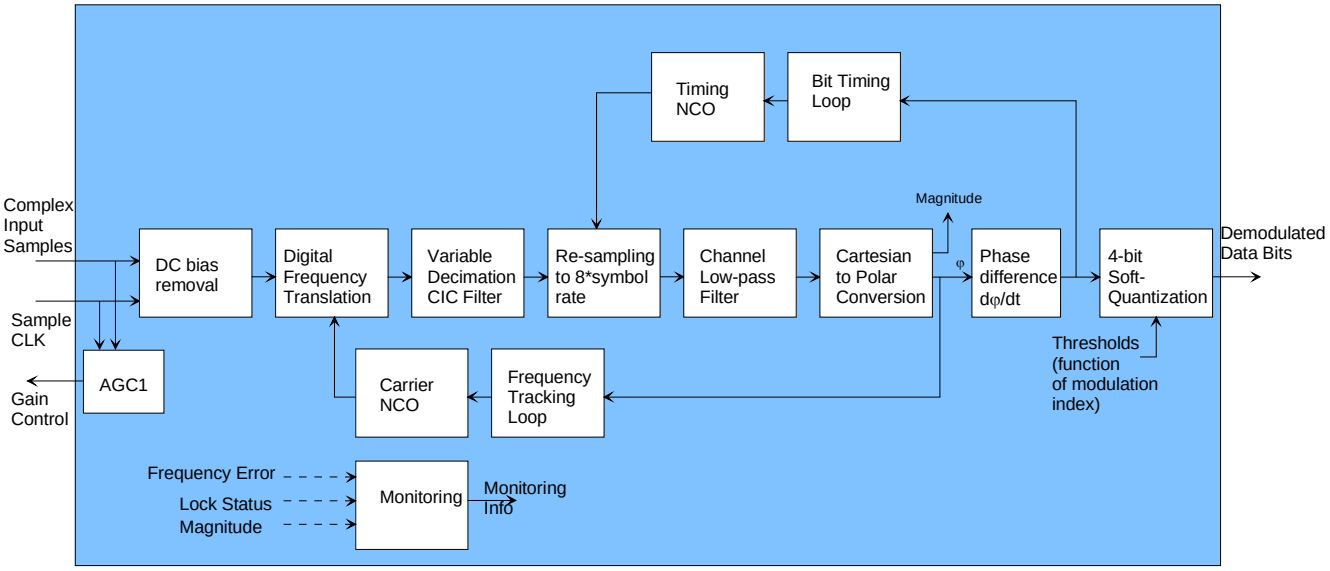
 Issued 2/5/2006

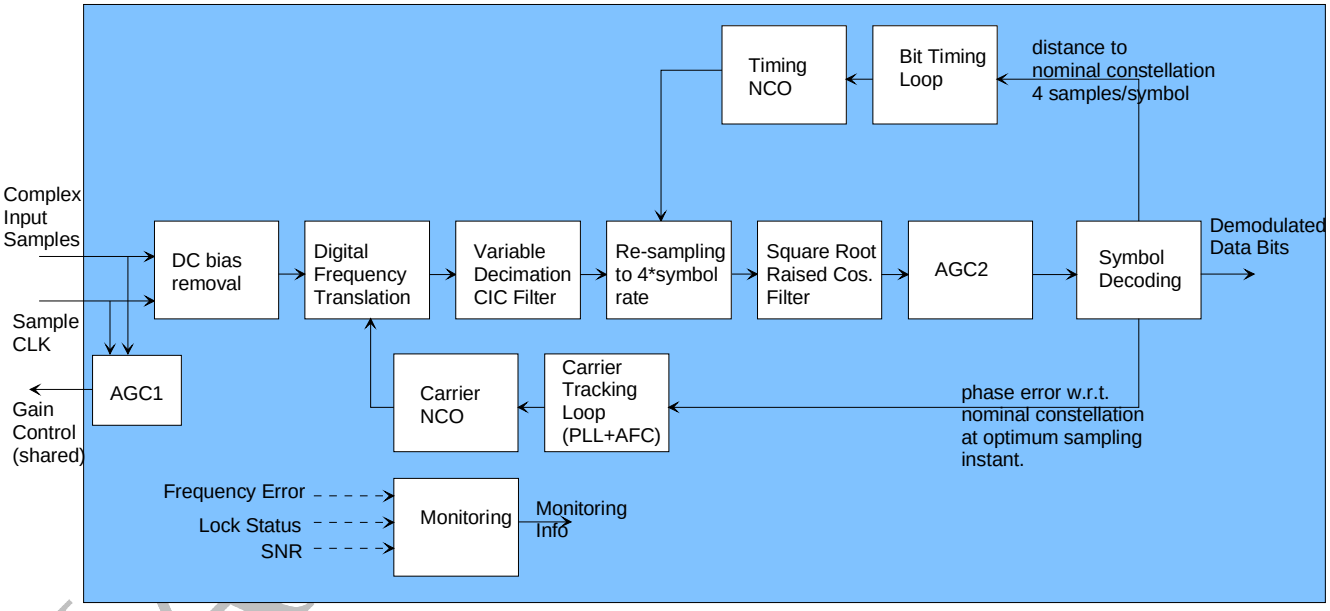
Overall Block Diagram



Block Diagram (FSK Digital Demodulator1)



Block Diagram (n-PSK / QAM / APSK Digital Demodulator2)



Electrical Interface

Digital Input Interfaces (J4)	**Definition**
DATA_I_IN[9:0]	Modulated input signal, real axis. 10-bit precision. Synchronous with rising edge of CLK_IN. Format: 2's complement or unsigned. Unused LSBs are pulled low.
DATA_Q_IN[9:0]	Modulated input signal, imaginary axis. 10-bit precision. Same format as DATA_I_IN.
SAMPLE_CLK_IN	Input signal sampling clock $\mathbf{f_s}$. One CLK_IN-wide pulse. Read the input signal at the rising edge of CLK_IN when SAMPLE_CLK_IN = '1'. The minimum input sampling rate is 8 samples per symbol for FSK modulation and 4 samples/symbol for PSK, QAM and APSK modulations. Samples can be consecutive. For example, SAMPLE_CLK_IN can be fixed at '1' to indicate that new input samples are provided once per CLK_IN clock period. Signal is pulled-up.
CLK_IN	Input reference clock for synchronous I/O. DATA_x_IN and SAMPLE_CLK_IN are read at the rising edge of CLK_IN. Maximum 80 MHz.

Analog Input Interfaces (J7)	**Definition**
RX_I_P / RX_I_N	I-channel differential inputs. (_P for +, _N for -). 200 Ohm input impedance. 2Vpp differential (1Vpp on each RX_I_P and RX_I_N signal) for full scale 10-bit ADC conversion. Common-mode voltage is approximately 2.3V. It is recommended that the input be AC coupled.
RX_Q_P / RX_Q_N	Q-channel differential inputs. (_P for +, _N for -). Same electrical characteristics as above.
RX_AGC1	Output. When this demodulator is connected directly to an analog receiver, it generates an analog 0 – 3.3V signal to control the analog gain prior to A/D conversion. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3.3V is the minimum gain. Pin J7/A6.

Output Interfaces	**Definition**
USB 2.0	Type B receptacle. This interface supports two virtual channels: one for monitoring and control, the other to convey a high-speed demodulated data stream from demodulator demod1 OR demod2 back to a host

	computer. Use USB 2.0 approved cable for connection to a host computer. Maximum recommended cable length is 3'.
LAN (COM-1230)	4 wire. 10Base-T/100Base-TX. RJ45 connector. NIC wiring. Use standard category 5 cable for connection to a Hub/Switch. Use crossover cable for connection to a host computer. This interface supports three virtual channels: one for monitoring and control, the two other to convey demodulated data from the two demodulators back to a host computer.
DATA_OUT[3:0]	Synchronous serial output. Read at the rising edge of CLK_OUT when BIT_CLK_OUT = '1'. 4-bit soft-quantized demodulated bits for use by subsequent error correction decoders. Unsigned representation: 0000 for maximum amplitude '0', 1111 for maximum amplitude '1'. The information bit is the most significant bit DATA_OUT(3).
BIT_CLK_OUT	Demodulated bit clock. One CLK-wide pulse. Read the output signal at the rising edge of CLK_OUT when BIT_CLK_OUT = '1'.
RX_LOCK	'1' when the demodulator is locked, '0' otherwise.
CLK_OUT	Output reference clock. Typically 40 MHz.

Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the symbol clock rate (f_{symbol_clk}). The maximum power consumption is 650mA.

Important: Digital I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration

Complete ComBlock assemblies can be monitored and controlled centrally over a single USB (default), TCP-IP/LAN (COM-1230), Serial or PC Card connection (via adjacent ComBlocks).

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

This module operates at a fixed internal clock rate $\mathbf{f_{clk}}$ of 80 MHz.

n-FSK Demodulator1	
Parameters	**Configuration**
Variable Decimation	Set the CIC Filter characteristics: CIC_N number of stages, 1 to 8 CIC_M differential delay 1 to 2 CIC_R decimation 1 to 16384 Number of truncated output bits: 0 to 63 Set R = 1 to bypass this stage. REG0 bits 3-0: CIC_N REG0 bits 5-4: CIC_M REG1: CIC_R LSB REG2: CIC_R MSB REG3 bits 5 - 0: number of truncated output bits
Nominal Symbol rate (f_{symbol_clk})	32-bit unsigned integer expressed as fsymbol rate * 2^{32} / $\mathbf{f_{clk}}$. The maximum symbol rate is $\mathbf{f_{clk}}$/8 (0x1FFFFFFF). The data rate is 1x, 2x or 3x the symbol rate depending on the M-ary number set in REG15. REG5 = bit 7-0 (LSB) REG6 = bit 15 – 8 REG7 = bit 23 – 16 REG8 = bit 31 – 23 (MSB)
Nominal Center frequency ($\mathbf{f_c}$)	This frequency value is subtracted from the received signal actual center frequency. 32-bit signed integer (2's complement representation) expressed as $\mathbf{f_c}$ * 2^{32} / $\mathbf{f_{clk}}$. Maximum theoretical range: ± $\mathbf{f_{clk}}$ /2. REG9 = bit 7-0 (LSB) REG10 = bit 15 – 8 REG11 = bit 23 – 16 REG12 = bit 31 – 23 (MSB)
Inverse Modulation Index **1/h**	1/(Modulation index **h**). Format 8.8 Thus, 0x0200 represents the inverse of a modulation index of 0.5. (MSK or GMSK modulation imply h = 0.5). Valid range for **1/h**: 0.125 – 4 REG13: bits 7:0 LSB REG14: bit 15:8: MSB
M-ary number	Size of the symbol alphabet: 00 = 2-ary, 2-FSK, M=2 01 = 4-ary, 4-FSK, M=4 10 = 8-ary, 8-FSK, M=8 REG15 bits 1-0
Channel filter selection	Selects the channel filter: 00 = no filter 01 = raised cosine filter 25% rolloff. REG15 bits 3-2
Spectrum inversion	Invert Q bit. Flips the baseband modulation spectrum. Does not affect any frequency error. 0 = off

	1 = on REG15 bit 4
AFC enable	An automatic frequency control circuit can be enabled to acquire and track the received signal center frequency in applications where the frequency error is prohibitive. 00 = automatic AFC selection based on the lock status. 01 = force AFC disabled. No carrier acquisition and tracking. 10 = force AFC enabled. REG15 bits 6-5
Force (Re-) acquisition	A one-time write of '1' forces the loops back into acquisition mode. This can be used to get out of any potential false lock condition. There is no need to clear this bit. REG15 bit 7
n-PSK/QAM/APSK Demodulator2	
Parameters	**Configuration**
Variable Decimation	Set the CIC Filter characteristics: CIC_N number of stages, 1 to 8 CIC_M differential delay 1 to 2 CIC_R decimation 1 to 16384 Number of truncated output bits: 0 to 63 Set R = 1 to bypass this stage. REG18: bits 3-0: CIC_N REG18: bits 5-4: CIC_M REG19: CIC_R LSB REG20: CIC_R MSB REG21 bits 5 - 0: number of truncated output bits
Nominal Symbol rate (f_{symbol_clk})	32-bit unsigned integer expressed as fsymbol rate * 2^{32} / $\mathbf{f_{clk}}$. The maximum symbol rate is $\mathbf{f_{clk}}$/4 (0x3FFFFFFF). The data rate is between 1x and 6x the symbol rate depending on the modulation type. REG23 = bit 7-0 (LSB) REG24 = bit 15 – 8 REG25 = bit 23 – 16 REG26 = bit 31 – 23 (MSB)
Nominal Center frequency ($\mathbf{f_c}$)	This frequency value is subtracted from the received signal actual center frequency. 32-bit signed integer (2's complement representation) expressed as $\mathbf{f_c}$ * 2^{32} / $\mathbf{f_{clk}}$. Maximum theoretical range: ± $\mathbf{f_{clk}}$ /2. REG27 = bit 7-0 (LSB) REG28 = bit 15 – 8 REG29 = bit 23 – 16 REG30 = bit 31 – 23 (MSB)
Modulation type	0 = BPSK 1 = QPSK 2 = OQPSK 3-7 = reserved for future QPSK constellations 8 = 8PSK constellation 8A 9 = 8PSK constellation 8B 10 = 8PSK constellation 8C 11 = 8PSK constellation 8D 12-15 = reserved for future 8PSK constellations 16 = 16QAM 17-23 reserved for future 16QAM constellations. 24 = 16APSK 25-31 reserved for future 16APSK 32 = 32APSK 33-39 reserved for future 32APSK REG31 bits 5-0
Spectrum inversion	Invert Q bit. 0 = off 1 = on REG31 bit 6
Channel filter bypass	0 = enable the root raised cosine filter (general case) 1 = bypass the root raised cosine filter (special use in applications when a root raised cosine filter is not used in the modulator.) REG31 bit 7
Carrier frequency tracking loop gain	00 = nominal 01 = 2x loop gain 10 = 4x loop gain 11 = 8x loop gain The loop gain can be changed dynamically to ease the transition between acquisition and tracking. A higher loop gain can be used to increase acquisition range or to minimize cycle slips at low data rate. A lower loop gain minimizes demodulation losses. REG32 bits 1-0
AFC enable	The automatic frequency control circuit extendeds the frequency acquisition over +/- 10% of the symbol rate. When disabled, the receiver only means of carrier acquisition is the carrier frequency tracking loop which is inherently limited to approximately 1% of the symbol rate. The AFC should only be used during acquisition as it interferes with the Costas Loop operation. 00 = automatic AFC selection. 01 = force AFC disabled. Carrier tracking loop only 10 = force AFC enabled. 11 = reserved (test). REG32 bits 3-2
Lock status	Demodulator lock status is based on the

threshold	standard deviation of the phase error. When std(phase error) is below this user-defined threshold, the receiver is deemed to be locked onto the received signal. 000 = 1 deg 001 = 2 deg 010 = 5 deg 011 = 10 deg 100 = 15 deg 101 = 20 deg 110 = 25 deg (recommended settings when automatic AFC selection) REG32 bits 6-4
Force (Re-) acquisition	A one-time write of '1' forces the carrier loops (carrier PLL, AFC) back into acquisition mode. This can be used to get out of any potential false lock condition. There is no need to clear this bit. REG32 bit 7
Inputs	
Parameters	**Configuration**
Input selection	00 = 2 * 10-bit unsigned samples, left J4 connector 01 = 2 * 10-bit signed 2's complement samples, left J4 connector 10 = baseband analog interface, bottom J7 connector. REG35 bits 1-0
Rx ADC gain	Analog signals prior to the built-in A/D converter can be amplified by steps of about 1 dB. This 5-bit unsigned integer controls the variable gain between 0 and 20 dB. Applies equally to the I and Q channels. When the COM-1229/1230 is used in conjunction with the COM-3501 UHF transceiver, a settings of 10 (x0A) is recommended. REG35 = bits 6-2
AGC1 response time	The front-end AGC1 response time is user controlled. The RX_AGC1 analog gain control signal is updated as follows 0 = every symbol, 1 = every 2 symbols, 2 = every 4 symbols, 3 = every 8 symbols, etc…. 20 = every 1 million symbols. Valid range 0 to 20. REG36 bits 4-0
DC bias removal	Enable or disable the DC bias removal circuit at the input. May be helpful in cases where the external analog-to-digital converters introduce unwanted DC bias. Bias is averaged over approximately 1024 symbols. If the modulated data is not random over this averaging period, or if the modulation index is very small, it is recommended to disable the DC bias removal. 0 = disabled/bypassed 1 = enabled REG36 bit 5
Output	
Parameters	**Configuration**
Output selection	000 = USB (demodulator 1 only) 001 = TCP-IP (**COM-1230**) 010 = synchronous serial J5 right connector (**COM-1229**) 011 = synchronous serial J5 right connector (**COM-1229**) with swapped demodulated streams (1->B, 2->A). 100 = synchronous serial J9 connector used as demod1 output instead of test points. 101 = synchronous serial J9 connector used as demod2 output instead of test points. 110 = USB (demodulator 2 only) REG37 bits 2-0
Output format	Users may have to tradeoff throughput versus soft-quantization when using the USB 2.0 or TCP-IP connection as media to route demodulated data to a host computer. Demodulated data can be transmitted as 1-bit 'hard-quantized' or 4-bit 'soft-quantized' samples. Due to throughput limitation on these media, the maximum demodulated data rate may only be available as 1-bit 'hard-quantized' samples. No such limitation exists when using the synchronous serial output format. 0 = 1-bit hard quantized samples 1 = 4-bit soft quantized samples REG37 bit 3
BER measurement data stream selection	Selects which demodulator output data stream is to be subjected to BER measurement. 0 = demodulator 1 (FSK) 1 = demodulator 2 (PSK/QAM/APSK) REG37 bit 4
IP address (**COM-1230**)	4-byte IP address. Example : 0x AC 10 01 80 designates address 172.16.1.128 The new address becomes effective immediately (no need to reset the ComBlock). REG38: MSB REG39 REG40 REG41: LSB
10Base-T / 100Base-TX LAN selection (**COM-1230**)	00 = 10Base-T 01 = 100Base-TX 10 = Auto negotiation Changes will take effect at the next power up. REG42 bits 1-0

Half / Full duplex LAN link (COM-1230)	0 = half duplex 1 = full duplex Changes will take effect at the next power up. REG42 bit 2
Reserved	REG43 through 48 are reserved for the LAN MAC address. These registers are set at the time of manufacturing. REG4, REG22 reserved for future use. Set as 0.

Baseline configurations can be found at www.comblock.com/tsbasic_settings.htm and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

Monitoring

Digital status registers are read-only.

n-FSK Demodulator1 Monitoring	
Parameters	**Monitoring**
Carrier frequency offset (fcdelta)	Residual frequency offset with respect to the nominal carrier frequency. 24-bit signed integer (2's complement) expressed as fcdelta * 2^{24} / (8*fsymbol rate). SREG0 = bit 7 – 0 SREG1 = bit 15 – 8 SREG2 = bit 23 – 16
Received signal magnitude after channel filtering	8-bit unsigned SREG3 bit 7-0.
AFC lock status	0 = unlocked 1 = locked SREG4 bit 0
Signal power detection	0 = below threshold 1 = signal power detection SREG4 bit 1
n-PSK/QAM/APSK Demodulator2 Monitoring	
Parameters	**Monitoring**
Carrier frequency offset (fcdelta)	Residual frequency offset with respect to the nominal carrier frequency. 24-bit signed integer (2's complement) expressed as fcdelta * 2^{24} / fsymbol rate. SREG10 = bit 7 – 0 SREG11 = bit 15 – 8 SREG12 = bit 23 – 16
Received signal magnitude after channel filtering	8-bit unsigned SREG13 bit 7-0.
Carrier tracking loop lock status	Lock is declared if the standard deviation of the phase error is less than the user-defined threshold. See Lock status threshold control. 0 = unlocked 1 = locked SREG14 bit 0
BER Measurement	
Parameters	**Monitoring**
Bit Errors	Number of bit errors in a fixed-length window. 32 bit unsigned. SREG20: error_count[7:0] SREG21: error_count[15:8] SREG22: error_count[23:16] SREG23: error_count[31:24] The bit errors counter is updated once every periodic measurement window. Reading the value will not reset the counter.
BER Synchronization status	0 = not synchronized. 2047-bit pattern is not detected. 1 = synchronized SREG24 bit 0.
n-PSK Phase ambiguity. Cycle slip detection.	Number indicating the phase offset between modulated and demodulated data streams. A change in phase offset denotes a cycle slip. The phase offset is expressed as 00 = 0 deg 01 = +90 deg 10 = +180 deg 11 = +270 deg SREG24 bits 2-1
TCP-IP Connection Monitoring	
Parameters	**Monitoring**
TCP-IP connection	Monitors the TCP-IP connection status on ports 1024 (demod1), 1026 (demod2) and 1028 (monitoring & control). 1 = connected, 0 otherwise. SREG30 bit 0 port 1024 (demod1) SREG30 bit 1 port 1026 (demod2) SREG30 bit 2 port 1028 (M&C)
Number of bytes received from demodulator and forwarded to host over TCP-IP/LAN	32-bit byte count. Counter rolls over when reaching 0xFFFFFFFF. SREG31: bits 7-0 (LSB) SREG32: bits 15-8 SREG33: bits 23-16 SREG34: bits 31-24 (MSB)
MAC address	Unique 48-bit hardware address (802.3). In the form SREG35:SREG36:SREG37:…:SREG40

ComScope Monitoring

Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-1229/1230 signal traces and trigger are defined as follows:

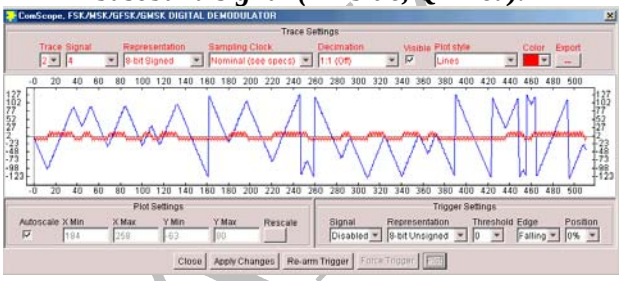
Trace 1 signals (Input & demod1)	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Composite input I signal	8-bit signed (8MSB/12)	f_{clk}	512
2: I signal after frequency translation to baseband	8-bit signed (8MSB/12)	Input sampling rate	512
3: Cartesian-to-Polar conversion: phase	8-bit signed (8MSB/10)	8 samples /symbol	512
4: Recovered phase, after scaling for modulation index (i.e. prior to soft quantization)	8-bit signed (8MSB/14)	1 samples /symbol (optimum sampling instant)	512
5: Recovered carrier frequency offset. Resolution is fsymbol/32.	8-bit signed (8MSB/24)	8 samples /symbol	512
Trace 2 signals (Input & demod1)	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: Composite input Q signal	8-bit signed (8MSB/12)	f_{clk}	512
2: front-end AGC RX_AGC1	8-bit unsigned (8MSB/10)	Decimated symbol rate. See control REG32.	512
3: I signal after variable decimation and resampling at 8 samples/symbol	8-bit signed (8MSB/12)	8 samples /symbol	512
4: Cartesian-to-Polar conversion: magnitude	8-bit signed (8MSB/14)	8 samples /symbol	512
5: Phase difference	8-bit signed (8MSB/10)	8 samples /symbol	512
Trace 3 signals (demod2)	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: I signal after frequency translation to baseband	8-bit signed (8MSB/12)	Input sampling rate	512
2: I signal after root raised cosine filtering	8-bit signed (8MSB/12)	4 samples /symbol	512
3: Demodulated I signal at optimum sampling instant	8-bit signed	1 sample /symbol	512
4: 2nd AGC average control gain	8-bit unsigned (8MSB/14)	4 sample /symbol	512
Trace 4 signals (demod2)	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: I signal after variable decimation and resampling	8-bit signed (8MSB/12)	4 samples /symbol	512
2: phase error variance (units: $(deg/360*2048)^2$ /256	8-bit unsigned	1 sample /symbol	512
3: Demodulated I signal after phase correction and normalization	8-bit signed	4 samples /symbol	512
4: Symbol timing recovered phase	8-bit signed (8MSB/32)	1 sample /symbol	512
Trigger Signal	**Format**		
1: Demod1 AFC lock status	Binary		
2: Demod1 Signal power detection	Binary		
3: BER measurement: detected start of PRBS-11 sequence	Binary		

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk} processing clock as real-time sampling clock.

In particular, selecting the f_{clk} processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.

ComScope Window Sample: showing GMSK input baseband signal (I = blue, Q = red).



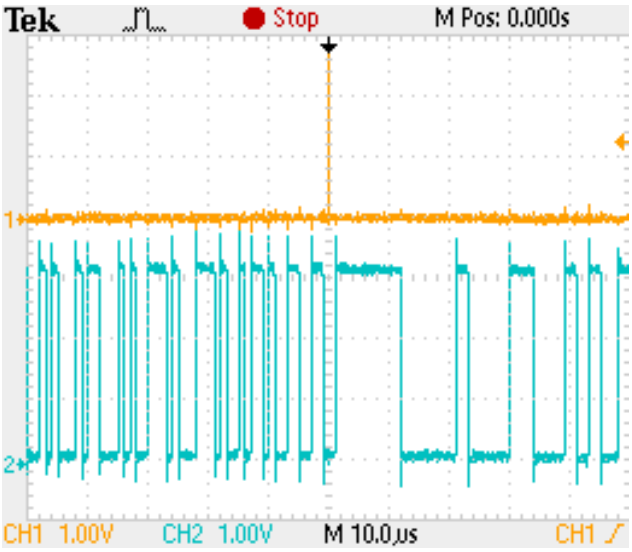
ComScope Window Sample: showing GMSK demodulated phase (blue) and reconstructed unfiltered symbols (red).

Digital Test Points

Test points TP1 through TP10 are generally routed to the J9 10-pin 0.1” connector.

Note: Test points are disabled when the user selects the J9 connector to route output data streams to external devices using a ribbon connector. See control register REG37(2:0).

Digital Test Point	Definition
TP1	Demod 1: AFC lock status (1 = locked, 0 = unlocked)
TP2	Demod 1: Recovered carrier (carrier NCO output MSB). Includes the fixed offset defined by the user as Nominal Center Frequency.
TP3	Demod 1: Recovered bit timing Compare with modulator bit timing.
TP4	Demod 2: lock status
TP5	Demod 2: Recovered carrier (carrier NCO output MSB). Includes the fixed offset defined by the user as Nominal Center Frequency.
TP6	Demod 2: Recovered symbol clock. Compare with modulator symbol clock.
TP7	BER measurement: Synchronization
TP8	BER measurement: Bit error
TP9	BER measurement: Start of PRBS-11 periodic test sequence detected with less than 10% bit errors.
TP10	BER measurement: demodulated bit stream.
DONE	‘1’ indicates proper FPGA configuration.
INITB	Reference clock $\mathbf{f_{clk}}$ / 8 = 10 MHz.



Test points TP9 (orange) and TP10 (teal) are helpful in visualizing the demodulated data stream. The screen capture above shows the characteristic waveform of a PRBS-11 test sequence demodulated at 1 Mbit/s. Trigger the oscilloscope on the start of the PRBS-11 sequence TP9.

Analog Test Points

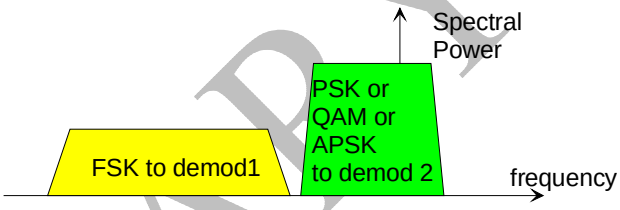
Key internal signals can also be monitored continuously by routing them to the bottom 40-pin connector and using the built-in high-speed D/A conversion module. Monitoring is non-obstrusive: it can be run concurrently with normal demodulation.

Analog Test Point	Definition
TPA1_P/TPA1_N	Demod2 demodulated I signal after phase correction and normalization Differential output signal
TPA2_P/TPA2_N	Demod2 demodulated Q signal after phase correction and normalization Differential output signal
TPA3	Demod2 Symbol clock. Approximately 50% duty cycle. Rising edge is located near the optimum sampling instant.
TPA4	Demod1 residual amplitude modulation (AM) of the received signal after the channel filter. This is the residual amplitude modulation not removed by the slow-moving AGC1. Single-ended output signal.
TPA5	Undefined.

Operation

FDMA

The COM-1229/1230 is capable of demodulating two frequency-division multiplexed signals simultaneously. An essential requirement is that the two modulated signals are sufficiently separated in frequency to mimize interferences. The center frequencies and bandwidths are independently programmable for both signals. Input center frequencies can be positive, zero, or negative.



Input Signal Pre-Processing

Prior to being routed to the FSK or n-PSK demodulator, the input signal is subject to AGC1, variable decimation, and frequency translation to near-zero frequency.

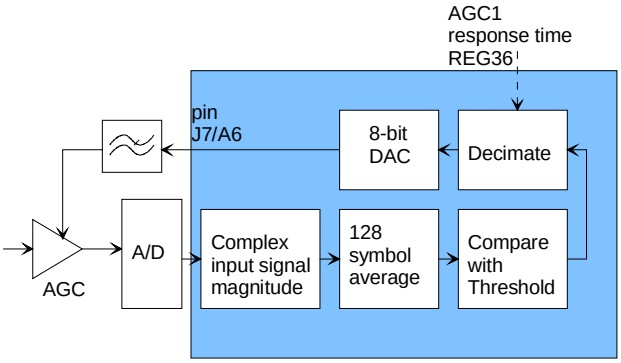
AGC1

The purpose of this AGC is to prevent saturation at the input signal A/D converters while making full use of the A/D converters dynamic range. Therefore, AGC1 reacts to the composite input signal which may comprise two FDMA signals, interferers and noise. The principle of operations is outlined below:

(a) The magnitude of the complex input samples is computed and continuously averaged over 128 symbols.

(b) The average magnitude is compared with a target magnitude threshold and the AGC gain is adjusted accordingly. Users can control the rate at which the gain control value is updated (to prevent instabilities, depending on the gain control slope and linearity at the RF front-end). See control register REG36.

(c) An 8-bit D/A converter generates the analog gain control signal RX_AGC1 for use by the external variable gain amplifiers.



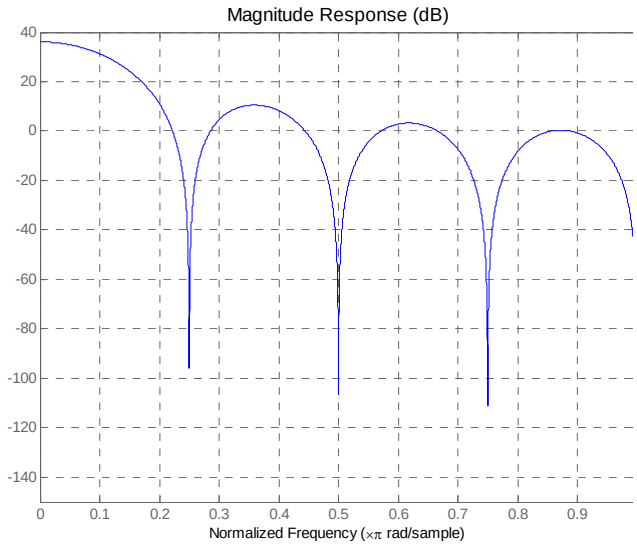
AGC1 principle

Variable Decimation

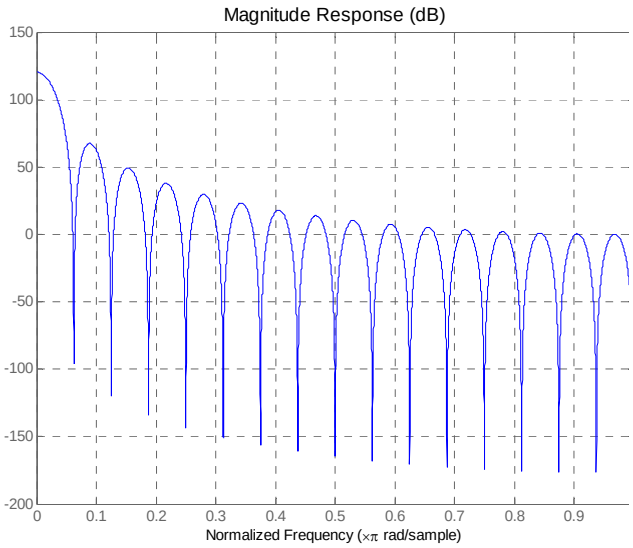
The user can reduce the rate of sampling of the input signal before it reaches the digital demodulator. The decimation rate R is user programmable. A Cascaded Integrated Comb (CIC) filter is used prior to decimation to prevent aliasing.

The implementation lets the user specify the number of stages N (in the range from 1 to 8), the differential delay M (in the range from 1 to 2), the decimation rate R (in the range from 8 to 16384) and the number of least significant bits to be truncated at the output (in the range from 0 to 63). It is generally recommended to set the latter to N*log2(RM), which is the bit growth during the CIC calculation due to the gain G = $(RM)^N$.

Examples of CIC filter responses are shown below:
X-axis is [0,input sampling frequency/2]
Y-axis is the magnitude response in dB.



N = 2, M = 1, R = 8



N = 4, M = 1, R = 32

Matlab functions:
hm = mfilt.cicdecim(r,m,n,ibits,obits,bps);
fvtool(hm);

The first zero is located at
(input sampling frequency) / (R * M).

Generally, the best tradeoff between maximizing aliasing rejection and minimizing in-band signal distortion is to select R and M such that
*R * M = (input sampling rate) / (4*symbol rate).*
For example, for a 1 Msymbols/s modulation, select R = 20, M = 1.

In order to prevent saturation, *the number of truncated bits must be selected to be the smallest integer greater than log2(RM)^N* . For example, if R = 20, M = 1, N = 2, truncate 10 output bits.

Bit Error Rate Measurement

A built-in BER measurement circuit counts the number of demodulated bit errors in a 1,000,000 bit window when the transmitted data stream is a 2047-bit pseudo-random sequence (PRBS-11). Most ComBlock modulators can be configured to generate this test sequence.

The BER measurement circuit synchronizes itself with the demodulated stream. It also detects bit stream inversion and BPSK/QPSK phase ambiguities. The latter is useful in determining whether cycle slips occur in the demodulator.

The synchronization status, last completed error count, and inversion/phase-ambiguity is reported in the status window.

This single BER measurement component is shared between the two demodulators.

Demodulator 1

FSK Modulation

The FSK modulation and its derivatives (CPFSK, MSK, GMSK, GFSK) are best described by the following equations for the modulated signal s(t). The first equation describes a phase modulator, with the modulated centered around the center frequency f_c.

$$s(t) = \sqrt{\frac{2E_s}{T}}.\cos(2\pi f_c t + \theta(t) + \theta_0)$$

where
- E_s is the energy per symbol
- T is the symbol period
- f_c is the center frequency
- $\theta(t)$ is the phase modulation

The COM-1229/1230 implements a continuous phase FSK demodulator. It assumes that there are no phase discontinuities between symbols. The CPFSK phase modulation can be described as:

$$\theta(t) = \frac{\pi h}{T}\int_0^t a_i(t)dt$$

where:
- h is the modulation index. A modulation index of 0.5 yields a maximum phase change of π/2 over a symbol.

a_i are the symbols. With 2-FSK, the binary data is represented as –1 (for '0') and +1 (for '1').

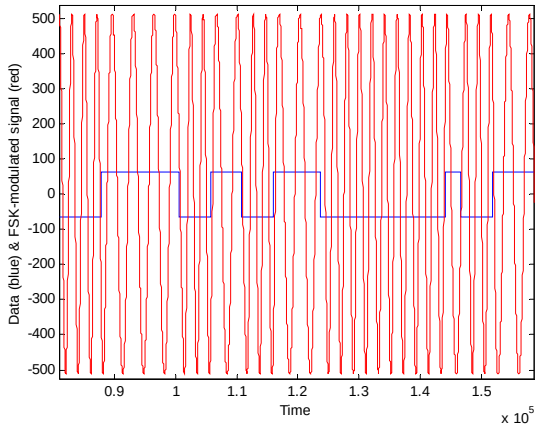
M-ary Number M

The transmitted data is grouped into symbols of size 1, 2, or 3 consecutive bits. The size of the symbol alphabet is thus M = 2, 4 or 8. The symbol MSB is sent first to the DATA_OUT output.

The mapping between modulation symbol a_i and symbol alphabet is described in the table below:

Modulation symbol a_i	Symbol alphabet
-1	2-FSK '0'
+1	2-FSK '1'

-3	4-FSK “00”
-1	4-FSK “01”
+1	4-FSK “10”
+3	4-FSK “11”
-7	8-FSK “000”
-5	8-FSK “001”
-3	8-FSK “010”
-1	8-FSK “011”
+1	8-FSK “100”
+3	8-FSK “101”
+5	8-FSK “110”
+7	8-FSK “111”



Continuous FSK modulated signal example

FSK modulation is sometimes characterized by the frequency separation between symbols. The relationship between modulation index h and frequency separation is $f_{separation} = 0.5\ h\ f_{symbol\_clk}$

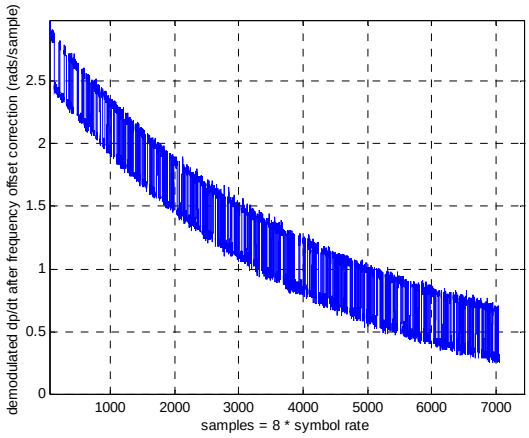
Frequency Acquisition and Tracking

The demodulator comprises an automatic frequency control (AFC) loop to acquire and track the residual frequency offset of the modulated signal.

The tracking range $f_{tracking}$ is bound by the following constraints:
$abs(\mathbf{f_{tracking}}/(4* \mathbf{f_{symbol\_clk}})) + \mathbf{h}/8 < 1$

For example, if the modulation index **h** is 0.5, the maximum tracking range is ± 3.75 $\mathbf{f_{symbol\_clk}}$. We recommend an additional 10% implementation margin.

The AFC response time is illustrated below for an initial frequency offset of (3.37* $\mathbf{f_{symbol\_clk}}$) and modulation index h = 0.5.



AFC response to input frequency step

An AFC lock status is provided in status register SREG4 and at a test point. AFC lock is declared when the residual frequency error is below 1/16th of the symbol rate.

Bit Timing Tracking

A first order loop is capable of acquiring and tracking bit timing differences between the transmitter and the receiver, up to ± 500 ppm.

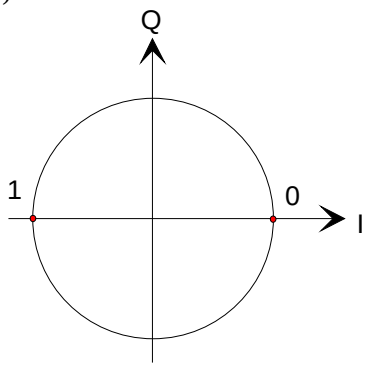
Demodulator 2

Demodulator 2 is designed to demodulate several PSK, QAM and APSK modulations. The symbol mapping for each modulation is shown below:

Symbol Mapping

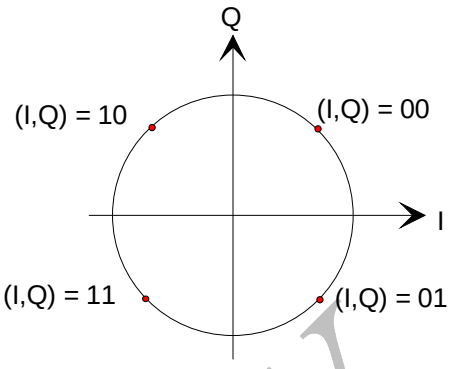
BPSK

REG31(5:0) = 0



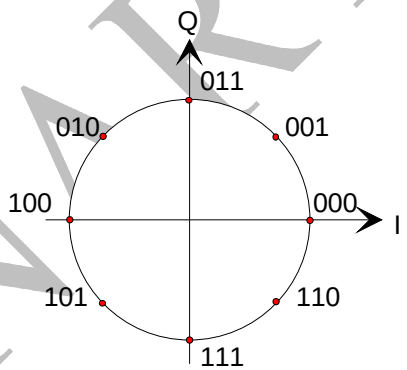
QPSK

REG31(5:0) = 1



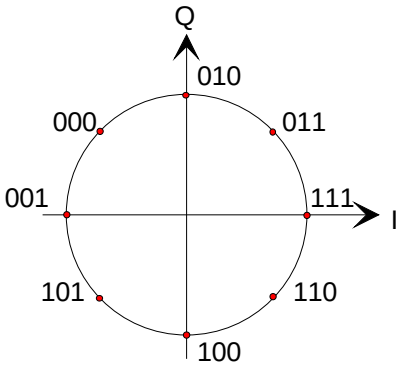
8PSK (1)

REG31(5:0) = 8



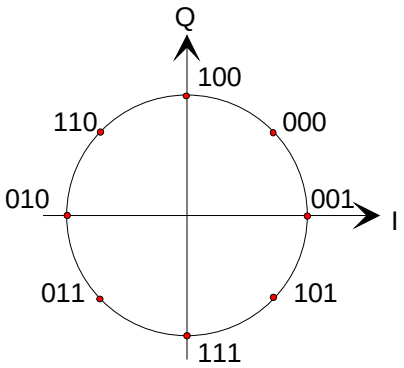
8PSK (2)

REG31(5:0) = 9



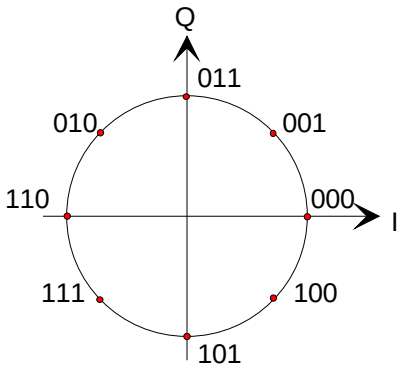
8PSK (3)

REG31(5:0) = 10



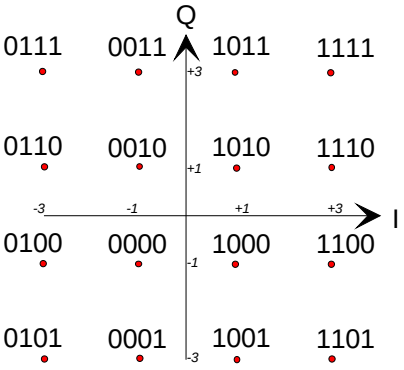
8PSK (4)

REG31(5:0) = 11



16QAM

REG31(5:0) = 16



Filter Response

For all demodulator 2 modulations, the channel filter is a root raised cosine filter, which is applied to both In-phase and Quadrature signals at baseband. In order to minimize intersymbol interferences, one expects the same filter to be used at the modulator. To this effect, users can select one of several rolloff factors: 20%, 25%, 35% and 40%.

Changing the rolloff selection requires loading the firmware once using the ComBlock control center, then switching between up to four stored firmware versions (it takes 2.2 seconds).

The four firmware versions can be downloaded from www.comblock.com/download.

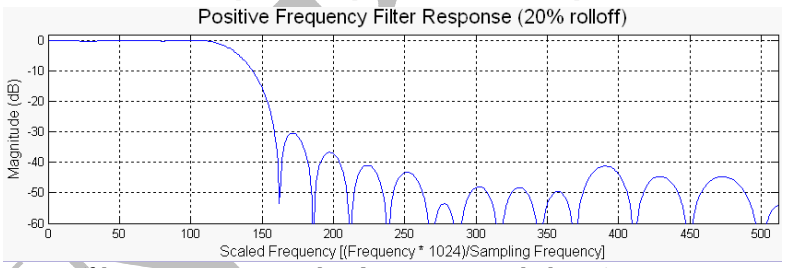
COM-1229-**A** 20% rolloff

COM-1229-**B** 25% rolloff

COM-1229-**D** 35% rolloff

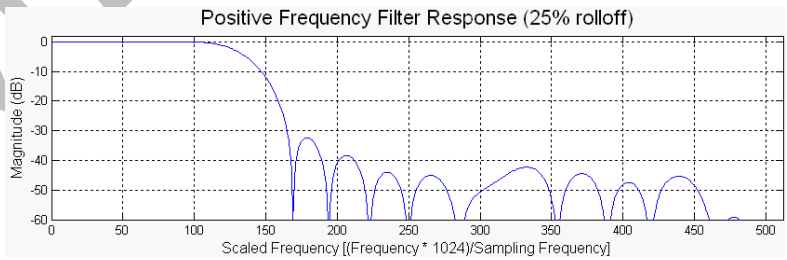
COM-1229-**E** 40% rolloff

Filter Response (-A 20% rolloff)



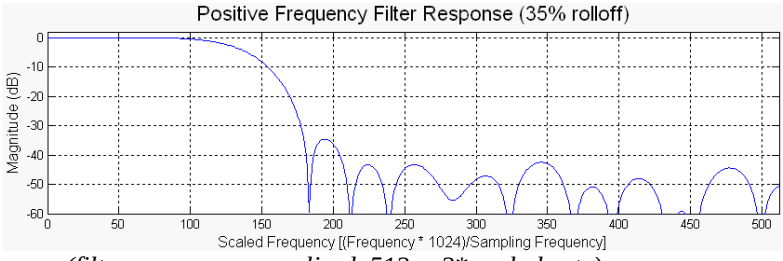
*(filter response normalized. 512 = 2*symbol rate)*

Filter Response (-B 25% rolloff)



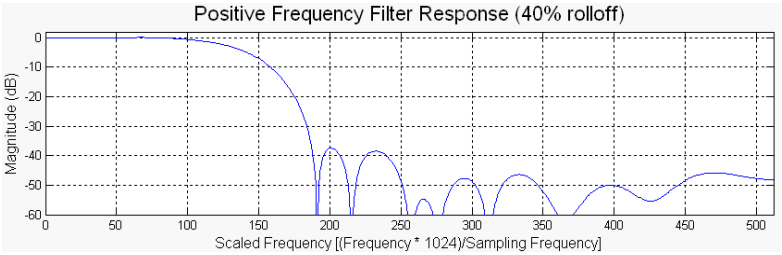
*(filter response normalized. 512 = 2*symbol rate)*

Filter Response (-D 35% rolloff)



*(filter response normalized. 512 = 2*symbol rate)*

Filter Response (-E 40% rolloff)



*(filter response normalized. 512 = 2*symbol rate)*

LAN / TCP-IP (*COM-1230*)

Initial Configuration (via Serial Link)

The static IP address must first be configured over non-TCP-IP connections such as USB or through other ComBlocks. This network setting is saved in non-volatile memory (see control registers REG38-41). The TCP-IP connection can be used once the correct network setting is configured and after a COM-1230 power cycle.

IP Ports

The COM-1230 acts as a TCP-IP server. As such it opens the following sockets in listening mode:

- Port 1024: receive demodulator 1 data stream.
- Port 1026: receive demodulator 2 data stream.
- Port 1028: monitoring and control port.

In addition, the COM-1230 opens port 1029 as a UDP port for remote reset.

IP Protocols

This module supports the following IP protocols:

- Ping
- ARP
- TCP-IP

Ping

The module responds to ping requests with size up to 470 bytes. Ping can be used to check the module response over the network. Ping can be used at any time, concurrently with other transmit and receive transactions. For example, on a Windows operating system, open the Command prompt window and type “ping –t –l 470 172.16.1.128” to send pings forever of length 470 bytes to address 172.16.1.128.

Concept

The COM-1230 converts a serial data stream into a TCP-IP socket stream. TCP, IP and Network information, and in particular routing information, are not transmitted from one end to the other.

At the receiving end, the network client must first connect to the COM-1230 to receive data.

A key assumption is that the network client is reading as fast as the demodulator(s) can forward demodulated data. If not, data will be lost. The demodulated data is stored within a 16 Kbit elastic buffer within the COM-1230. This buffer size determines the maximum interruption for which the network client (operating system) can temporarily stop reading data. For example, for a 1 Mbit/s data stream, the maximum interruption allowed is 16.384 ms.

Throughput Benchmarks

The COM-1230 is capable of a sustained (average) throughput of 50 Mbits/s over 100base-Tx. In most cases, the sustained throughput is limited by the TCP-IP client computer and the application running on the client computer as illustrated in the one-way data transfer benchmark below:

Throughput tests conditions	**Throughput**
Client: Intel Pentium 4 2.6 GHz running winsock-based console application. Connection over LAN switch. No other network connection. No other application running. COM-1230 configured as 'Auto Negotiation". 100Base-Tx connection.	41 Mbits/s min 54.7 Mbits/s max 100 Mbytes received in 16.0 seconds.

Format Conversion

Serial to parallel conversion occurs when converting the demodulated data stream into 8-bit byte over the TCP-IP link. The key rule is that the first received bit is placed at the MSb position in the byte.

UDP-IP

Port 1029 is open as a UDP receive-only port. This port serves a single purpose: being able to reset all TCP-IP connections gracefully. This feature is intended to remedy a common practical problem: it is a common occurrence for one side of a TCP-IP connection to end abnormally without the other side knowing that the connection is broken (for example when a server 'crashes'). In this case, new connections cannot be established without first closing the previous ones. The problem is particularly acute when the COM-1230 is at a remote location.

The command "@001RST<CR><LF>" sent as a UDP packet to this port will reset all TCP-IP connections within the COM-1230.

Client Programming

This section is intended to help designers who want to design their own client application. It can be skipped by users of ready-to-use applications such as Hyperterminal, ComBlock Control Center, etc.

In network terminology, the COM-1230 is a server. It awaits connection establishment and connection termination under the initiation of clients. It never initiate any connection establishment or termination.

An example of C-language Winsock programming for Windows OS clients is shown below. More information about Winsock programming can be found at http://msdn.microsoft.com/library/default.asp?url=/library/en-us/winsock/winsock/finished_server_and_client_code.asp

Be sure to include a reference to the Winsock2 library (WS2_32.lib) in the project release and/or debug settings.

```
#include <stdio.h>
#include "winsock2.h"
void main() {

    // Initialize Winsock.
    WSADATA wsaData;
    int iResult = WSAStartup( MAKEWORD(2,2), &wsaData );
    if ( iResult != NO_ERROR )
        printf("Error at WSAStartup()\n");

    // Create a socket.
    SOCKET m_socket;
    m_socket = socket( AF_INET, SOCK_STREAM, IPPROTO_TCP );

    if ( m_socket == INVALID_SOCKET ) {
        printf( "Error at socket(): %ld\n", WSAGetLastError() );
        WSACleanup();
        return;
    }

    // Connect to a server.
    sockaddr_in clientService;

    clientService.sin_family = AF_INET;
// insert destination address below
    clientService.sin_addr.s_addr = inet_addr( "172.16.1.128" );
// insert destination port below
    clientService.sin_port = htons(1024);

    if ( connect( m_socket, (SOCKADDR*) &clientService, sizeof(clientService) ) ==
SOCKET_ERROR) {
        printf( "Failed to connect.\n" );
        WSACleanup();
        return;
    }

    // Send and receive data.
    int bytesSent;
    int bytesRecv = SOCKET_ERROR;
    char sendbuf[32] = "Client: Sending data.";
    char recvbuf[32] = "";

    bytesSent = send( m_socket, sendbuf, strlen(sendbuf), 0 );
    printf( "Bytes Sent: %ld\n", bytesSent );

    while( bytesRecv == SOCKET_ERROR ) {
        bytesRecv = recv( m_socket, recvbuf, 32, 0 );
        if ( bytesRecv == 0 || bytesRecv == WSAECONNRESET ) {
            printf( "Connection Closed.\n");
            break;
        }
        if (bytesRecv < 0)
            return;
        printf( "Bytes Recv: %ld\n", bytesRecv );
    }

    return;
}
```

USB Interface

USB Throughput Benchmarks

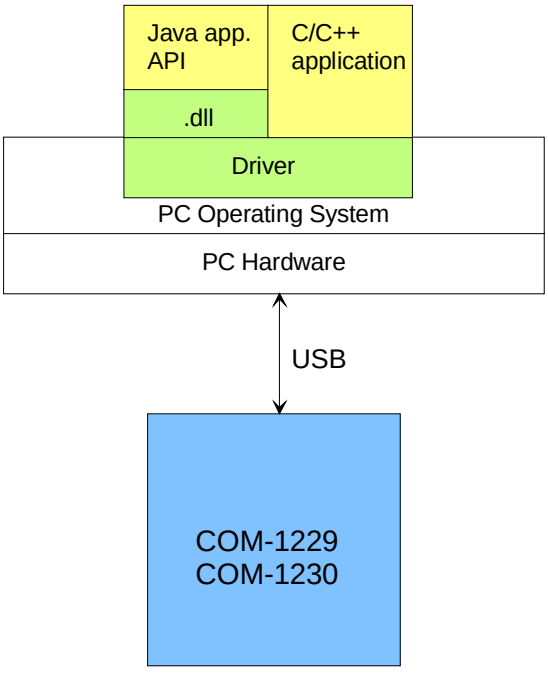
The COM-1229/1230 is capable of a sustained (average) throughput of 85 Mbits/s over USB 2.0. In most cases, the sustained throughput is limited by the host computer and the application(s) running on the host computer.

Client Programming : USB 2.0

Software to help developers create USB high-speed communications between the COM-1229/1230 and a host PC is provided. The **USB 2.0 software package** includes the following:

- Windows device driver for XP/2000/Me (.sys, .inf files)
- Java API, .dll and application sample code
- C/C++ application sample code

The **USB 2.0 software package** is available in the ComBlock CD and can also be downloaded from ComBlock.com/download/usb20.zip.
The user manual is available at ComBlock.com/download/USB20_UserManual.pdf

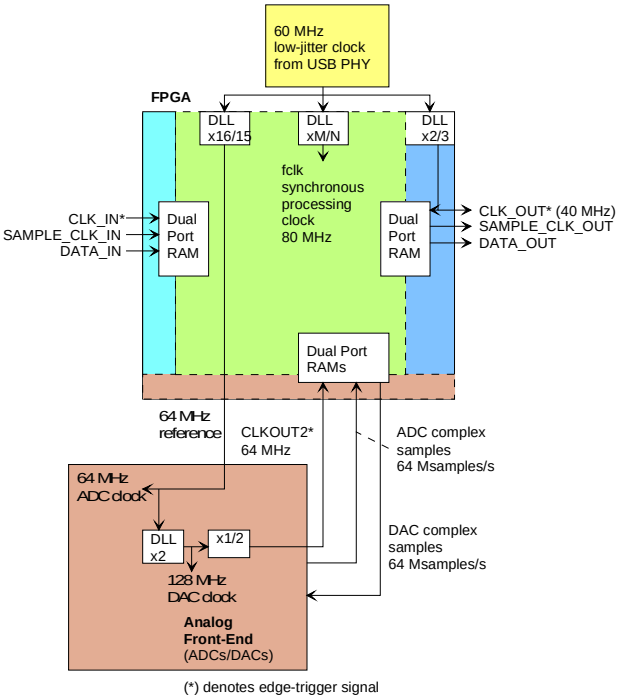


Blue: supplied hardware
Green: supplied ready-to-use software
Yellow: source code examples

Timing

Clocks

The clock distribution scheme embodied in the COM-1229/1230 is illustrated below.



Baseline clock architecture
Yellow = 60 MHz reference clock
Green = f_{clk} processing zone
Dark Blue = 40 MHz output clock
Light Blue = 40 MHz external input clock
Brown = 64 MHz I/O zone

The core signal processing performed within the FPGA is synchronous with the processing clock $\mathbf{f_{clk}}$. In order to minimize clock jitter, the processing clock is derived from a 60 MHz reference clock with low-jitter. $\mathbf{f_{clk}}$ is not related to the CLK_IN clock. $\mathbf{f_{clk}}$ is used for internal processing and for generating the output clock CLK_OUT.

The signals at the digital input connector J4 are synchronous with the CLK_IN signal at J4/A1. This clock can be 40 MHz.

The signals at the digital output connector J5 are synchronous with the 40 MHz CLK_OUT signal derived from the 60 MHz reference clock.

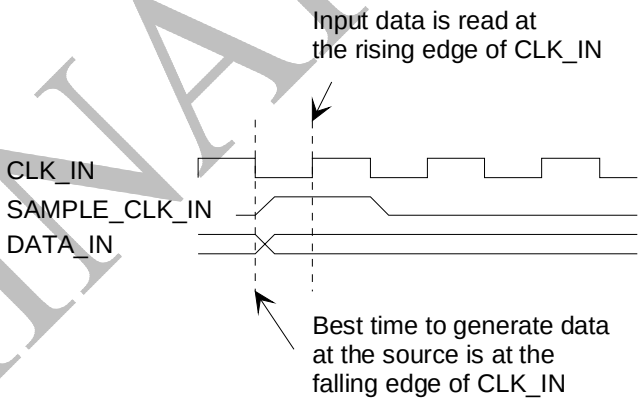
The signals at the analog front-end interface are synchronous with the 64 MHz reference clock generated by the FPGA.

16Kbit dual-port RAM elastic buffers are used at the boundaries between I/Os and internal processing area.

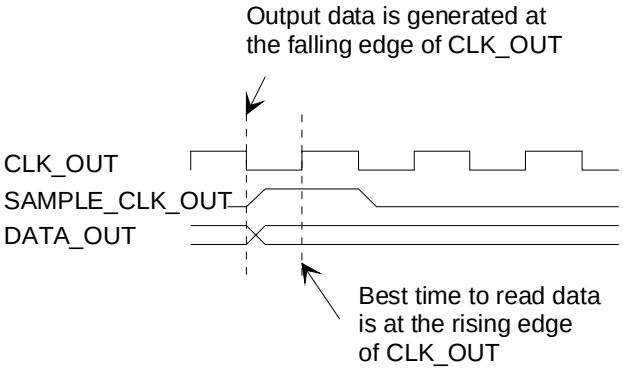
I/Os

All I/O signals are synchronous with the rising edge of the reference clock CLK_IN or CLK_OUT (i.e. all signals transitions always occur after the rising edge of clock). The maximum frequency for CLK_IN is 40 MHz. The frequency for CLK_OUT is fixed at 40 MHz .

Input



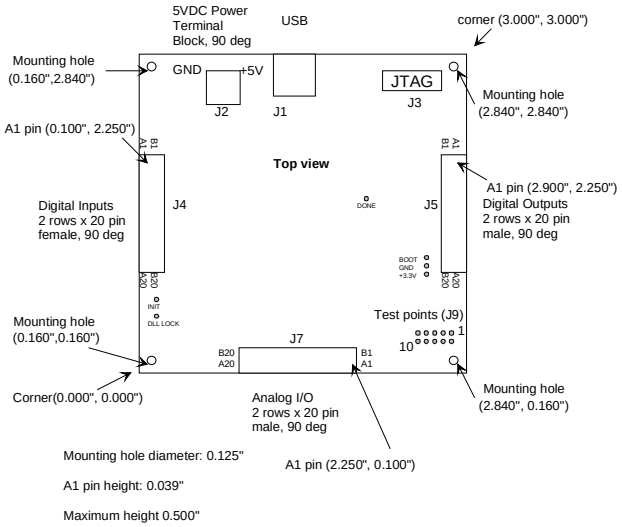
Output



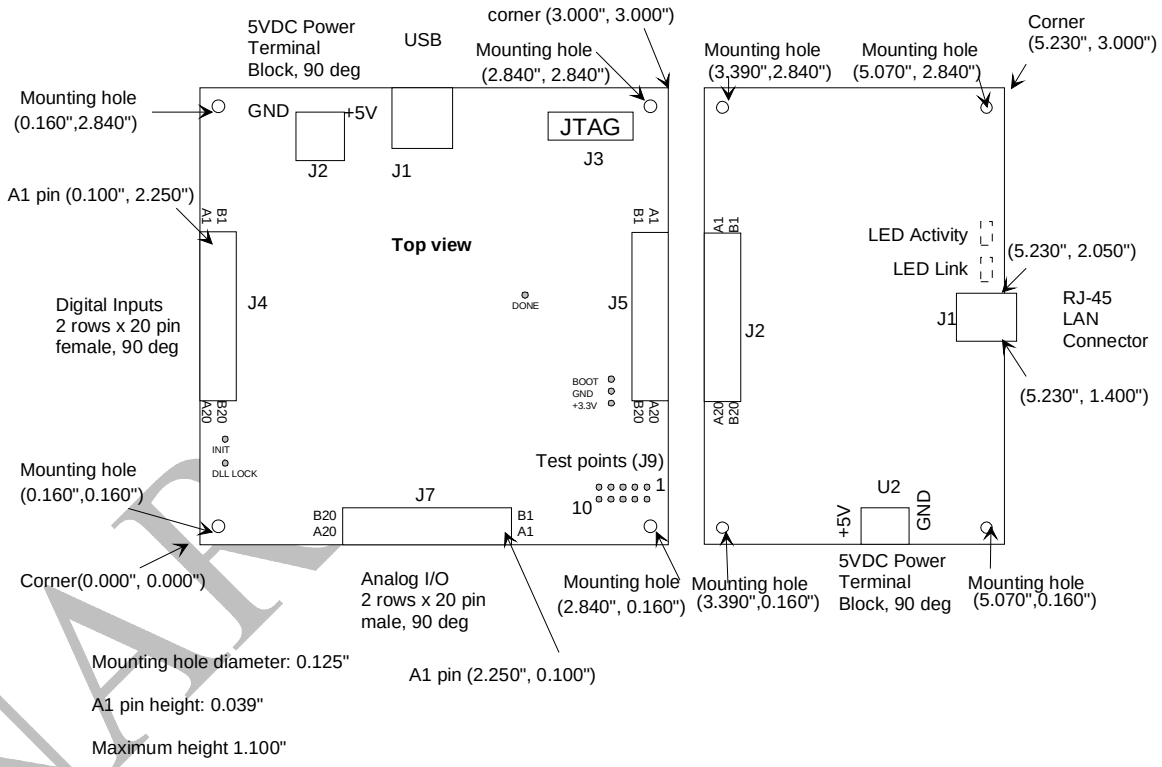
LEDs

2 LEDs located close to the LAN RJ-45 jack provide summary information as to the LAN: Link and activity.

Mechanical Interface



COM-1229



COM-1230

Schematics

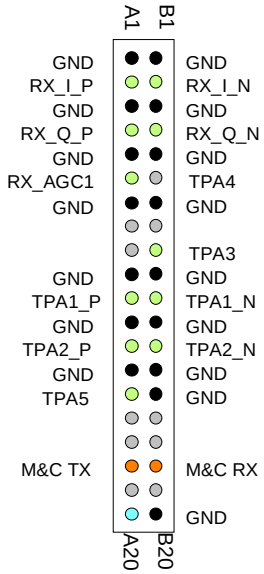
The board schematics are available on the ComBlock CD-ROM supplied with the module and on-line at http://www.comblock.com/download/com_1200schematics.zip

Pinout

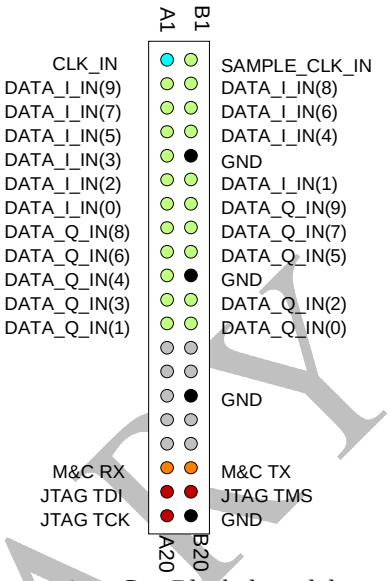
USB

USB type B receptacle, as the COM-1229/1230 is a USB device.

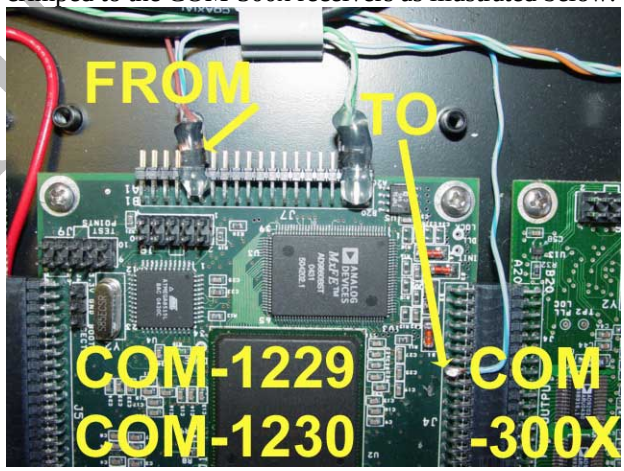
Analog I/O Connector J7



Input Connector J4

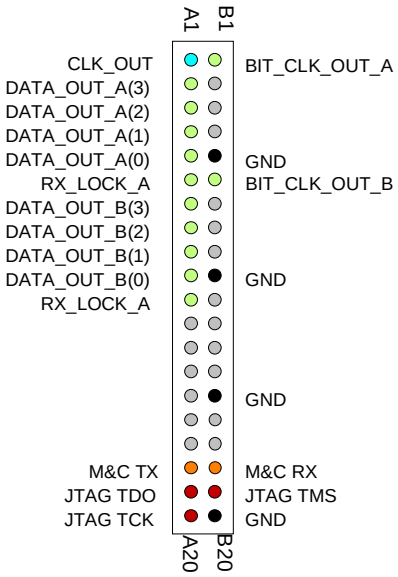


Note: unlike previous ComBlock demodulators, pin B13 does not supply a pulse-width modulated gain control signal to the RF/IF front-end. Instead, a more precise and faster-response analog gain control signal RX_AGC1 is available on J7/A6. Therefore, a wire must be soldered or crimped to the COM-300x receivers as illustrated below:



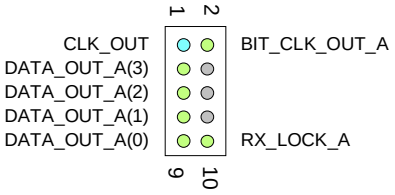
Analog AGC wire assembly instruction
for COM-300x receivers.
From COM-1229 J7/A6 to COM-300x pin B13.

Output Connector J5



The connector pinout shown above is used when demodulated data signals are routed to the output connector for direct ***point-to-point*** connection between two ComBlocks. See Output selection, REG37(2:0)). COM-1229 only. Not applicable for COM-1230.

Test/Output Connector J9



The connector pinout shown above is used when a demodulated data streams is routed to the J9 connector (See Output selection, REG37(2:0)).

I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-300x RF receivers[1]	COM-7001 Turbo code decoder
COM-350x RF transceivers	COM-1009 Convolutional decoder K=7
COM-1002 BPSK/QPSK/OQPSK digital modulator (back to back)	COM-8002 High-speed data acquisition. 256MB, 1Gbit/s, 50 Msamples/s.
COM-1028 FSK/MSK/GFSK/GMSK digital modulator (back to back)	
COM-1023 BER generator, AWGN generator	
COM-1024 Multipath simulator.	

Configuration Management

This specification is to be used in conjunction with VHDL software revision 1.

Comparison with Previous ComBlocks

Key Improvements with respect to COM-1001 BPSK/QPSK/OQPSK demodulator
- Includes digital anti-aliasing filter with variable decimation, thus alleviating the need for an external COM-1008. - 32-bit numerically controlled oscillators for carrier and symbol timing (versus 24-bit) - Significant increase in center frequency tuning range - Automatic AFC (versus manual) - Analog or Digital input signals (versus digital-only) - Analog gain control output for fast response (versus slower pulse-width modulated gain control). - User-programmable AGC response time. - Multiple output interfaces: USB2.0, TCP-IP (COM-1230), synchronous serial (versus synchronous serial only) - Built-in BER measurement, thus alleviating the need for an external COM-1005 - ComScope monitoring of key internal demodulator signals.
Key Improvements with respect to COM-1027 n-FSK demodulator
- Includes digital anti-aliasing filter with variable decimation, thus alleviating the need for an external COM-1008. - 32-bit numerically controlled oscillators for carrier and symbol timing (versus 24-bit) - Significant increase in center frequency tuning range - Automatic AFC (versus manual) - Analog or Digital input signals (versus digital-only) - Analog gain control output for fast response (versus slower pulse-width modulated gain control). - User-programmable AGC response time. - Multiple output interfaces: USB2.0, TCP-IP (COM-1230), synchronous serial (versus synchronous serial only) - Built-in BER measurement, thus alleviating the need for an external COM-1005 - ComScope monitoring of key internal demodulator signals.

[1] Requires soldering/crimping one wire for analog AGC.

ComBlock Ordering Information

COM-1229
Dual Demodulator: (n-FSK / n-PSK / QAM / APSK) with USB2.0 interface

COM-1230
Dual Demodulator: (n-FSK / n-PSK / QAM / APSK) with USB2.0 / TCP-IP interface

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