COM-1300
PCMCIA/CardBus FPGA DEVELOPMENT PLATFORM

Key Features

- Generic 16-bit PC Card / 32-bit CardBus Type II (5mm height) card for custom application development.
- Typical sustained data throughputs are 9.5 Mbit/s (PCMCIA), 100/40 Mbits/s (CardBus Transmit/Receive).
- Xilinx Spartan-3 XC3S400-4 FPGA features 400K system gates including 288Kbit of dual port memory and 16 dedicated 18x18 multipliers.
- 32MB SDRAM for use as elastic buffer.
- Development environment includes
  - Windows driver (.sys and .inf files)
  - VHDL top-level template code
  - NGC components for PCMCIA, CardBus and SDRAM controller
  - API and associated .jar and .dll files
  - C/C++ API and associated code examples
  - Hardware schematics
- Tools required (not provided):
  - Xilinx ISE with VHDL synthesis
  - Java development environment or
  - C++ compiler
- Supports **multiple personalities** and **dynamic reconfiguration**:
  - Up to 14 custom FPGA configurations can be stored in non-volatile flash memory.
  - The selected configuration is automatically reloaded at power up or upon command within 0.4 seconds.

Development Card with case
Right: 68-pin PCMCIA/CardBus interface
Left: 40-pin ComBlock interface

- Graphical User Interface, the ComBlock Control Center, is used for remote monitoring and control over simple serial link. This includes loading the FPGA configuration file into flash.
- Interface compatible with other pre-programmed ComBlock modules via the standard 2-row 40-pin 2mm connector.
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on a host computer.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1300.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm.

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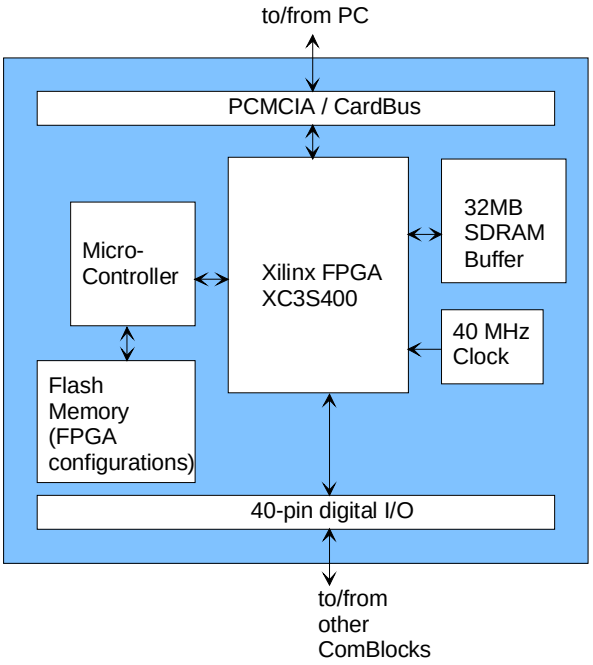
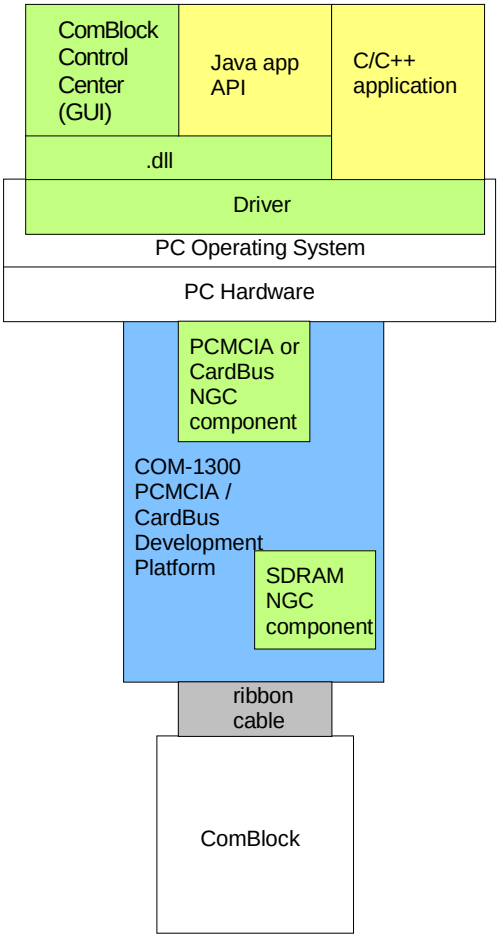
 Issued 7/31/2009



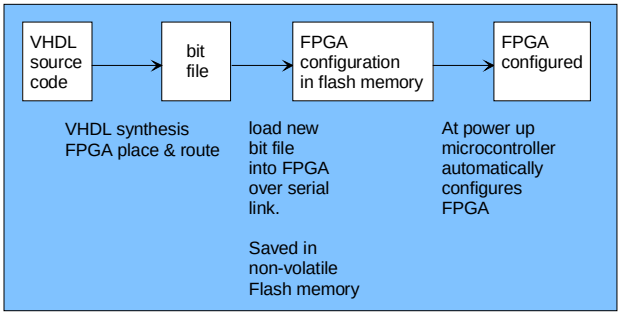
Development Card Hardware Block Diagram



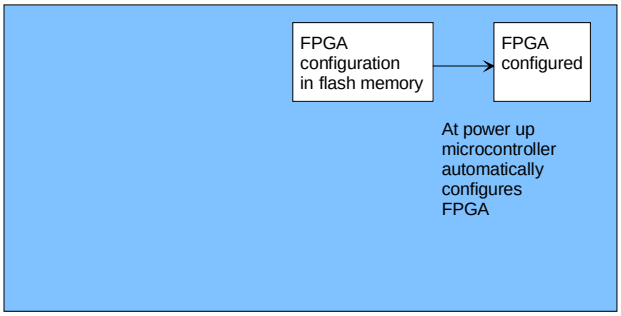
Software Development environment
Blue: supplied hardware
Green: supplied ready-to-use software
Yellow: application-level code examples.

Application Development Process

FPGA/VHDL



Development environment.



Run-time environment.

Operations

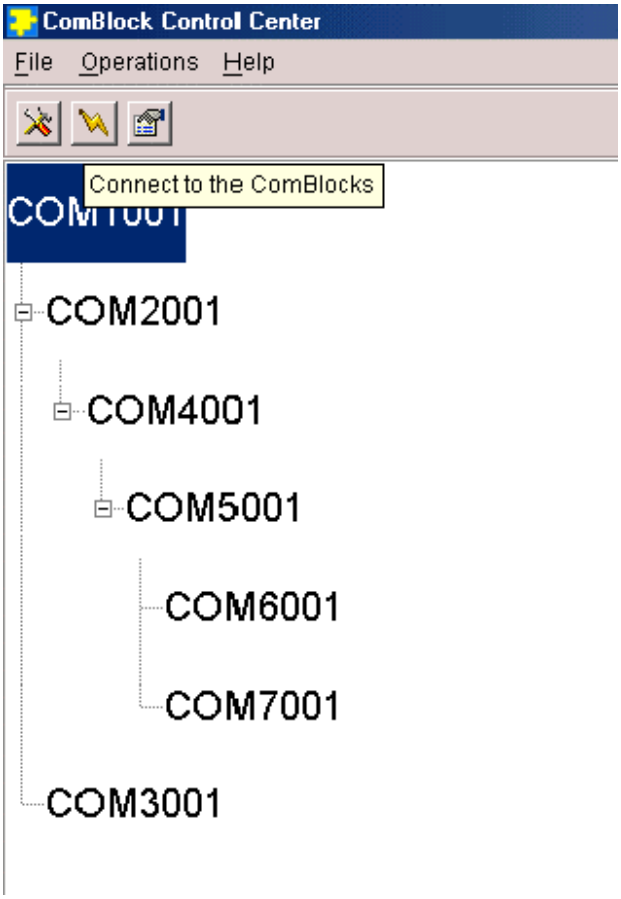
Graphical User Interface

A user-friendly graphical user interface, the ComBlock Control Center, is supplied with the COM-1300. The GUI runs on a host computer with a Windows operating system. It allows the user to communicate with the COM-1300 over the PCMCIA/CardBus interface and/or, when other ComBlocks are connected, via serial link or LAN.

The primary use of the ComBlock Control Center is

(a) To download new FPGA firmware (first stored into Flash memory)
(b) To set control registers
(c) To monitor status registers
(d) To capture and display internal signals (ComScope)

When activated, the ComBlock Control Center enumerates the ComBlock modules within the assembly. The modules are identified by their name in a tree-like structure. Each module can be configured and monitored remotely.



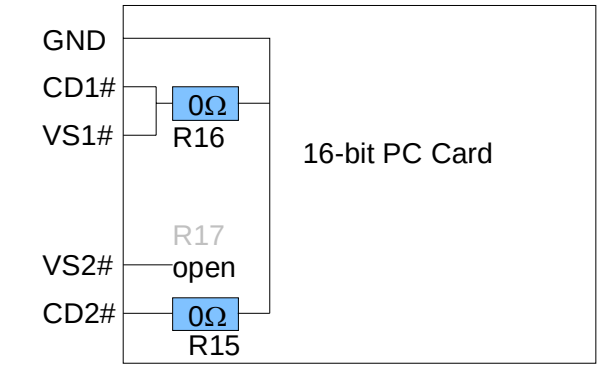
The ComBlock Control Center software is provided with all ComBlock modules. The user's manual can be found at
www.comblock.com/download/ccchelp.pdf

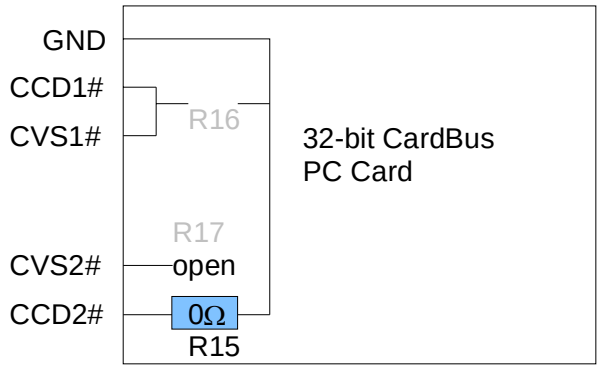
The ComScope user's manual can be found at
www.comblock.com/download/comscope.pdf

16/32-bit Interface

The 32-bit CardBus card employs the same 68-pin connector as used by the 16-bit PC card. However, most of the pin definitions are different, as well as the card detection and voltage sensing schemes.

The COM-1300 card can be configured as a 16-bit PCMCIA or a 32-bit CardBus Card. Although the bus pinout assignment is handled primarily by the FPGA under software control, the card detect pins must be configured hardware-wise by soldering/desoldering a 0Ω 0603 surface-mount resistors, as illustrated below.





At the time of ordering, the COM-1300 can be preconfigured for PCMCIA (**-P** option) or CardBus (**-C** option).

3V/5V Supply

The PC Card voltage is supplied through the PCMCIA/CardBus interface. It accepts any supply voltage in the range 3V – 6V.

The PC Card is wired so that the card detect pins and the voltage sense pins indicate to the host PC that a 3.3V initial supply voltage is needed. Likewise, the default CIS indicates that the card requires 3.3V supply for nominal operation.

Even though the FPGA itself is not 5V tolerant, The PC Card I/Os can safely connect to a 5V PCMCIA/CardBus bus thanks to 180Ω series resistors.

Flash Memory

The FPGA configuration is stored in non-volatile (Flash) memory. The ComBlock Control Center includes the utility to write the FPGA .mcs PROM file into the flash memory over the selected communication link between host computer and COM-1300.

At power up, the FPGA is automatically configured with the configuration file stored within the flash memory. Configuring the FPGA takes approximately 0.4 seconds.

Accidental FPGA file corruption

The COM-1300 is protected against corruption by an invalid FPGA configuration file. To recover from such occurrence, connect the BOOT SECTOR pin A20 to ground (pin B20) and insert the card into the host computer PCMCIA/CardBus slot. The card will be automatically configured with a default FPGA configuration that restores PCMCIA/CardBus communication. This boot file is unerasable. Once this is done, the user can safely re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center.

Multiple Configurations

Up to 14 distinct custom FPGA configurations can be retained in the Flash memory. The user can select which configuration is to be loaded at power up. Configuration time is typically less than 0.4 seconds. Unlike the other ComBlocks, a change in the FPGA configuration, whether from the graphical user interface or by software command, necessitates the removal and re-insertion of the PCMCIA/CardBus card into the slot. The user manual for the multiple configuration feature is available at http://comblock.com/download/dynamic_reconfig.pdf

Host <-> Target Communication Methods

The basic software supports two methods of bi-directional data exchange between host and target:

- One virtual bi-directional channel is I/O mapped and exchanges 8-bit wide data.
- The other virtual bi-directional channel is memory-mapped, exchanges 16-bit (PCMCIA) or 32-bit (CardBus) words and is optimized for maximum throughput.

The intent is to use the I/O mapped channel to communicate with ComBlock itself, for monitoring and control purposes. The Memory-mapped channel's intended use is for transferring payload data.
Beyond the basic software, developers can create multiple I/O and Memory-mapped channels by instantiating multiple VHDL components and specifying non-overlapping address ranges.

Electrical Interface

16-bit PCMCIA Interface

The cell shaded green indicates that the pin is under FPGA (software) control.

Pin: Signal	Definition
1:GND	Ground
2:D3	Data bit 3 (I/O)
3:D4	Data bit 4 (I/O)
4:D5	Data bit 5 (I/O)
5:D6	Data bit 6 (I/O)
6:D7	Data bit 7 (I/O)
7:CE1#	Card Enable 1, an active low signal to specify access to address locations which are transferred over D7: D0 (I)
8:A10	Address bit 10 (I)
9:OE#	Output Enable, active low and asserted during memory read transfer
10:A11	Address bit 11 (I)
11:A9	Address bit 9 (I)
12:A8	Address bit 8 (I)
13:A13	Address bit 13 (I)

14:A14	Address bit 14 (I)
15:WE#	Write Enable, active low and asserted during memory write transfer (I)
16:READY	Upon card insertion, the host will postpone reading the CIS until the ready signal is asserted. Typically occurs within 1 second after power is applied (time to load the FPGA) (O)
16:IREQ#	Once the initialization phase is complete, pin 16 can be used as an interrupt request. (O)
17:VCC	Card supply voltage (I)
18:VPP1	Programming Voltage (EPROM). Not applicable. Not connected. (I)
19:A16	Address bit 16 (I)
20:A15	Address bit 15 (I)
21:A12	Address bit 12 (I)
22:A7	Address bit 7 (I)
23:A6	Address bit 6 (I)
24:A5	Address bit 5 (I)
25:A4	Address bit 4 (I)
26:A3	Address bit 3 (I)
27:A2	Address bit 2 (I)
28:A1	Address bit 1 (I)
29:A0	Address bit 0 (I)
30:D0	Data bit 0 (I/O)
31:D1	Data bit 1 (I/O)
32:D2	Data bit 2 (I/O)
33:WP	Memory-only: Write Protect (O)
33:IOIS16	Memory or I/O: Can be used to tell the host that the current I/O transfer is 8 or 16-bit wide. (O)
34:GND	Ground
35:GND	Ground
36:CD1#	Card Detect 1, a status signal, pulled up to Vcc from the socket, and internally tied to ground in a PC Card (O)
37:D11	Data bit 11 (I/O)
38:D12	Data bit 12 (I/O)
39:D13	Data bit 13 (I/O)
40:D14	Data bit 14 (I/O)
41:D15	Data bit 15 (I/O)
42:CE2#	Card Enable 2, an active low signal to specify access to an odd address locations which transfer over D15: D8 (I)
43:VS1#/Refresh	Voltage sense 1, used by a low-voltage socket to determine the initial Vcc requirement (combined with VS2#) (O)
44:Reserved	Memory-only: Reserved
44:IORD#	Memory or I/O: I/O Read, asserted during I/O read (I)
45:Reserved	Memory-only: reserved
45:IOWR#	Memory or I/O: I/O Write, asserted during I/O write (I)
46:A17	Address bit 17 (I)
47:A18	Address bit 18 (I)
48:A19	Address bit 19 (I)
49:A20	Address bit 20 (I)
50:A21	Address bit 21 (I)
51:VCC	Card supply voltage (I)
52:VPP2	Programming Voltage 2 (EPROM). Not applicable, not connected. (I)
53:A22	Address bit 22 (I)
54:A23	Address bit 23 (I)
55:A24	Address bit 24 (I)
56:A25	Address bit 25 (I)
57:VS2#	Voltage sense 2, used by a low-voltage socket to determine Vcc requirement (combined with VS1#) (O)
58:RESET	Card reset signal that forces the PC Card to reset internal devices and clear its configuration registers. (I)
59:WAIT#	Wait signal for bus cycle control to extend normal access timing to the card (O)
60:Reserved	Memory-only: Reserved
60:INPACK#	Memory or I/O: The input port acknowledgement. It is asserted to indicate that an I/O read is in progress and the address is within the valid I/O range (I)
61:REG#	Identifies access to attribute memory: 1 for common memory read/write, 0 for attribute memory (CIS) read or I/O read/write (I)
62:BVD2/SPKR	Neither memory backup nor speaker functions used. FPGA to pull high. (O)
63:BVD1	Memory-only: Battery Voltage Detect 1 (Not applicable, no battery backup) (O)
63:STSCHG	Memory or I/O: Status Changed (Not applicable pin replacement register not used) (O)
64:D8	Data bit 8 (I/O)
65:D9	Data bit 9 (I/O)
66:D10	Data bit 10 (I/O)
67:CD2#	Card Detect 2, a status signal, pulled up to Vcc from the socket, and internally tied to ground in a PC card. (O)
68:GND	Ground

32-bit CardBus Interface

The cell shaded green indicates that the pin is under FPGA (software) control. The COM-1300 is assumed to be the target, not the initiator/master.

Pin: Signal	Definition
1: GND	Ground
2: CAD0	Address/Data bit 0 (I/O)
3: CAD1	Address/Data bit 1 (I/O)
4: CAD3	Address/Data bit 3 (I/O)
5: CAD5	Address/Data bit 5 (I/O)
6: CAD7	Address/Data bit 7 (I/O)
7: CC/BE0#	CardBus command or Byte Enable 0, to define type of transaction (I)
8: CAD9	Address/Data bit 9 (I/O)
9: CAD11	Address/Data bit 11 (I/O)
10: CAD12	Address/Data bit 12 (I/O)
11: CAD14	Address/Data bit 14 (I/O)
12: CC/BE1#	CardBus command or Byte Enable 1, to define type of transaction (I)
13: CPAR	Parity signal (I/O)
14: CPERR#	Data parity error (O)
15: CGNT#	Bus arbitration grant. Not applicable. FPGA pulls high (I)
16: CINT#	Interrupt request (O)
17: Vcc	Card supply voltage (I)
18: Vpp1	Programming Voltage 1 (EPROM). Not applicable, not connected. (I)
19: CCLK	CardBus clock signal, 0 to 33 MHz (I)
20: CIRDY#	Initiator ready (I)
21: CC/BE2#	CardBus command or Byte Enable 2, to define type of transaction (I)
22: CAD18	Address/data bit 18 (I/O)
23: CAD20	Address/data bit 20 (I/O)
24: CAD21	Address/data bit 21 (I/O)
25: CAD22	Address/data bit 22 (I/O)
26: CAD23	Address/data bit 23 (I/O)
27: CAD24	Address/data bit 24 (I/O)
28: CAD25	Address/data bit 25 (I/O)
29: CAD26	Address/data bit 26 (I/O)
30: CAD27	Address/data bit 27 (I/O)
31: CAD29	Address/data bit 29 (I/O)
32: RFU	Reserved for Future Use (I/O)
33: CCLKRUN#	Asserted by master if clock runs normally, de-asserted before clock stops or slow down (I/O)
34: GND	Ground
35: GND	Ground
36: CCD1#	Card detect 1 (O)
37: CAD2	Address/data bit 2 (I/O)
38: CAD4	Address/data bit 4 (I/O)
39: CAD6	Address/data bit 6 (I/O)
40: RFU	Reserved for Future Use (I/O)
41: CAD8	Address/data bit 8 (I/O)
42: CAD10	Address/data bit 10 (I/O)
43: CVS1#	Voltage Sense 1, same as PCMCIA (O)
44: CAD13	Address/data bit 13 (I/O)
45: CAD15	Address/data bit 15 (I/O)
46: CAD16	Address/data bit 16 (I/O)
47: RFU	Reserved for Future Use (I/O)
48: CBLOCK#	Lock the currently addressed memory target (I)
49: CSTOP#	Target wants to stop the transaction (O)
50: CDEVSEL#	Device select. Asserted by target upon successful decoding of the address and command. (O)
51: Vcc	Card supply voltage (I)
52: Vpp2	Programming Voltage 2 (EPROM). Not applicable, not connected. (I)
53: CTRDY#	Target ready (O)
54: CFRAME#	Data Frame indicator (I)
55: CAD17	Address/data bit 17 (I/O)
56: CAD19	Address/data bit 19 (I/O)
57: CVS2#	Voltage sense 2 (O)
58: CRST#	Reset signal. Forces all CardBus configuration registers to an initialized state. (I)
59: CSERR#	System error (O)
60: CREQ#	Arbitration request. Not applicable as the COM-1300 is never master. Pull high (I)
61: CC/BE3#	CardBus command or Byte Enable 3, to define type of transaction (I)
62: CAUDIO#	Card audio output. Not used: FPGA to pull high. (O)
63: CSTSCHG	Status change signal (O)
64: CAD28	Address/data bit 28 (I/O)
65: CAD30	Address/data bit 30 (I/O)
66: CAD31	Address/data bit 31 (I/O)
67: CCD2#	Card Detect 2 (O)
68: GND	Ground

40-pin ComBlock Interface

ComBlock / Digital I/O	Definition
J1/A1	External clock, an alternative to the internal 40 MHz clock.
J1/A18	Asynchronous serial communication with ComBlock. Maybe input (M&C_RX) or output (M&C_TX) depending on configuration. LVTTL (0-3.3V)
J1/B18	Asynchronous serial communication with ComBlock. Maybe input (M&C_RX) or output (M&C_TX) depending on configuration. LVTTL (0-3.3V)
J1/A20	BOOT_SECTOR signal. Establish connection to ground (B20) prior to inserting card into socket to activate default FPGA configuration link.

Absolute Maximum Ratings

Supply voltage	-0.5V min, +6V max
68-pin PCMCIA/CardBus interface inputs	-0.5V min, +5.25V max
40-pin connector inputs	-0.5V min, +3.6V max

Important: The I/O signals connected directly to the FPGA or Atmel microcontroller are NOT 5V tolerant!

Schematics

The board schematics are available on-line at http://www.comblock.com/download/com_1300schematics.zip

Software

PCMCIA/CardBus Drivers

Two software packages are provided to help developers create communication links between the COM-1300 platform and a host PC over the PCMCIA and CardBus interface respectively.

Each software package includes the following:

- Windows device driver for XP/2000 (.sys and .inf files)
- Java API
- Java simple application code example
- C/C++ simple application code example
- PCMCIA/CardBus NGC component for integration within the VHDL code

The software packages are available in the ComBlock CD and can also be downloaded from http://www.comblock.com/download/pcmcia.zip
User manuals for the PCMCIA / CardBus interfaces can be downloaded from www.comblock.com/download/PCMCIA_UserManual.pdf
and
www.comblock.com/download/CardBus_UserManual.pdf

Card Information Services (CIS)

The CIS is a data structure stored in non-volatile memory within the PC Card. It is read by the operating system to determine what kind of PC card is installed, along with its speed, size and the system resources required by the card. A detailed description of the CIS is provided in the PCMCIA/CardBus user manuals (see above). The CIS is defined as a ROM within the VHDL code.

VHDL code template

A VHDL template project is available on-line at http://www.comblock.com/download/com1300_003.zip

The template project includes:

- Two top-level VHDL source codes (.vhd), one for PCMCIA interface (**-P** option), the other for CardBus interface (**-C** option).
- NGC components for the PCMCIA, the CardBus and the SDRAM drivers.
- the constraint file (.ucf) listing all pin assignments.
- The Xilinx project with the synthesis and implementation settings.
- The resulting bit file (.mcs) ready to be loaded into flash memory.

The sample code describes how the application interfaces with the ComBlock Control Center graphical user interface through control and monitoring registers. The ComBlock Control user manual is available at www.comblock.com/download/ccchelp.pdf

It also describes how to capture key internal signals in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.

SDRAM_CONTROLLER NGC Component

The SDRAM_CONTROLLER component allows one to save up to 256 Mbits (32 MB) at high-speed into a synchronous SDRAM memory without having to take care of the SDRAM maintenance tasks such as refresh and initialization. The maximum operating conditions are:

- maximum clock speed: 50 MHz
- data bus width: 16-bit
- maximum write throughput: 400 Mbit/s.
- maximum read throughput: 400 Mbit/s.

The user simply specifies the start address, end address and generates a trigger pulse to start the upload (to the SDRAM) or the download (from the SDRAM) action.

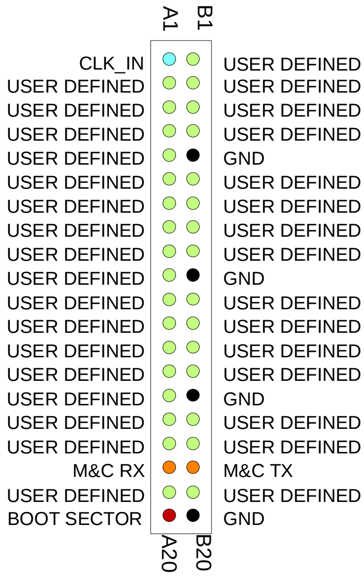
The component interface is as follows:

```
entity SDRAM_CONTROLLER is port (
--// CLOCK, RESET
ASYNC_RESET: in std_logic;
  -- Asynchronous reset, active high
CLK: in std_logic;
   -- Reference clock

--// Control signals
POWER_DOWN: in std_logic;
  -- High indicates low power mode. Low indicates normal
  -- mode. Note: after a power down the SDRAM will be
  -- re-initialized.

UPLOAD_START_ADDR: in std_logic_vector(23 downto 0);
  -- Upload start address. Each address represents one 16-bit word.
UPLOAD_END_ADDR: in std_logic_vector(23 downto 0);
  -- Upload end address. Each address represents one 16-bit word.
  -- IMPORTANT REQUIREMENT:
  -- number of words written i.e(UPLOAD_END_ADDR –
  -- UPLOAD_START_ADDR + 1)  MUST BE A MULTIPLE OF 4
  -- words.
START_UPLOAD_PULSE: in std_logic;
  -- One clock pulse wide pulse indicating that we want to start
  -- an upload session.
UPLOAD_COMPLETED_PULSE: out std_logic;
  -- One CLK wide pulse indicating that the current upload is
  -- completed.

DOWNLOAD_START_ADDR: in std_logic_vector(23 downto 0);
  -- Download start address. Each address represents one 16-bit word.
DOWNLOAD_END_ADDR: in std_logic_vector(23 downto 0);
  -- Download end address. Each address represents one 16-bit word.
  -- IMPORTANT REQUIREMENT:  number of words read i.e –
  -- (DOWNLOAD_END_ADDR -DOWNLOAD_START_ADDR+ 1)
  -- MUST BE A MULTIPLE OF 4 words.
 START_SINGLE_DOWNLOAD_PULSE: in std_logic;
   -- One clock pulse wide pulse indicating that we want to start
   -- a single download session.
 START_CONTINUOUS_DOWNLOAD_PULSE: in std_logic;
    -- One clock pulse wide pulse indicating that we want to start
    -- a continuous download session.

  STOP_CURRENT_OPERATION_PULSE: in std_logic;
     -- One clock pulse wide pulse indicating that we want to cancel the
     -- current upload or download session.

--// Monitoring signals
WRITE_POINTER_OUT: out std_logic_vector(23 downto 0);
READ_POINTER_OUT: out std_logic_vector(23 downto 0);
SDRAM_DOWNLOAD_IN_PROGRESS: out std_logic;
  -- Asserted if download is in progress, deasserted otherwise.
  -- Exactly the same signals as SINGLE_DOWNLOAD_FLAG OR:ed
  -- with CONTINUOUS_DOWNLOAD_FLAG.
SDRAM_UPLOAD_IN_PROGRESS: out std_logic;
  -- Asserted if upload is in progress, deasserted otherwise.
  -- Exactly the same signals as UPLOAD_FLAG.


--// User interface (write to SDRAM)
AT_LEAST_4_WORDS_AVAILABLE: in std_logic;
  -- User states that it is ready to write 4 words in rapid succession.
  -- Triggers a 4-word burst write cyle as soon as SDRAM is ready.
  -- Should stay high as long as 4-words of data are available for
  -- upload.  Enacted upon only if this component is in "UPLOAD"
  -- mode.
 DATA_IN: in std_logic_vector(15 downto 0);
  -- The 16 bit wide data word to be written to SDRAM.
  -- The user MUST provide the data in a timely manner, i.e. exactly
  -- one CLK after  a data word is requested by
  -- DATA_ON_INPUT_WANTED. 4 words are to be written in a row.
DATA_ON_INPUT_WANTED: out std_logic;
  -- Signal telling the user to send us data to be written to SDRAM.
  -- expect the data on the very next clock cycle after the request was
  -- made.


--// User interface (read from SDRAM)
DATA_OUT_4W_REQ: in std_logic;
  -- signal requesting 4 words from the SDRAM.
  -- Should stay high as long as data is needed.
  -- Valid only if this component is in 'DOWNLOAD (continuous or
  -- one-time)" mode.
DATA_OUT: out std_logic_vector(15 downto 0);
  -- Data retrieved from the SDRAM memory. Read at rising edge of
  -- CLK when DATA_OUT_CLK = '1'.
DATA_OUT_CLK: out std_logic;
  -- A one clock cycle per DATA_OUT wide pulse indicating that the
  -- data on the DATA_OUT lines are to be read.
FIRST_WORD_OUT: out std_logic;
  -- Signal indicating that the data currently being sent out is the
  -- first in the chosen window. Aligned with the DATA_OUT_CLK.
LAST_WORD_OUT: out std_logic;
  -- Only in use during a single download session. Signal indicating
  -- that the data currently being sent out is the last in the chosen
  -- window. Aligned with the DATA_OUT_CLK.

--// Test points
RD_TRIGGER: out std_logic;
  -- one CLK pulse at the start of a SDRAM burst read cycle
WR_TRIGGER: out std_logic;
 -- one CLK pulse at the start of a SDRAM burst write cycle

--// Direct SDRAM interface:
SDRAM_A: out std_logic_vector(12 downto 0);
  -- Address lines.
SDRAM_DQ: inout std_logic_vector(15 downto 0);
  -- Bi-directional data lines
SDRAM_BA0: out std_logic;
SDRAM_BA1: out std_logic;
SDRAM_CAS_N: out std_logic;
SDRAM_RAS_N: out std_logic;
SDRAM_WE_N: out std_logic;
SDRAM_CLK: out std_logic;
SDRAM_CKE: out std_logic;
SDRAM_CS_N: out std_logic;
SDRAM_DQML: out std_logic;
SDRAM_DQMH: out std_logic
);
end entity;
```

I/Os

Pinout

40-pin Digital Connector (Incoming data flow configuration)



40-pin (2 rows x 20 pins) 2mm corner female connector.

I/O Compatibility List

(Not an exhaustive list)

Incoming data flow
COM-3001/2/3/4/5/6/7/8/9 RF receivers.
COM-1001 BPSK/QPSK/OQPSK demodulator
COM-1418 Direct-sequence spread-spectrum demodulator
COM-1027 FSK/MSK/GFSK/GMSK demodulator
COM-1008 Variable decimation
COM-8002 High-speed data acquisition. 256MB, 40 Msamples/s.

Configuration Management

This specification is to be used in conjunction with VHDL code template software revision 3, and the ComBlock Control Center revision 2.36 or above.

PLEASE NOTE: the PCMCIA –P option requires a special version of the ComBlock Control Center: "setup_beta236PCMCIAsupport.exe" located on the CD-ROM shipped with the card.

ComBlock Ordering Information

COM-1300-**P** PCMCIA/CardBus FPGA Development Platform, PCMCIA preconfigured.

COM-1300-**C** PCMCIA/CardBus FPGA Development Platform, CardBus preconfigured.

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