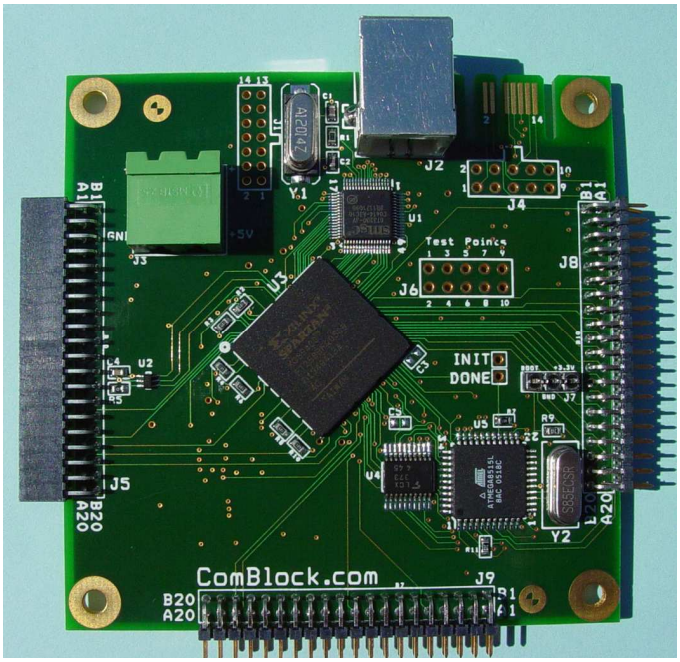
COM-1402
PSK / QAM / APSK DIGITAL MODULATOR

Key Features

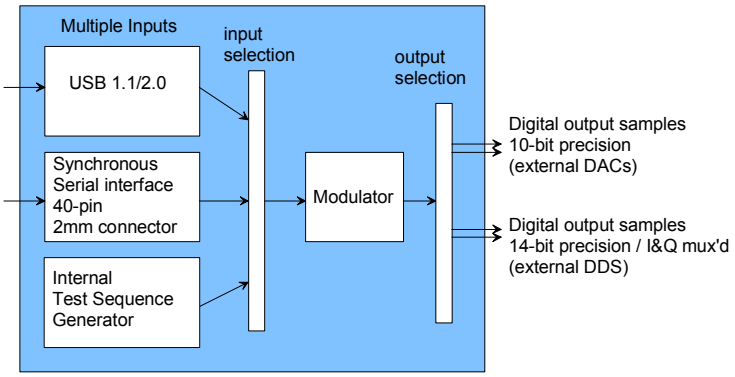
- Digital modulator with flexible configuration:
  - Modulation: BPSK, QPSK, OQPSK, π/4 DQPSK, 8-PSK, 16QAM, 16APSK, 32APSK.
  - Variable data rates up to 22 Msymbols/s.
  - Center frequency: +/- 10 MHz.
- Modulator outputs:
  - digital (2 * 10-bit complex, up to 90 Msamples/s)
  - digital (2 * 14-bit complex, up to 50 Msamples/s)
- Modulator data inputs:
  - synchronous serial interface, or
  - USB 1.1/2.0.
- Synchronization sequence (unique word) insertion to facilitate demodulator phase ambiguity removal.
- Internal generation of pseudo-random bit stream and unmodulated carrier for test purposes.
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Connectorized 3"x 3" module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom). Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1402.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .



Block Diagram



This PSK/QAM/APSK modulator is a generic modulator. It does NOT comply with the DVB-S2 (ETSI EN 302 307) physical layer specifications.

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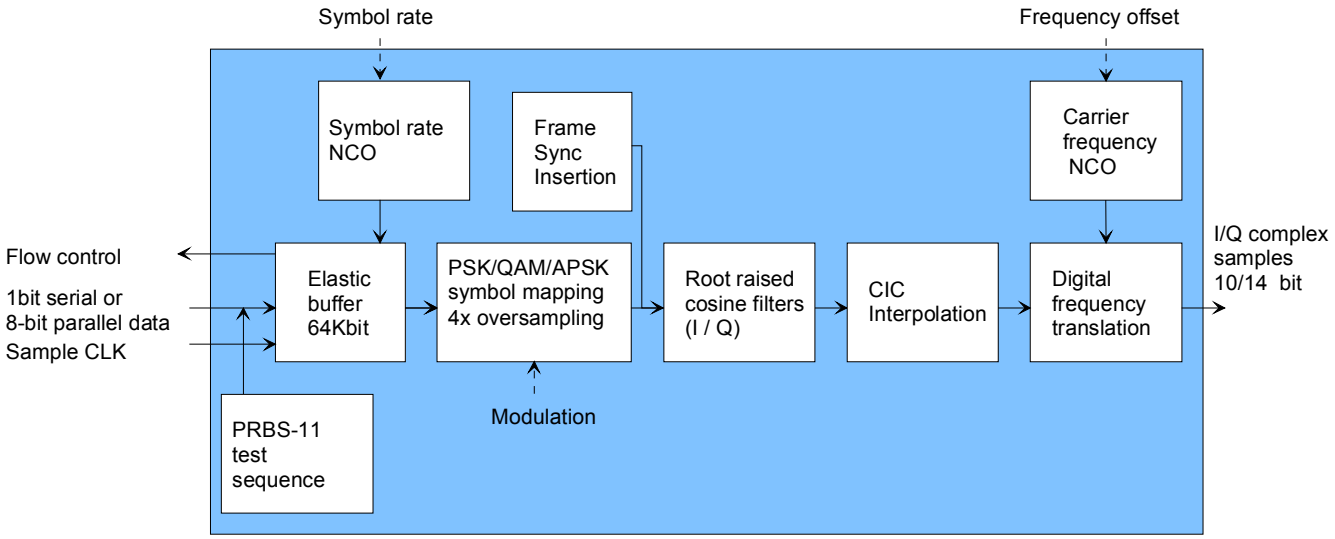


Functional Block Diagram

Electrical Interface

Two basic types of input connections are available for user selection:

- direct connection between data source and modulator.
- single data source to multiple modulators over a shared bus.

Modulator Digital Input Interfaces (J5) Direct connection between two ComBlocks, REG5(5) = '0'	**Definition**
DATA_IN	Input data stream. Can be configured as one-bit serial, or 8-bit parallel. When configured as 1-bit serial input, only DATA_IN(0) is used.
SAMPLE_CLK_IN	Input sample clock. One CLK-wide pulse. Read the input signals at the rising edge of CLK when SAMPLE_CLK_IN = '1'.
SAMPLE_CLK_IN_REQ	Output. One CLK_IN-wide pulse. Requests a data bits from the module upstream. For flow-control purposes.
CLK_IN	Input reference clock for synchronous I/O. DATA_IN, and SAMPLE_CLK_IN are read at the rising edge of CLK_IN. Maximum 40 MHz.

Input Module Interface Bus connection, REG5(5:4) = '11'	**Definition**
BUS_CLK_IN	40 MHz input reference clock for use on the synchronous bus.
BUS_ADDR[3:0]	Bus address. Input (since this module is a bus slave). Designates which slave module is targeted for this read or write transaction. All 1's indicates that the write data is to be broadcasted to all receiving slave modules. Read at the rising edge of BUS_CLK_IN
BUS_RWN	Read/Write#. Input (since this module is a bus slave). Indicates whether a read (1) or write (0) transaction is conducted. Read at the rising edge of BUS_CLK_IN. Read and Write refer to the bus master's perspective.

BUS_DATA[15:0]	Bi-directional data bus. Input when BUS_RWN='0'. Output when BUS_RWN='1'. Read data latency is 2 clock periods after the read command. Functional definition during write: • bit 0 SAMPLE_CLK_IN. '1' when DATA_IN is available • bit 1 DATA_IN data stream to modulator. • bits(15:2) undefined Functional definition during read: • bit 0 SAMPLE_CLK_IN_REQ requests data from the source. Used for flow control. • bits(15:1) undefined

Input Interfaces	**Definition**
USB 2.0	Type B receptacle. This interface supports two virtual channels: one for monitoring and control, the other to convey a high-speed modulated data stream from a host computer to the modulator. Use USB 2.0 approved cable for connection to a host computer. Maximum recommended cable length is 3'.

Two basic types of output connections are available for user selection:

- connection to dual 10-bit DACs, parallel I and Q samples, output sampling clock.
- connection to dual 14-bit DACs, multiplexed I and Q samples, input sampling clock.

Output Module Interface (Output data pushed out) Parallel 10-bit I & Q samples. REG9(2) ='0'	**Definition**
DATA_I_OUT[9:0]	Modulated output signal, real axis. 10-bit precision. Format: 2's complement or unsigned, selected by configuration bit 1.
DATA_Q_OUT[9:0]	Modulated output signal, imaginary axis. 10-bit precision. Same format as DATA_I_OUT.
SAMPLE_CLK_OUT	Output signal sampling clock. Read the output signal at the rising edge of CLK when SAMPLE_CLK_OUT = '1'. Sampling rate is either 4 x symbol rate or fclk (interpolation off/on configuration bit 7). SAMPLE_CLK_OUT can stay high when output samples are transmitted in successive CLK periods.
DAC_CLK_OUT	Output sampling clock for Digital to Analog Converters. DAC reads the output sample at the rising edge.
CLK_OUT	Output reference clock. Same as CLK internal processing clock. Typically 40 MHz.

Output Module Interface (Output data pulled) REG9(2) ='1'	**Definition**
SAMPLE_CLK_REQ_IN	Input. 100 MHz clock requesting output samples.
DATA_OUT[13:0]	Output. Quadrature baseband samples, 14-bit precision, 2's complement format. Bit 13 is the most significant bit. The in-phase (I) and quadrature (Q) samples alternate. Output samples are synchronous with the falling edge of SAMPLE_CLK_REQ_IN.
TX_ENABLE	Output. Transmit enable. Active high. The first sample after TX_ENABLE becomes active is an in-phase (I) sample.

Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the symbol clock rate (f_{symbol_clk}). The maximum power consumption is 650mA.

Important: Digital I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- USB

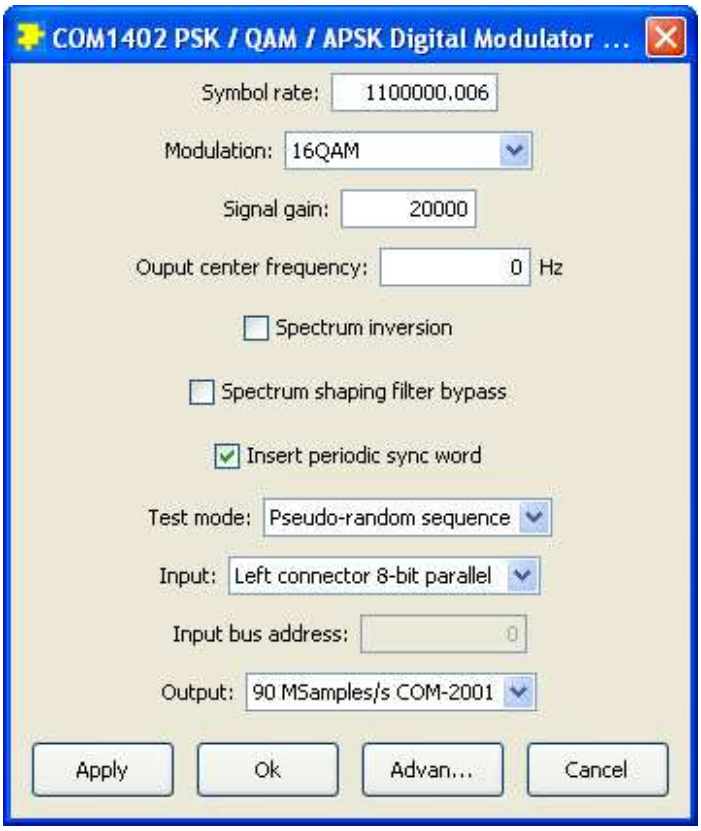
or connections via adjacent ComBlocks:

- USB
- TCP-IP/LAN,
- Asynchronous serial (DB9)
- PC Card (CardBus, PCMCIA).

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1402 is to use the ComBlock Control Center software supplied with the module(s).



After detecting the ComBlock modules (2nd button from left), highlight the COM-1402 module to be configured. Then press the settings button (3rd button from the left).

Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center "Advanced" configuration or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

This module operates at a fixed internal clock rate f_{clk} of 90 MHz.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

PSK/QAM/APSK Modulator	
Parameters	**Configuration**
Symbol rate (f_{symbol_clk})	32-bit unsigned integer expressed as fsymbol rate * 2^{32} / f_{clk}. The maximum symbol rate is f_{clk}/4 (0x3FFFFFFF). However, in practice it is recommended to limit the maximum symbol rate to 0.99*(f_{clk}/4) to account for possible clock drifts between modulator and demodulator. The data rate is between 1x and 6x the symbol rate depending on the modulation type. REG0 = bits 7-0 (LSB) REG1 = bits 15 – 8 REG2 = bits 23 – 16 REG3 = bits 31 – 23 (MSB)
Modulation type	0 = BPSK 1 = QPSK 2 = OQPSK 3-7 = reserved for future QPSK constellations 8 = 8PSK constellation 8A 9 = 8PSK constellation 8B 10 = 8PSK constellation 8C

	11 = 8PSK constellation 8D 12 = π/4 DQPSK (differential QPSK) 16 = 16QAM 24 = 16APSK, DVB-S2, γ = 2.85 32 = 32APSK, DVB-S2, γ1 = 2.84, γ2 = 5.27 REG4 bits 5-0
Spectrum inversion	Invert Q bit. This is helpful in compensating any frequency spectrum inversion occurring in a subsequent RF frequency translation. 0 = off 1 = on REG4 bit 6
Spectrum shaping filter bypass	0 = enable the root raised cosine filter (general case) 1 = bypass the root raised cosine filter (special use in applications when a root raised cosine filter is not used in the demodulator.) REG4 bit 7
Test mode	00 = disabled 01 = internal generation of 2047-bit periodic pseudo-random bit sequence as modulator input. (overrides external input bit stream). 10 = unmodulated carrier. (overrides external input bit stream) REG5 bits 1-0
Fixed / Adaptive symbol rate new	0 = the modulation symbol rate f_{symbol_clk} is fixed, as set in control registers REG0/3. Data is 'pulled' from the data source at the correct rate using flow-control. 1 = the modulator adjusts the symbol rate up to +/- 200ppm around the nominal f_{symbol_clk} . by tracking variations in the input. Data is 'pushed' by the data source without using flow control. Key requirement: the input rate must be within +/- 200ppm of its nominal (expected) value. REG5 bit 2
Tx unique word	Insert a periodic 32 bit Unique Word (synchronization sequence) to assist the demodulator in synchronizing and recovering ambiguities. The unique word is 5A 0F BE 66, transmitted MSb first. 2048 data symbols are transmitted between successive unique words. The unique word is using a simplified BPSK modulation, irrespective of the modulation type. The frame size is thus 2080 symbols. 0 = disabled 1 = periodically insert a Unique Word. REG5 bit 3

Input selection	Select the origin of the modulator input data stream. 00 = 1-bit serial from left connector, direct point to point connection. 01 = 8-bit parallel from left connector, direct point to point connection. 10 = 8-bit parallel from USB. 11 = 1-bit serial bus interface through left connector (COM-8004 interface) Note: MSb of the 8-bit parallel byte is transmitted first. Note: the input is disabled when the internal test mode is on. See above. REG5 bits 5-4
Signal gain	Signal level. 16-bit unsigned integer. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Therefore, we recommend checking for saturation at test point TP4 (or using ComScope trace 1 signal 4 for example) when changing either the symbol rate or the signal gain. REG6 = bits 7-0 (LSB) REG7= bits 15-8 (MSB)
Output Center frequency (f_{cout})	Frequency translation. 32-bit signed integer (2's complement representation) expressed as $f_{cout} * 2^{32} / f_{clk}$. Maximum recommended range: ± 10 MHz. REG8 = bits 7-0 (LSB) REG9 = bits 15 – 8 REG10 = bits 23 – 16 REG11 = bits 31 – 23 (MSB)
Output selection	Direct the modulator output to one of several possible interfaces: 0 = digital 2*10-bit precision unsigned, J8/J9 right/bottom connectors resampled at 40 MSamples/s. Compatible with most ComBlocks, including the COM-2001 dual D/A converter. 1 = digital, 2*14-bit precision, signed, J8/J9 right/bottom connectors., resampled at 50 Msamples/s. Compatible with COM-4004. 2 = digital 2*10-bit precision unsigned, J8/J9 right/bottom connectors at 90 MSamples/s (no resampling at output). Compatible with COM-2001 dual D/A converter

	REG12 bits 2-0
Input Bus address	Unique 4-bit address identifying this module on the input bus (if the input bus is enabled in REG5 bits 5-4). Ignore otherwise. This module acts as bus slave: it performs the read/write transaction requested by the bus master if and only if the bus address matches its own address defined here. This address must be unique among modules connected to the same bus in order to avoid conflicts. REG13 bits 3-0

Writing to REG13 resets the output interface. When interfacing with the COM-4004 70 MHz modulator, any configuration change in the COM-4004 should be followed by an interface reset. (otherwise, a spectral inversion may occur).

Configuration example:
REG3/2/1/0 = 38 E3 8E 38
REG4 = 01
REG5 = 09
REG7/6 = 60 00
REG11/10/9/8 = 00
REG12 = 00
REG13 = 00
configures the modulator as follows:
symbol rate = 20 Msymbols/s
QPSK, no spectrum inversion, insert periodic synchronization pattern, input is 2047-bit pseudo-random bit stream generation, no frequency offset, unsigned output format

Monitoring

Digital status registers are read-only.

USB 2.0 Connection Monitoring	
Parameters	**Monitoring**
Number of bytes received from host PC to digital modulator over USB	32-bit byte count. Counter rolls over when reaching 0xFFFFFFFF. SREG0: bits 7-0 (LSB) SREG1: bits 15-8 SREG2: bits 23-16 SREG3: bits 31-24 (MSB)

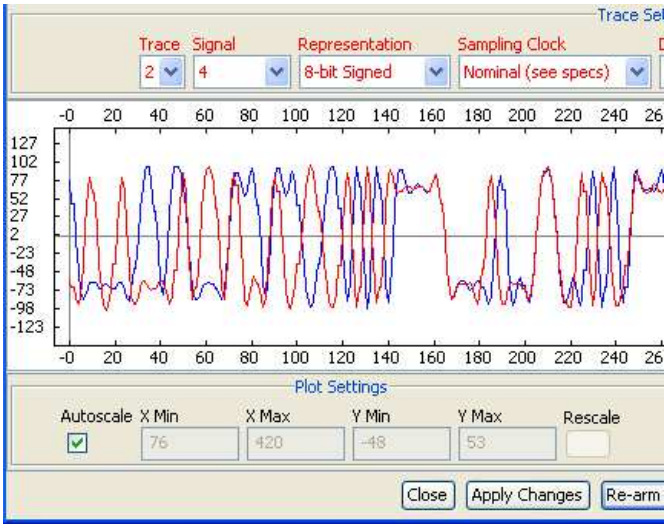
ComScope Monitoring

Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-1402 signal traces and trigger are defined as follows:

Trace 1 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: serial bit stream	8-bit signed	Bit rate	512
2: modulator symbol (I-channel) before channel filter. Ideal constellation	8-bit signed	f_{symbol_clk}	512
3: baseband Q-channel modulator output (after channel filter, before frequency translation and interpolation)	8-bit signed	$4*f_{symbol\_clk}$	512
4: modulator output (I-channel) after frequency translation & interpolation	8-bit signed	f_{clk}	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: symbol stream	8-bit signed	f_{symbol_clk}	512
2: modulator symbol (Q-channel) before channel filter. Ideal constellation	8-bit signed	f_{symbol_clk}	512
3: baseband I-channel modulator output (after channel filter, before frequency translation and interpolation)	8-bit signed	$4*f_{symbol\_clk}$	512
4: modulator output (Q-channel) after frequency translation & interpolation	8-bit signed	f_{clk}	512
Trigger Signal	**Format**		
1: start of PRBS-11 internal test sequence	Binary		
2: Unique word symbol insertion	Binary		

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk} processing clock as real-time sampling clock.

In particular, selecting the f_{clk} processing clock as real-time sampling clock allows one to have the same time-scale for all signals.



ComScope monitoring the modulator output (QPSK)

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.

Digital Test Points (J6)

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
TP1	USB received sample clock. 11ns pulse for each byte received.
TP2	Input data, DATA_IN(0)
TP3	Input data, DATA_IN(1)
TP4	Interpolation filter saturation (if so, reduce the signal gain as it may affect the output spectrum shape).
TP5	Elastic buffer serial output bit stream
TP6	Elastic buffer serial output sample clock
TP7	Unique word flag, '1' during 32-symbol unique word insertion.
TP8	PRBS-11 test sequence
TP9	PRBS-11 sample clock
TP10	PRBS-11 periodic start of test sequence
INIT	f_{clk} /8 = 11.25 MHz
DONE	'1' when the FPGA is properly configured

Operation

Differential Encoding

In low data rate applications where phase noise may become a problem, link performances can be improved by using differential encoding. At the encoder, the symbol information transforms into a phase shift, not an absolute phase. For QPSK, the phase shift is as follows:
The symbol 00 is mapped into +0 deg
The symbol 01 is mapped into +90 deg
The symbol 10 is mapped into +180 deg
The symbol 11 is mapped into +270 deg

For BPSK, the phase shift is as follows:
The bit 0 is mapped into +0 deg
The bit 1 is mapped into +180 deg

Unique Word

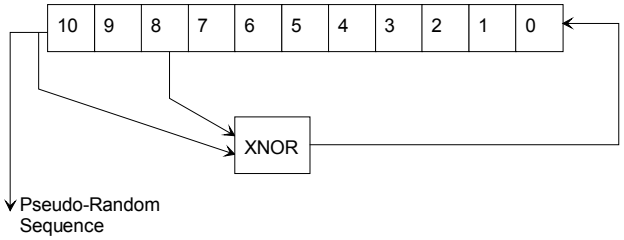
A unique word can be inserted periodically every 2048 data symbols to resolve phase ambiguities at the demodulator. This feature should only be enabled when used in conjunction with a compatible demodulator (i.e. designed to recognize this specific unique word and frame length).

The unique word is 32-bit long:
01011010 00001111 10111110 01100110 (binary)
0x 5A 0F BE 66 (hex)
The most significant bit (left-most) is transmitted first.

The unique word is always modulated as differentially encoded BPSK, irrespective of the modulation selected for the following 2048 symbols.

Pseudo-Random Bit Stream

A periodic pseudo-random sequence can be used as modulator source instead of the input data stream. A typical use would be for end-to-end bit-error-rate measurement of a communication link. The sequence is 2047-bit long maximum length sequence generated by an 11-tap linear feedback shift register:



The first 100 bits of the PN sequence are as follows:
0000000000 0111111111 0011111110 0001111100
1100111000 0000010011 1111010001 1110110100
1101001100 0011000001

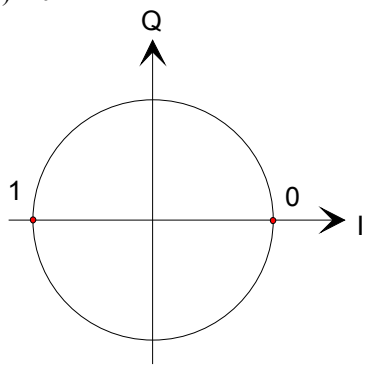
Performance

Constellation: Symbol Mapping

The serial input data stream is packed into symbols with the Most Significant bit first.

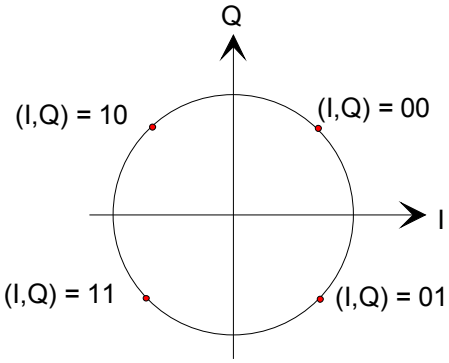
BPSK

REG31(5:0) = 0



QPSK

REG31(5:0) = 1
Gray encoding.



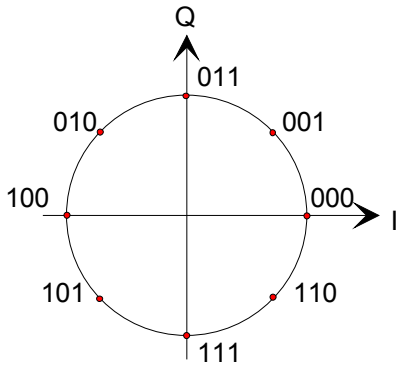
π/4 DQPSK

REG31(5:0) = 12

Input symbol	Phase shift
00	+ π/4
01	+ 3π/4
10	- π/4
11	-3π/4

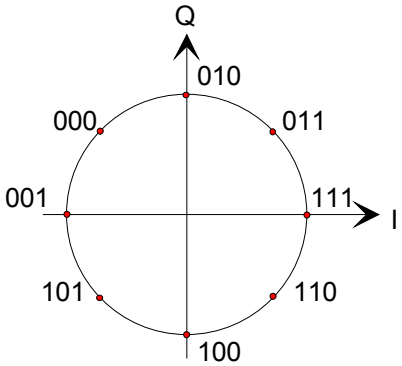
8PSK (1)

REG31(5:0) = 8



8PSK (2)

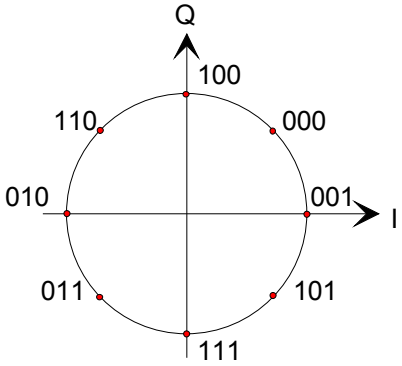
REG31(5:0) = 9



8PSK (3)

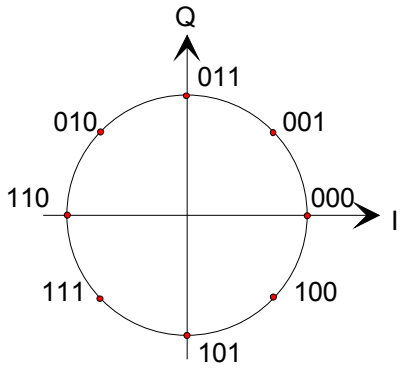
REG31(5:0) = 10

Gray encoded.



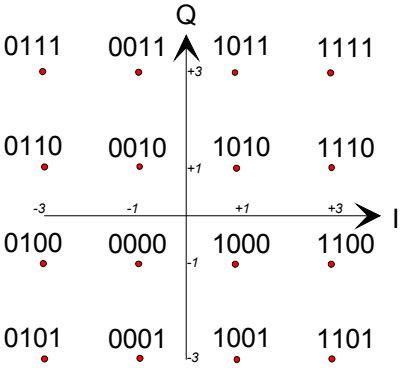
8PSK (4)

REG31(5:0) = 11



16QAM

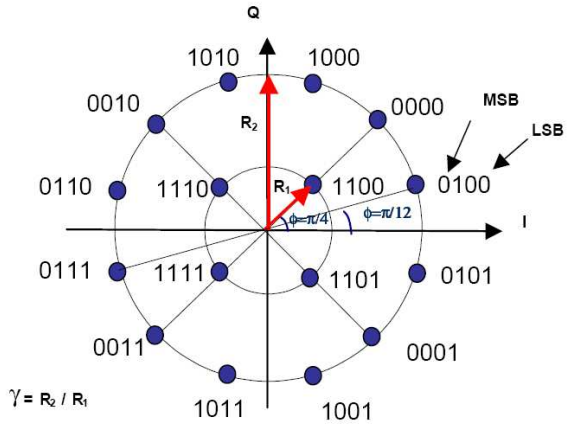
REG31(5:0) = 16



16APSK

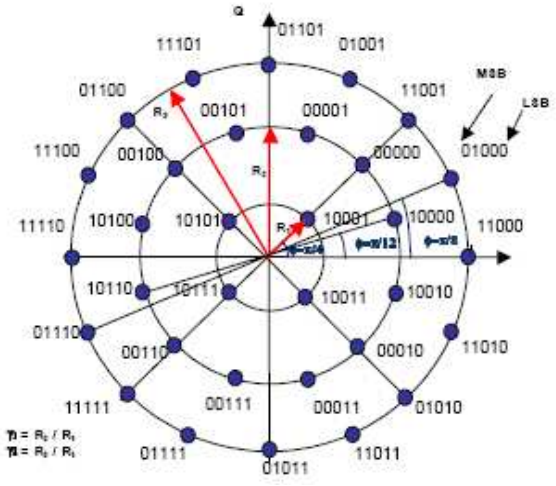
REG31(5:0) = 24

$\gamma = R2 / R1 = 2.85$, best for code rate 3/4



32APSK

REG31(5:0) = 32
γ1 = 2.84, γ2 = 5.27, best for code rate 3/4



Filter Response

The channel filter is a root raised cosine filter, which is applied to both In-phase and Quadrature signals at baseband. In order to minimize intersymbol interferences, one expects the same filter to be used at the demodulator. To this effect, users can select one of several rolloff factors: 20%, 25%, 35% and 40%. Changing the rolloff selection requires loading the firmware once using the ComBlock control center, then switching between up to four stored firmware versions (it takes 0.5 seconds).

All firmware versions can be downloaded from www.comblock.com/download.

COM-1402-A 20% rolloff

COM-1402-B 25% rolloff

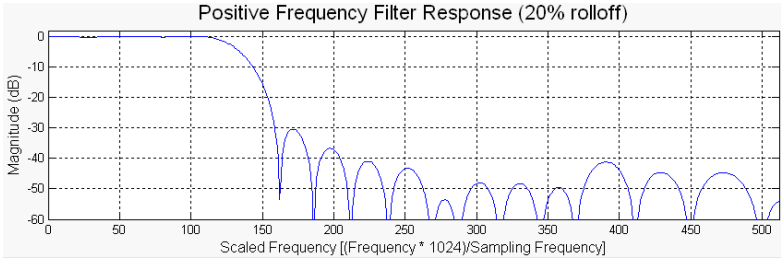
COM-1402-C 30% rolloff

COM-1402-D 35% rolloff

COM-1402-E 40% rolloff

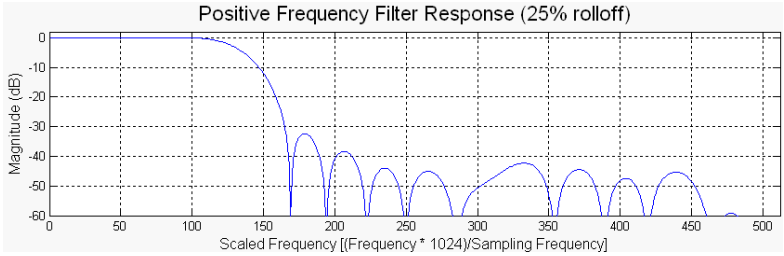
To verify which firmware is currently installed, open the settings window and click on the "Advanced" button. The firmware option is listed at the bottom of the advanced settings window.

Filter Response (-A 20% rolloff)



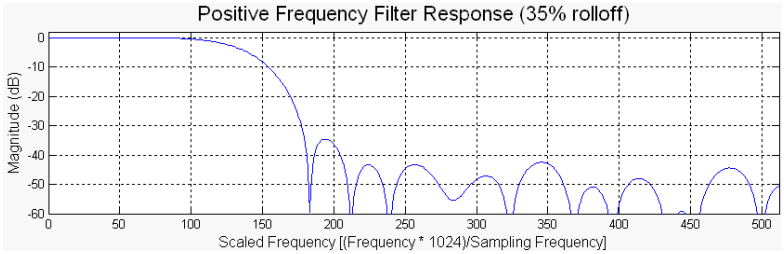
*(filter response normalized. 512 = 2*symbol rate)*

Filter Response (-B 25% rolloff)



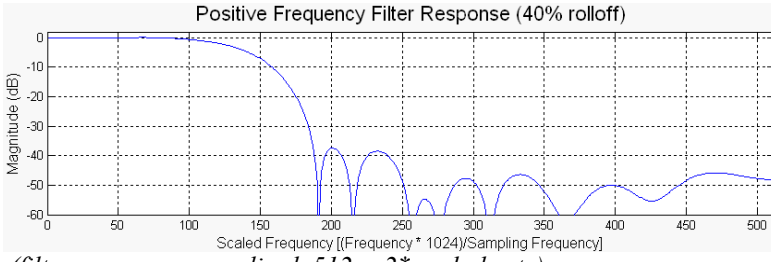
*(filter response normalized. 512 = 2*symbol rate)*

Filter Response (-D 35% rolloff)



*(filter response normalized. 512 = 2*symbol rate)*

Filter Response (-E 40% rolloff)



*(filter response normalized. 512 = 2*symbol rate)*

USB Interface

USB Throughput Benchmarks

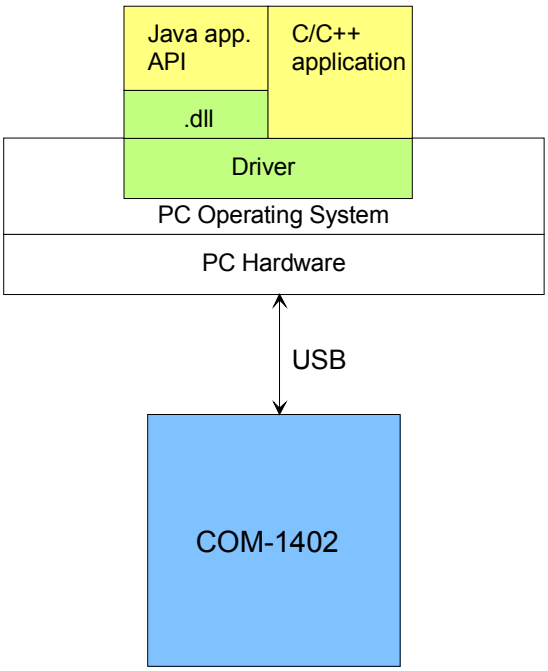
The COM-1402 is capable of a sustained (average) throughput of 85 Mbits/s over USB 2.0. In most cases, the sustained throughput is limited by the host computer and the application(s) running on the host computer.

Client Programming : USB 2.0

Software to help developers create USB high-speed communications between the COM-1402 and a host PC is provided. The **USB 2.0 software package** includes the following:

- Windows device driver for XP/2000/Me (.sys, .inf files)
- Java API, .dll and application sample code
- C/C++ application sample code

The **USB 2.0 software package** is available in the ComBlock CD and can also be downloaded from ComBlock.com/download/usb20.zip.
The user manual is available at ComBlock.com/download/USB20_UserManual.pdf

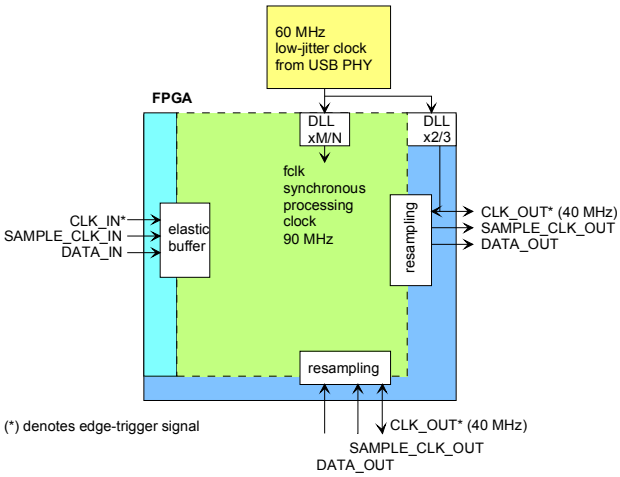


Blue: supplied hardware
Green: supplied ready-to-use software
Yellow: source code examples

Timing

Clocks

The clock distribution scheme embodied in the COM-1402 is illustrated below.



Baseline clock architecture
Yellow = 60 MHz reference clock
Green = f_{clk} processing zone
Dark Blue = 40/90 MHz output clock
Light Blue = 40 MHz external input clock

The core signal processing performed within the FPGA is synchronous with the processing clock $\mathbf{f_{clk}}$. In order to minimize clock jitter, the processing clock is derived from a 60 MHz reference clock with low-jitter. $\mathbf{f_{clk}}$ is not related to the CLK_IN clock. $\mathbf{f_{clk}}$ is used for internal processing.

The signals at the digital input connector J5 are synchronous with the CLK_IN signal at pin J5/A1. This clock can be 40 MHz.

The signals at the digital output connectors J8/J9 can be selected to be synchronous with the 40 MHz CLK_OUT or the 90 MHz $\mathbf{f_{clk}}$ derived from the 60 MHz reference clock.

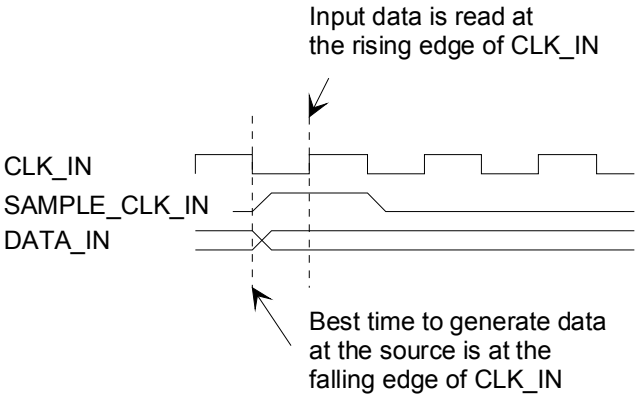
A 64Kbit elastic buffer is used at the boundary between input and internal processing area.

I/Os

The I/O signals on the 40-pin connectors are synchronous with a reference clock, as illustrated with the following timing diagrams:

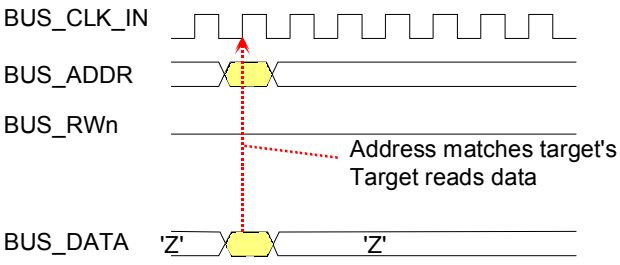
Input

Point to Point connection (REG5(5) = ‘0’)

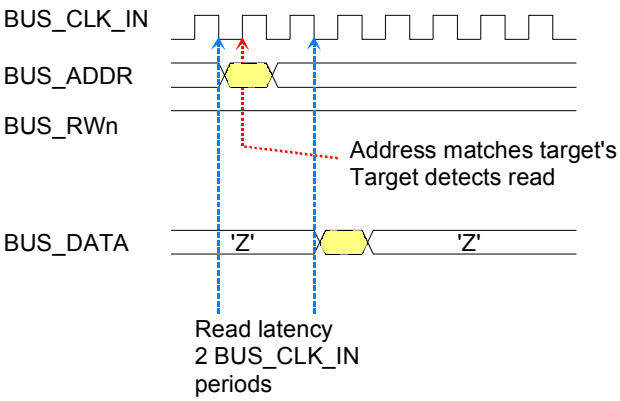


Input

Point to Multi-points connection (REG5(5:4) = ‘11’).
COM-1402 is a bus slave. It always listens to
BUS_CLK_IN, BUS_ADDR, BUS_RWN.



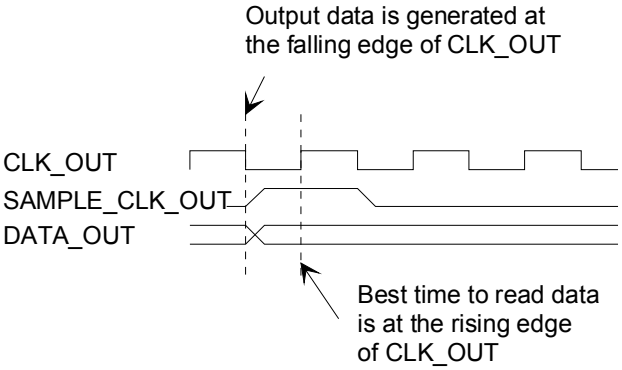
Master writes data streams to COM-1402 target(s)



Master reads flow control from COM-1402 target

Output

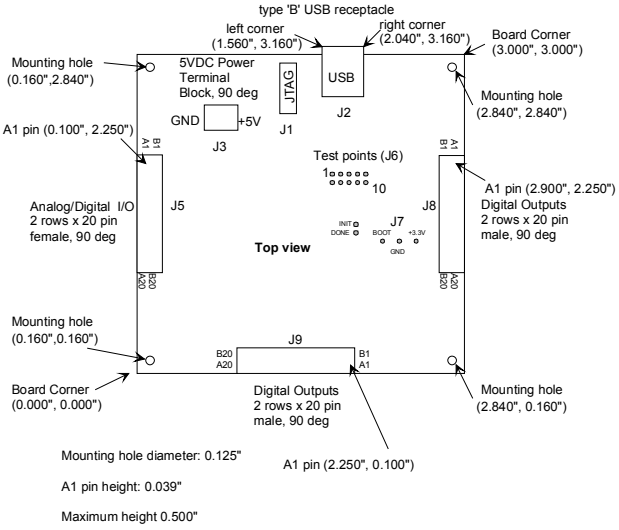
COM-2001/Dual DAC interface (REG12(2:0) = 001)



Schematics

The board schematics are available on the ComBlock CDROM shipped with the board. The schematics are also available on-line at ComBlock.com/download/com_1400schematics.pdf

Mechanical Interface



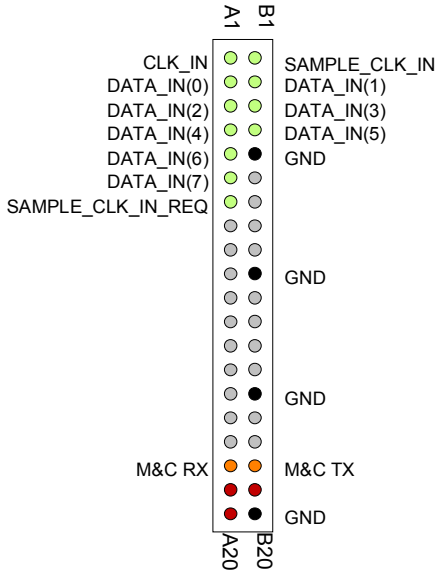
The front dimensions (plug face) of a type ‘B’ USB receptacle are 12 mm wide by 11 mm tall (above the board.)

Pinout

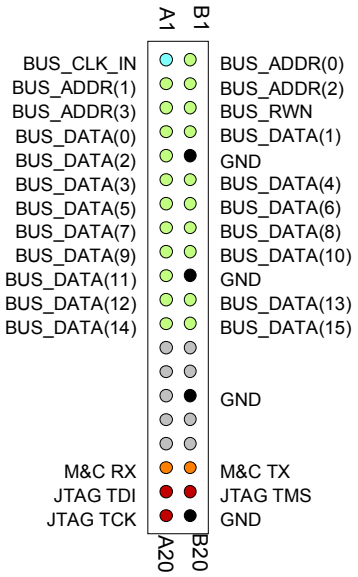
USB

USB type B receptacle, as the COM-1402 is a USB device.

Input Connector J5

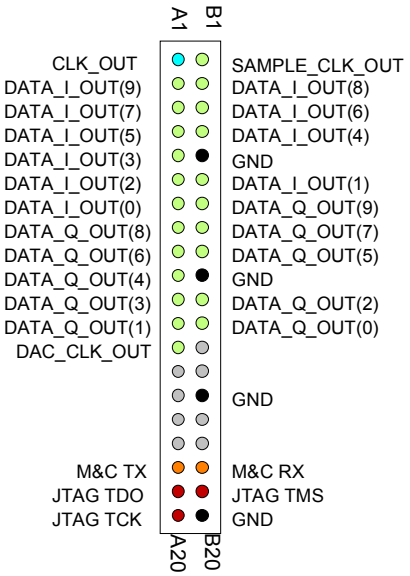


This connector is used for point-to-point input, i.e. direct connection between two ComBlocks when control register REG5(5) = '0'.

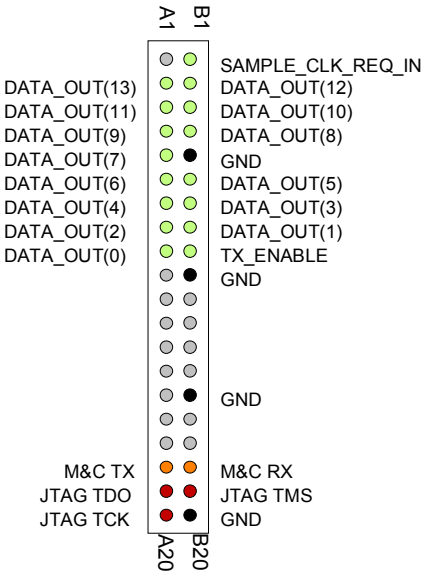


This connector is used for point-to-multipoint (bus) connection when control register REG5(5:4) = '11'. COM-1402 is a bus slave. It always listens to BUS_CLK_IN, BUS_ADDR, BUS_RWN.

Output Connectors J8, J9



COM-2001/Dual DAC interface configuration (REG12(0) = '0').



COM-4004/DDS interface configuration (REG12(0) = '1').

I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-1010 Convolutional encoder	COM-1202 PSK/QAM/APSK modem (back to back)
COM-7002 Turbo Code Error Correction	COM-2001 digital-to-analog converter (baseband).
COM-8001 Pattern generator 256MB	COM-4004 70 MHz IF modulator
COM-8004 Signal diversity splitter	COM-1023 BER generator, Additive White Gaussian Noise Generator
COM-5003 TCP-IP / USB Gateway	COM-1024 Multipath simulator.

Configuration Management

This specification is to be used in conjunction with VHDL software revision 13.

Comparison with Previous ComBlocks

Key Improvements with respect to COM-1002 BPSK/QPSK/OQPSK modulator
- Several additional modulations: π/4 DQPSK, 8PSK, 16QAM, 16APSK, 32APSK. - Higher symbol rate (22 versus 10 MSymbols/s). - Includes CIC interpolation filter for improved aliasing rejection when transmitting low data rates. - 32-bit numerically controlled oscillators for carrier and symbol timing (versus 24-bit) - Significant increase in center frequency tuning range - Multiple input interfaces: USB2.0, synchronous serial, synchronous parallel (versus synchronous serial only) - ComScope monitoring of key internal modulator signals.

ComBlock Ordering Information

COM-1402
PSK/QAM/APSK digital modulator

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