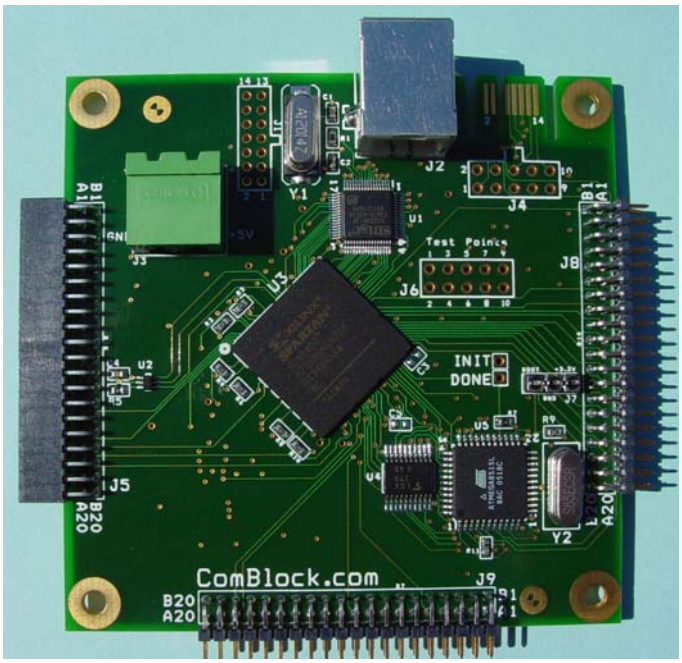
COM-1418 DIRECT SEQUENCE SPREAD-SPECTRUM DEMODULATOR 22 Mchip/s

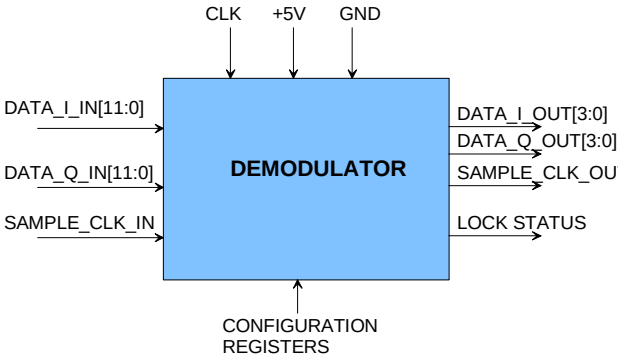
Key Features

- Direct sequence spread-spectrum digital demodulator.
- Variable chip rate up to 22 Mchips/s.
- Spreading factor: 3 to 2047
- Spreading codes:
  - Gold sequences
  - Maximal length sequences
  - Barker codes (length 11, 13)
  - GPS C/A codes.
  - Truncated codes.
- BPSK, QPSK selectable.
- Center frequency: +/- 10 MHz.
- Demodulation performances: within 1.5 dB from theory at threshold SNR of 5 dB.
- Sequential code search.
  False code-lock prevention.
- 4-bit soft-quantized demodulated bits to USB or synchronous output.
- Monitoring:
  - Receiver lock
  - Carrier frequency error
  - SNR
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right). Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.



Electrical Interface

Demodulator Inputs / Outputs



For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1418.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

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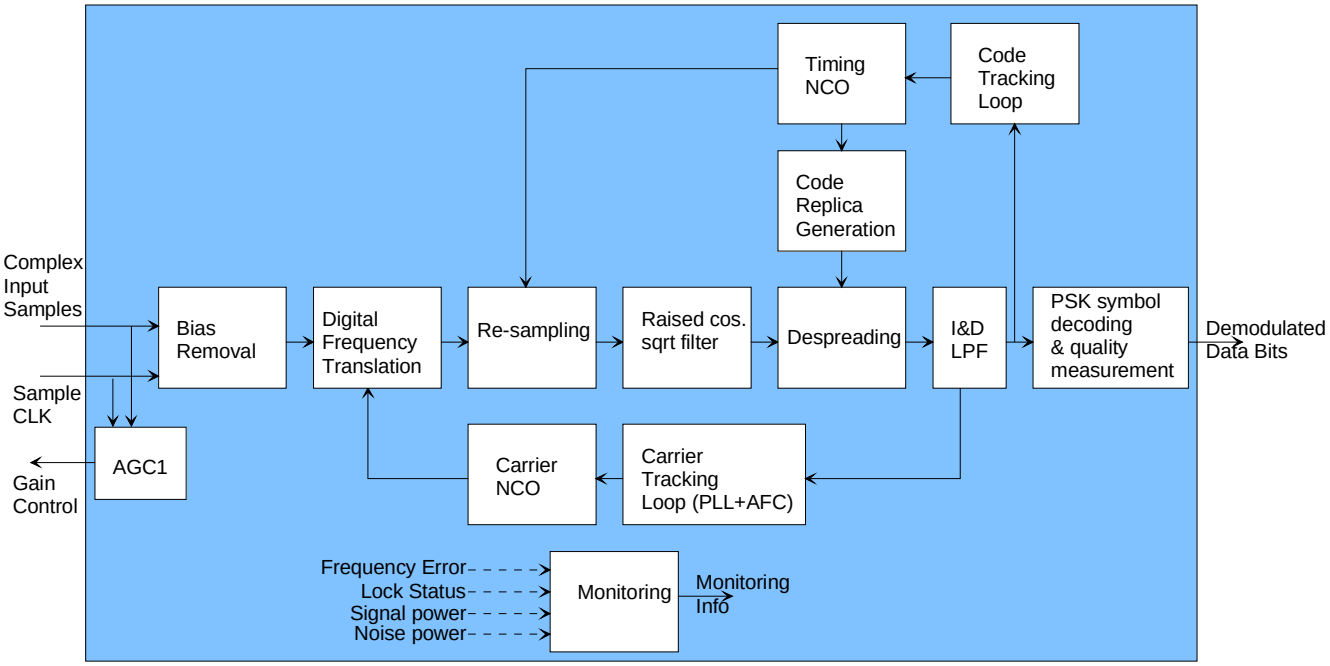
 Issued 9/26/2009

Block Diagram



Input Interface (J5)	Definition
DATA_I_IN[11:0]	Modulated input signal, real axis. 12-bit precision unsigned. Unused LSBs are pulled low. LVTTL 0 – 3.3V
DATA_Q_IN[11:0]	Modulated input signal, imaginary axis. Same format as DATA_I_IN.
SAMPLE_CLK_IN	Input signal sampling clock. One CLK-wide pulse. Read the input signal at the rising edge of CLK when SAMPLE_CLK_IN = '1'. Samples can be consecutive. Signal is pulled-up. LVTTL 0 – 3.3V
AGC1_OUT	Output. When this demodulator is connected directly to an analog receiver, it generates an analog signal to control the gain prior to A/D conversion. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3V is the minimum gain.
CLK_IN	Input reference clock for synchronous I/O. DATA_x_IN and SAMPLE_CLK_IN are read at the rising edge of CLK_IN. Maximum 90 MHz.

Demodulated Output (J8)	Definition
DATA_I_OUT[3:0]	4-bit soft-quantized demodulated bits, real axis. Unsigned representation: 0000 for maximum amplitude '0', 1111 for maximum amplitude '1'. When the serial output mode is selected, I and Q samples are transmitted one after another on this interface. I is transmitted before Q.
DATA_Q_OUT[3:0]	4-bit soft-quantized demodulated bits, imaginary axis. Same format as DATA_I_OUT. When the serial output mode is selected, this interface is unused.
SAMPLE_CLK_OUT	Demodulated bit clock. One CLK-wide pulse. Read the output signal at the rising edge of CLK when SAMPLE_CLK_OUT = '1'.
RX_LOCK	'1' when the demodulator is locked, '0' otherwise. The lock status is based on the code lock.
CLK_OUT	40 MHz output reference clock.

Monitoring Output (J9)	Definition
DESPREAD_I[9:0]	Output I-channel signal after channel filtering, despreading, integrate and dump. 10-bit precision unsigned. Can drive a COM-2001 dual D/A converter. LVTTL 0 – 3.3V
DESPREAD_Q[9:0]	Q-channel. Same format as DESPREAD_I
DESPREAD_CLK	Output signal sampling clock. One CLK-wide pulse once per symbol. Read the output signal at the rising edge of CLK when DESPREAD_CLK = '1'.
CLK_P	90 MHz output clock (internal processing clock).

Power Interface	4.75 – 5.25VDC. Terminal block. 250 mA typ.

Absolute Maximum Ratings

Supply voltage	-0.5V min, +6V max
40-pin connector inputs (when configured as LVTTL)	-0.5V min, +3.6V max

Important: I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- USB

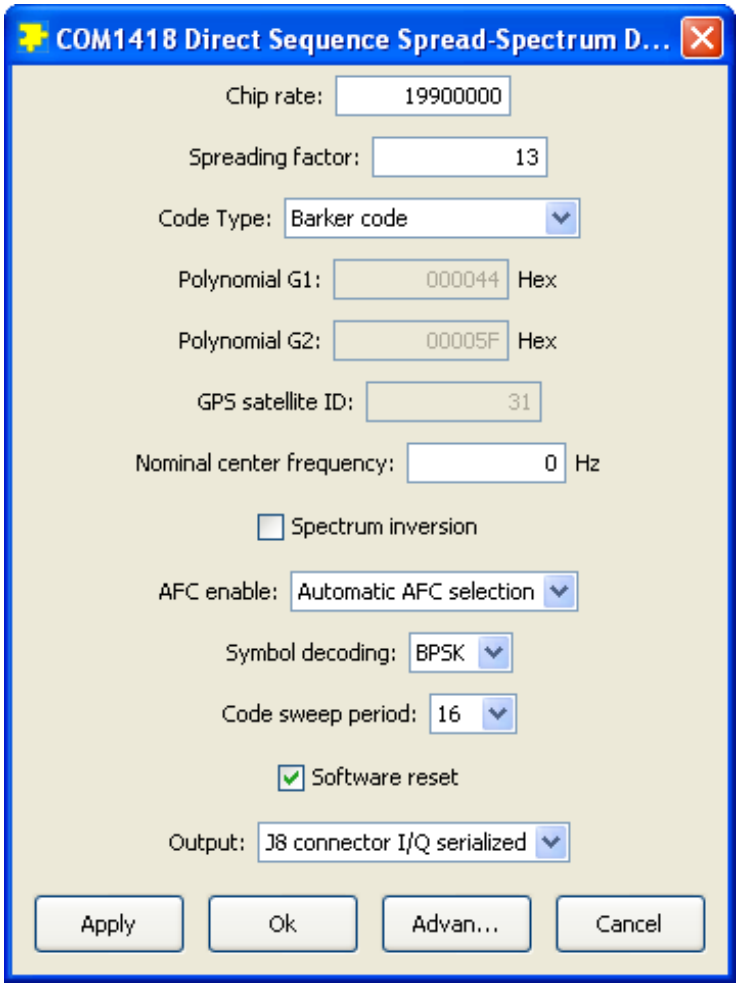
or connections via adjacent ComBlocks:

- USB
- TCP-IP/LAN,
- Asynchronous serial (DB9)
- PC Card (CardBus, PCMCIA).

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1418 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1418 module to be configured, next click the *Settings* button to display the *Settings* window shown below.



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

This module operates at a fixed internal clock rate $\mathbf{f_{clk}}$ of 90 MHz.

Parameters	Configuration
Chip rate (fchip rate)	32-bit integer expressed as fchip rate * 2^{32} / $\mathbf{f_{clk}}$. The maximum practical chip rate is 21.8 Mchips/s. Example: 1 Mchip/s is configured as 0x 2D82D82 The maximum allowed error between transmitted and received chip rate is +/- 100ppm. REG0 = bits 7-0 (LSB) REG1 = bits 15 – 8 REG2 = bits 23 – 16 REG3 = bits 31 – 24 (MSB)
Spreading factor (Processing gain, or code length))	Spreading code period Range: 3 – 2047 • When using Gold codes or maximal length sequences, it is important that this field be consistent with the G1 and G2 generator polynomials below. Length is always in the form 2^n-1, where n is an integer. • When using Barker codes, the spreading factor must be either 11 (0x0B) or 13 (0x0D). • Truncated codes can be generated by selecting a spreading factor other than the code length. REG4 bits 7-0 (LSB) REG5 bits 7-0 (MSB)
Code selection	001 = Gold code 010 = Maximal length sequence 011 = Barker code 100 = GPS C/A code REG6 bits 2-0
Gold sequence / Maximal Length Sequence generator polynomial G1	24-bit. Describes the taps in the linear feedback shift register 1: Bit 0 is the leftmost tap (2^0 in the polynomial). The largest non-zero bit is the polynomial order n. n determines the code period 2^n –1. Example: G1 = 1 + x + x^4 + x^5 + x^6 is represented as 0x000039 This field is used only if Gold code or Maximal length sequences are selected. REG7 = bits 7 – 0 REG8 = bits 15 – 8 REG9 = bits 23 – 16
Gold code generator polynomial G2	24-bit. Describes the taps in the linear feedback shift register 2: Same format as G1 above. This field is used only if Gold codes are selected. REG10 = bit 7 – 0 REG11 = bit 15 – 8 REG12 = bit 23 - 16
GPS satellite ID	GPS signals from different satellites are designated by a PRN signal number in the range 1 – 37. This field is used only if GPS C/A codes are selected. REG10 = bit 5 – 0
Nominal carrier center frequency ($\mathbf{f_c}$)	Nominal center frequency. This value is subtracted from the received signal actual center frequency. 32-bit signed integer expressed as $\mathbf{f_c}$ * 2^{32} / $\mathbf{f_{clk}}$. REG13 = bits 7 – 0 (LSB) REG14 = bits 15 – 8 REG15 = bits 23 – 16 REG16 = bits 31 – 24 (MSB)
Carrier frequency loop gain	00 = nominal 01 = 2x loop gain 10 = 4x loop gain 11 = 8x loop gain REG17 bits 3-2
Spectrum inversion	Invert Q bit. 0 = off 1 = on REG17 bit 5

AFC enable	The automatic frequency control circuit extendeds the frequency acquisition over +/- 10% of the symbol rate. When disabled, the receiver only means of carrier acquisition is the carrier frequency tracking loop which is inherently limited to approximately 1% of the symbol rate. The AFC should only be active during acquisition as it interferes with the Costas Loop operation. 00 = automatic AFC selection. 01 = force AFC disabled. Carrier tracking loop only 10 = force AFC enabled. 11 = reserved (test). REG17 bits 7-6
BPSK / QPSK decoding	00 = BPSK 01 = QPSK 1x = test mode. Forced code acquisition. REG18 bits 3-2
Code sweep period N_{lock}	Duration (in bits) of the search for a given code position during the code acquisition phase. This allows one to tradeoff acquisition time versus threshold SNR. 000 = 8 001 = 16 010 = 32 011 = 64 100 = 128 101 = 256 110 = 512 REG18 bits 6-4
Software reset	A one-time write of '1' forces all loops (code, carrier PLL, AFC) back into acquisition mode. This can be used to get out of a false lock condition. There is no need to clear this bit. REG18 bit 7.
Output selection	000 = J8 connector , 40 MHz clock. I/Q serialized when QPSK. 001 , J8 connector , 40 MHz clock, I/Q parallel 010 = USB, 1-bit hard quantized, packed into 8-bit bytes, MSb first. 011 = USB, 4-bit soft-quantized, packed into 8-bit bytes. REG19 bits 2-0
AGC response time	Users can to optimize AGC1 response time while avoiding instabilities (depends on external factors such as gain signal filtering at the RF front-end and chip rate). The AGC1_OUT analog gain control signal is updated as follows 0 = every chip, 1 = every 2 input chips, 2 = every 4 input chips, 3 = every 8 input chips, etc…. 20 = every 1 million input chips. 22 = every 4 million input chips. Valid range 0 to 22.
	The settings 16 = 0x10 is stable with most ComBlock analog/RF front-end receiver modules. REG20 bits 4-0

Status Registers

Digital status registers are read-only.

Parameters	Monitoring
Carrier frequency offset	Residual frequency offset with respect to the nominal carrier frequency. 32-bit signed integer expressed as fcdelta * * 2^{32} / f_{clk} SREG0 = bits 7 – 0 (LSB) SREG1 = bits 15 – 8 SREG2 = bits 23 – 16 SREG3 = bits 31 – 24 (MSB)
AGC1 gain	Front-end AGC1 gain settings 8 bit unsigned SREG4 bit 7-0.
Carrier Lock status	SREG5 bit 0 0 = unlocked 1 = locked
Code Lock status	SREG5 bit 1 0 = unlocked 1 = locked
Despread signal power S	Measured signal power (averaged over N_{lock} bits). Compute the signal to noise ratio after despreading as S/N. SREG6 = bits 7 – 0 (LSB) SREG7 = bits 15 – 8 SREG8 = bits 22 – 16 (MSB)
Noise power N	Measured noise power within the unspread symbol bandwidth (averaged over 512 symbols). SREG9 = bits 7 – 0 (LSB) SREG10 = bits 15 – 8 SREG11 = bits 22 – 16 (MSB)

ComScope Monitoring

Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-1418 signal traces and trigger are defined as follows:

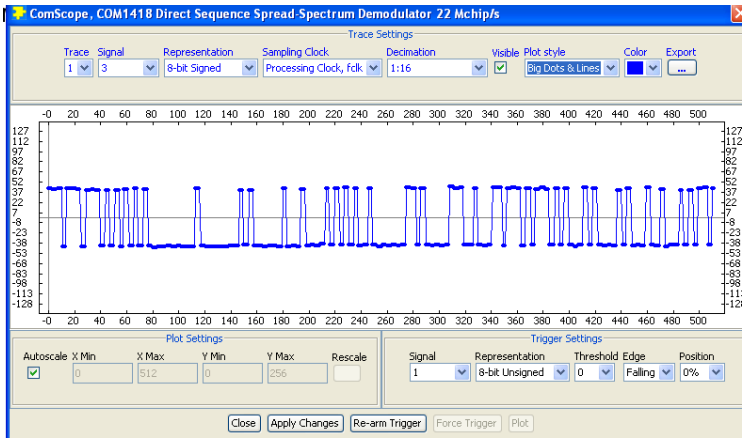
Trace 1 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Input I signal	8-bit signed.	Input sampling rate	512
2: spread I-channel after root raised cosine filter	8-bit signed	4 samples/chip	512
3: Despread I-channel, center, after I&D	8-bit signed	1 sample / symbol	512
4: code tracking phase correction (accumulated)	8-bit signed	1 sample / symbol	512
5: averaged despread signal power	8-bit signed	Once per code sweep period	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Input Q signal	8-bit signed	Input sampling rate	512
2: Code replica. Compare with spread input signals	8-bit signed	4 samples/chip	512
3: front-end AGC1	8-bit unsigned	AGC1 update rate	512
4: Carrier tracking phase	8-bit signed	4 samples/chip	512
5: averaged noise power (I only)	8-bit signed	Once per code sweep period	512
Trigger Signal	**Format**		
1: Start of code replica	Binary		
2. Code Lock	Binary		

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the $\mathbf{f_{clk}}$ processing clock as real-time sampling clock.

In particular, selecting the $\mathbf{f_{clk}}$ processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.

ComScope example, showing code lock with aligned: received spread signal after RRC filter (blue) vs code replica (red)



ComScope example: showing despread signal after integrate & dump.

Test Points (J6)

Test points are provided for easy access by an oscilloscope probe

Test Point	Definition
TP1	Carrier lock
TP2	Code lock (1) or scanning (0)
TP3	Recovered carrier
TP4	Recovered bit timing (i.e. start of code period). Useful to monitor code acquisition and tracking. Compare with modulator bit timing.
TP5	Spreading code replica
TP6	Spread I signal (MSB) (compare with spreading code replica above)
TP7	Demodulated data I-bit
TP8	Demodulated data Q-bit (when QPSK)
TP9	Start of spreading code replica (compare with start of spreading code at the modulator)
TP10	'1' when despread power is greater than detection (noise) threshold.

Implementation

Spreading codes

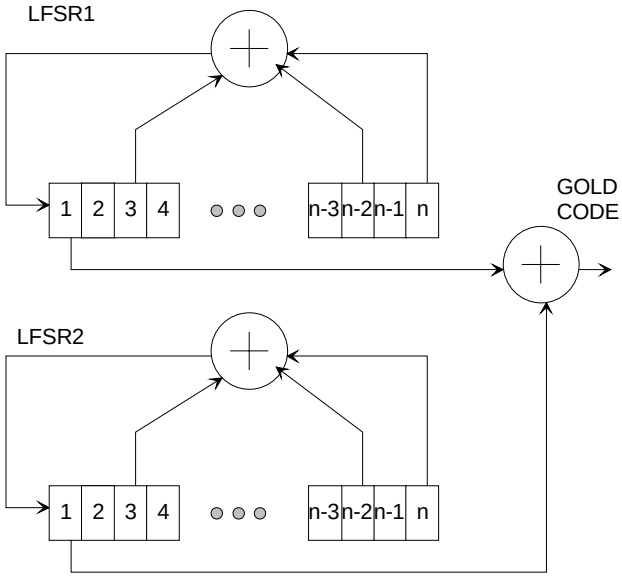
Spreading codes are pseudo random sequences which falls within the following categories:

- Gold sequences, for best autocorrelation properties
- Maximal length sequences
- Barker codes (length 11, 13)
- GPS C/A codes.

The same spreading code is used on both the in-phase (I) and quadrature (Q) channels.

Gold sequences

Gold sequences are generated using two linear feedback shift registers LFSR1 and LFSR2 as illustrated below:



The code period is 2^n-1, where n is the number of taps in the shift register. The LFRSa are initialized to all 1's at the start of each period. The LFRSs will generate all possible n-bit combinations, except the all zeros combination.

Each sequence is uniquely described by its two generator polynominals. The highest order is n. The generator polynominals are user programmable.

A few commonly used Gold sequences are listed below:

n = 5 (length 31):
G1 = $1 + x^2 + x^5$ (0x000012)
G2 = $1 + x + x^2 + x^4 + x^5$ (0x00001B)

n = 6 (length 63):
G1 = $1 + x^5 + x^6$ (0x000030)
G2 = $1 + x + x^4 + x^5 + x^6$ (0x000039)

n = 7 (length 127):
G1 = $1 + x^3 + x^7$ (0x000044)
G2 = $1 + x + x^2 + x^3 + x^4 + x^5 + x^7$ (0x00005F)

n = 9 (length 511):
G1 = $1 + x^5 + x^9$ (0x000110)
G2 = $1 + x^3 + x^5 + x^6 + x^9$ (0x000134)

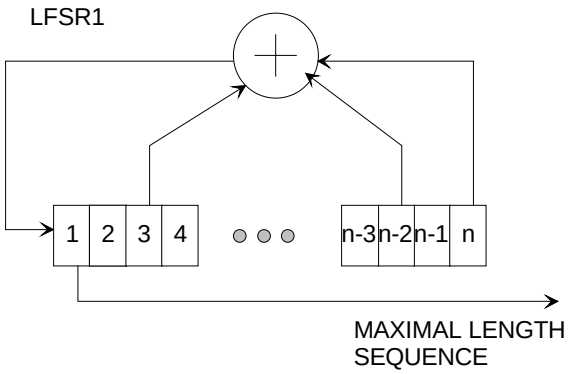
n = 10 (length 1023):
G1 = $1 + x^7 + x^{10}$ (0x000240)
G2 = $1 + x^2 + x^7 + x^8 + x^{10}$ (0x0002C2)

n = 11 (length 2047):
G1 = $1 + x^9 + x^{11}$ (0x000500)
G2 = $1 + x^3 + x^6 + x^9 + x^{11}$ (0x000524)

n = 17 (length 131071):
G1 = $1 + x^3 + x^6 + x^7 + x^9 + x^{10} + x^{14} + x^{16} + x^{17}$ (0x01A364)
G2 = $1 + x^9 + x^{13} + x^{14} + x^{17}$ (0x013100)

Maximal length sequences

Maximal length sequences are generated using one linear feedback shift register LFSR1 as shown below:



The code period is 2^n-1, where n is the number of taps in the shift register. The LFRSa are initialized to all 1's at the start of each period. The LFRSs will generate all possible n-bit combinations, except the all zeros combination.

Each sequence is uniquely described by its generator polynominal. The highest order is n. The generator polynominal is user programmable.

A few commonly used maximal length sequences are listed below:

n = 4 (length 15):
G1 = $1 + x + x^4$ (0x000009)
n = 5 (length 31):
G1 = $1 + x^2 + x^5$ (0x000012)
n = 6 (length 63):
G1 = $1 + x + x^6$ (0x000021)
n = 7 (length 127):
G1 = $1 + x + x^7$ (0x000041)
n = 8 (length 255):
G1 = $1 + x^2 + x^3 + x^4 + x^8$ (0x00008E)
n = 9 (length 511):
G1 = $1 + x^4 + x^9$ (0x000108)
n = 10 (length 1023):
G1 = $1 + x^3 + x^{10}$ (0x000204)

Barker Codes

11 bit Barker code: 101 1011 1000, or 0x5B8
13 bit Barker code: 1 1111 0011 0101, or 0x1F35

The length (11 or 13) must be entered as spreading factor in REG4/5.

GPS C/A Codes

GPS C/A codes are modified Gold codes of length 1023 with generator polynomials:
G1 = $1 + x^3 + x^{10}$
G2 = $1 + x^2 + x^3 + x^6 + x^8 + x^9 + x^{10}$

The G2 generator output is slightly modified so as to create a distinct code for each satellite. The G2 output is generated by summing two specific taps of the shift register. In the case of Satellite ID 1 for example, taps 2 and 6 are summed.

The G2 output taps are listed below:

Satellite ID / GPS PRN Signal Number	G2 output taps selection	Satellite ID / GPS PRN Signal Number	G2 output taps selection
1	2 xor 6	21	5 xor 8
2	3 xor 7	22	6 xor 9
3	4 xor 8	23	1 xor 3
4	5 xor 9	24	4 xor 6

5	1 xor 9	25	5 xor 7
6	2 xor 10	26	6 xor 8
7	1 xor 8	27	7 xor 9
8	2 xor 9	28	8 xor 10
9	3 xor 10	29	1 xor 6
10	2 xor 3	30	2 xor 7
11	3 xor 4	31	3 xor 8
12	5 xor 6	32	4 xor 9
13	6 xor 7	33	5 xor 10
14	7 xor 8	34	4 xor 10
15	8 xor 9	35	1 xor 7
16	9 xor 10	36	2 xor 8
17	1 xor 4	37	4 xor 10
18	2 xor 5		
19	3 xor 6		
20	4 xor 7		

Compliant with “Navstar GPS Space Segment / Navigation User Interfaces” specifications, ICD-GPS-200, Revision C. IRN-200C-004, 12 April 2000.

Data Rate

The data rate is determined by the chip rate, the processing gain (i.e. the spreading code period) and the modulation (BPSK/QPSK).
For a QPSK modulated signal, the data rate is
2 *fchip rate / processing gain

Filter Response

This module is configured at installation with a 40% rolloff filter. The filter rolloff can be selected among 20%, 25%, 35% and 40%. Changing the rolloff selection requires loading the firmware once using the ComBlock control center, then switching between up to four stored firmware versions (it takes 0.5 seconds).

All firmware versions can be downloaded from www.comblock.com/download.

COM-1418-**A** DSSS demodulator 20% rolloff

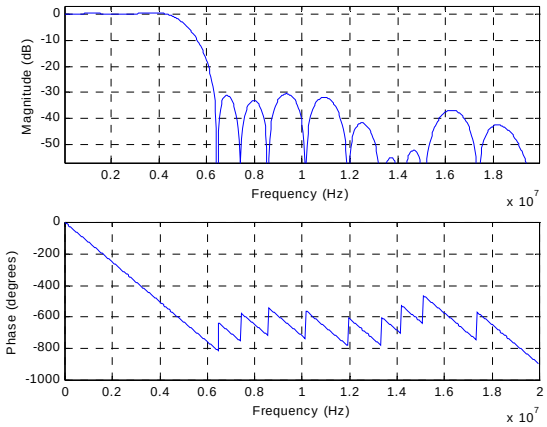
COM-1418-**B** DSSS demodulator 25% rolloff

COM-1418-**D** DSSS demodulator 35% rolloff

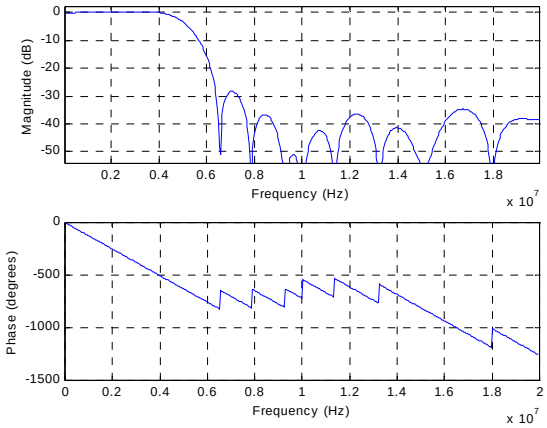
COM-1418-**E** DSSS demodulator 40% rolloff

To verify which firmware is currently installed, open the settings window and click on the “Advanced” button. The firmware option is listed at the bottom of the advanced settings window.

Filter Response (-A 20% rolloff)

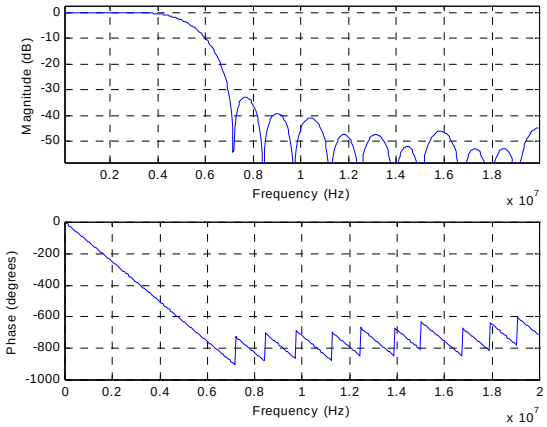


Filter Response (-B 25% rolloff)



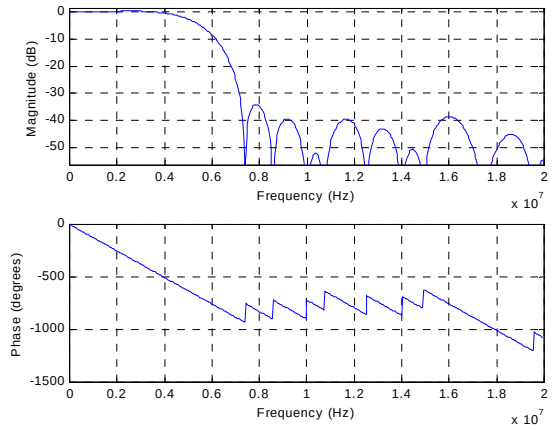
*(filter response normalized for 4*symbol rate = 40 MHz)*

Filter Response (-D 35% rolloff)

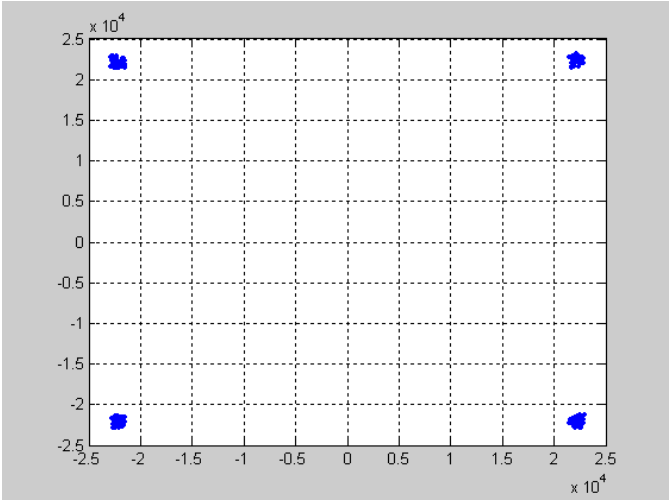


*(filter response normalized for 4*symbol rate = 40 MHz)*

Filter Response (-E 40% rolloff)



*(filter response normalized for 4*symbol rate = 40 MHz)*



I/Q constellation at the center of a spreading chip. Captured at the demodulator raised cosine square root filter output. QPSK. 40% rolloff. (digital modulator-demodulator back to back).

Frequency Tracking

The demodulator comprises both a phase locked loop (PLL) and an Automatic Frequency Control (AFC) loop. The AFC is to quickly detect and compensate for carrier frequency offsets, generally around the time of the code acquisition. The PLL is to detect and compensate for carrier phase errors.

The PLL is a second order loop. It can track the center frequency over a wide frequency range. The digital implementation of the Costas PLL has a small frequency acquisition range of about ±1% of the despread symbol rate.

The main purpose of the AFC is to increase the frequency acquisition window to about ±10% of the despread symbol rate (typical). Once acquisition is achieved, the AFC is automatically disabled.

If the unknown received carrier frequency uncertainty is larger, the user must program some search algorithm using the nominal center frequency control registers (REG13 through 16).

For high data rates (> 100 Kbps), carrier phase noise is generally negligible. For lower data rates, it is may be necessary to adjust the carrier tracking loop gain as a tradeoff between carrier phase noise (originating at the modulator, up-converter, down-converter, etc) and thermal noise. To this effect, the user is given control of the loop gain over a range of x1, x2, x4 and x8.

The higher loop gain can also be used temporarily during acquisition to increase the frequency acquisition window from approximately 1% to 3% of the symbol rate. However, use of the AFC is preferred because of the faster acquisition time and larger acquisition range.

In some conditions, such as no input signal, the AFC and PLL loops can drift out and inhibit (re-)acquisition. It is possible for the user to reset the accumulators within the AFC and PLL loops by writing a '1' in REG18 bit7.

Code Tracking Loop

The code tracking loop is a coherent delay lock loop (DLL) of the 1st order.

Code Acquisition

When code lock is not detected for N_{lock} consecutive bits, the receiver goes into code acquisition mode. The code replica is swept until code lock is detected (sequential code search). The rate at which the code replica is scanned is one chip every N_{lock} bits. The search stops as soon as code lock is detected. The parameter N_{lock} is user-defined.

Input Interpolation

This module provides fine selection of symbol rates, as long as the input sampling rate is between x4 and x8 the symbol rate. For higher ratios between input sampling rate / symbol rate, the COM-1008 variable decimation filter is recommended to prevent aliasing.

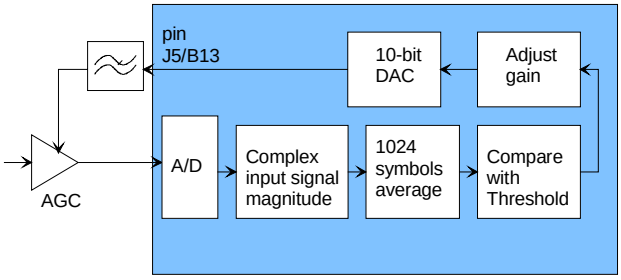
Front-End AGC1

The purpose of this AGC is to prevent saturation at the input signal A/D converters while making full use of the A/D converters dynamic range. Therefore, AGC1 reacts to the composite input signal which may comprise not only the useful signal but also adjacent channel interferers and noise. The principle of operations is outlined below:

(a) The magnitude of the complex input samples is computed and continuously averaged over 1024 symbols.

(b) The average magnitude is compared with a target magnitude threshold and the AGC gain is adjusted accordingly.

(c) A 10-bit D/A converter generates the analog gain control signal RX_AGC1 for use by the external variable gain amplifiers. (pin J5/B13, left connector)



AGC1 principle (analog output)

Troubleshooting Checklist

Demodulator can't achieve lock even at high signal-to-noise ratios:

- Make sure the modulator baseband I/Q signals do not saturate, as such saturation would strongly distort the modulation phase information. (this is a phase demodulator!)

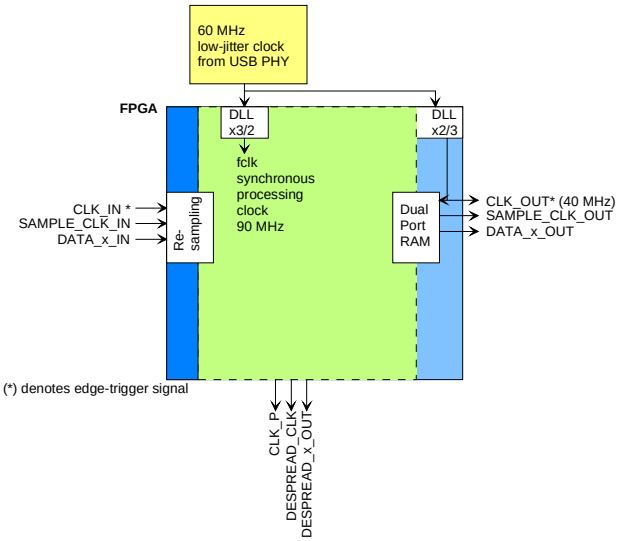
Demodulator can demodulate BPSK but not QPSK:

- A spectrum inversion may have occurred in the RF transmission chain. If so, invert the spectrum inversion flag at the demodulator.

Timing

Clocks

The clock distribution scheme embodied in the COM-1418 is illustrated below.

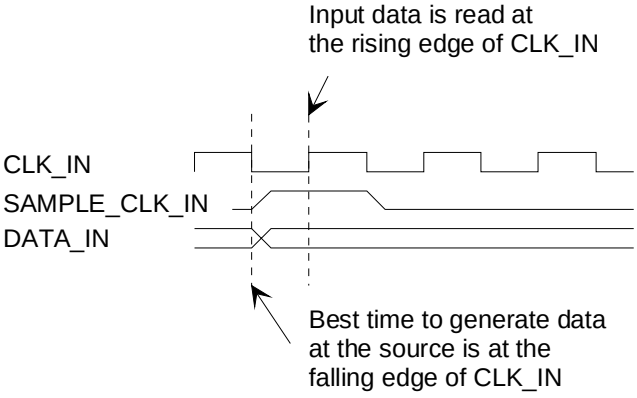


The COM-1418 generates an internal 90 MHz processing clock based on the 60 MHz reference from the USB PHY.

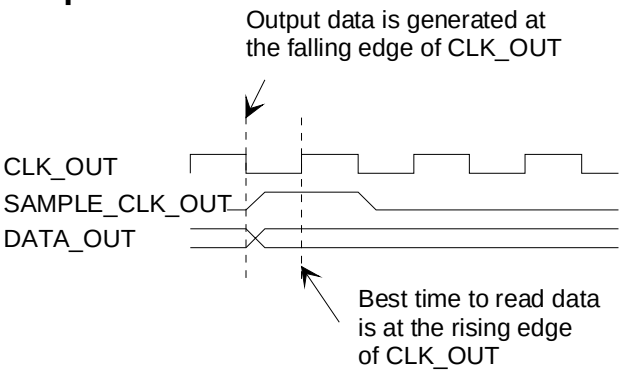
The input signal is reclocked with this 90 MHz processing clock. The input signal synchronous clock CLK_IN can be as high as 90 MHz.

All I/O signals are synchronous with the rising edge of a reference clock (i.e. the signals are stable around the rising edge of the associated reference clock).

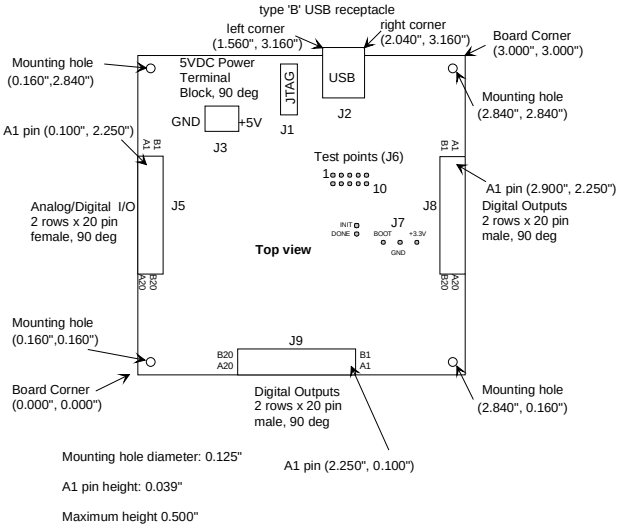
Input



Output



Mechanical Interface



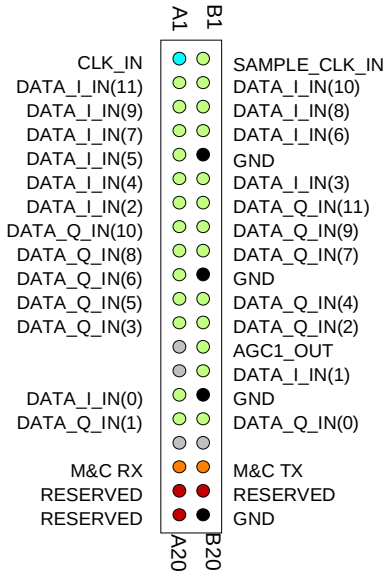
The front dimensions (plug face) of a type ‘B’ USB receptacle are 12 mm wide by 11 mm tall (above the board.)

Schematics

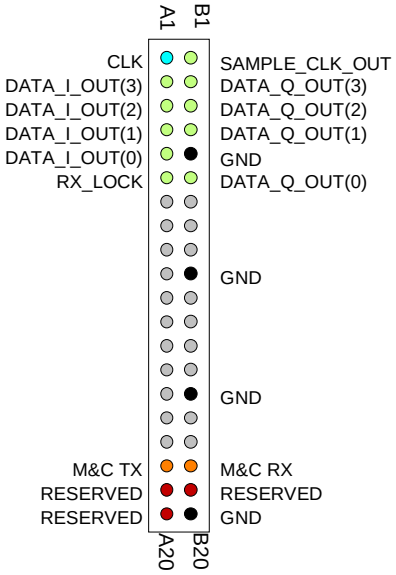
The board schematics are available on-line at ComBlock.com/download/com_1400schematics.zip

Pinout

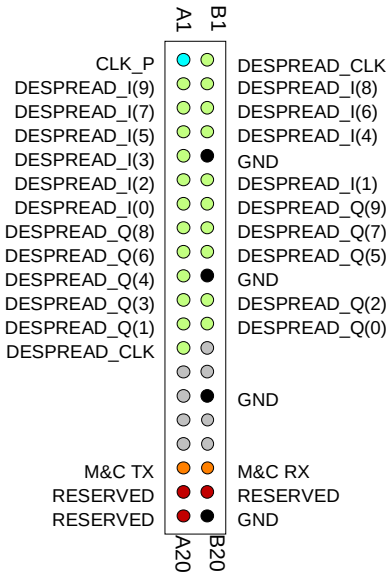
Input Connector J5



Output Connector J8



Output Connector J9



I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-300x RF receivers	COM-1005 Bit Error Rate Measurement
COM-1008 variable decimation	COM-7001 Turbo code decoder
COM-1012/1019 spread spectrum modulators (back to back)	COM-1009 Convolutional decoder K=7
COM-1023 BER generator, AWGN generator	COM-1209 LDPC + long BCH error correction decoder
COM-1024 Multipath simulator.	COM-5003 TCP-IP / USB Gateway

Configuration Management

This specification is to be used in conjunction with VHDL software revision 2.

It is possible to read back the option and version of the FPGA configuration currently active. Using the ComBlock Control Center, highlight the COM-1418 module, then go to the advanced settings. The option and version are listed at the bottom of the configuration panel.

Comparison with Previous ComBlocks

Key Improvements with respect to COM-1018 Direct-Sequence Spead-Spectrum Demodulator
- False code-lock prevention. - Support for truncated codes. - USB 2.0 high-speed output to send demodulated bits to a host computer. - Available despread-output, interface ready for D/A conversion (COM-2001 compatible) - Maximum input sampling rate increased from 40 Msamples to 90 Msamples/s. - Analog gain control for faster response (versus previous slower pulse-width modulated digital output) - True automatic frequency control to increase the frequency acquisition range (to +/- 10% of the symbol rate) during acquisition. - 32-bit numerically controlled oscillators for carrier and symbol timing (versus 24-bit) - Significant increase in center frequency tuning range - Added input bias removal

ComBlock Ordering Information

COM-1418 Direct sequence spread-spectrum demodulator. 22 Mchip/s.

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