COM-1505
INTEGRATED PSK MODEM

Overview

The COM-1505 is a complete digital PSK modem, including PSK modulation, demodulation, convolutional error correction, V.35 scrambling, HDLC framing, TCP-IP network interface and USB 2.0 interface.

Key features and performance:

- PSK (BPSK, QPSK, OQPSK) modulation
- Continuous mode operation (i.e. Burst mode is not supported)
- Convolution error correction, rates 1/2, 2/3, 3/4, 5/6 and 7/8.
- Overall performance: 2.10^{-5} BER @ 4dB Eb/No for K=7 rate ½ FEC.
- Serial HDLC to transmit empty frames over the synchronous link when no payload data is available.
- V.35 scrambling to randomize the modulated data stream.
- Maximum encoded data rate of 25 Msymbols/s.
- User interfaces:
  - Synchronous serial with elastic buffer or
  - GbE TCP-IP server
  - USB 2.0 FS/HS
- Demodulator performance:
  - BER: < 0.5 dB implementation losses w.r.t. theory
  - Programmable frequency acquisition range.
  - Demodulator acquisition threshold (uncoded) Eb/No = 1dB
- Includes test signal generation and bit error rate measurement.
- Monitoring:
  - Receiver lock
  - Carrier frequency error
  - SNR
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Connectorized 3”x 3” module for ease of prototyping. Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.

For the latest data sheet, please refer to the **ComBlock** web site: http://www.comblock.com/download/com1505.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

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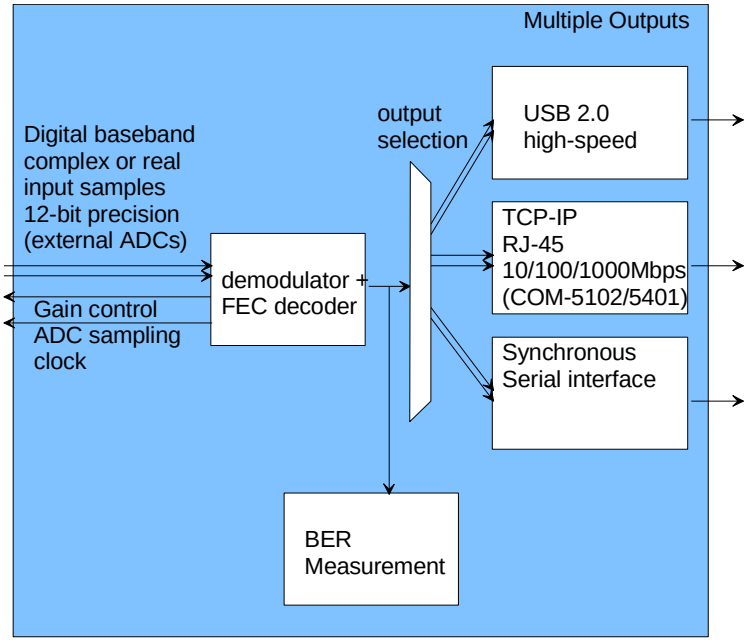
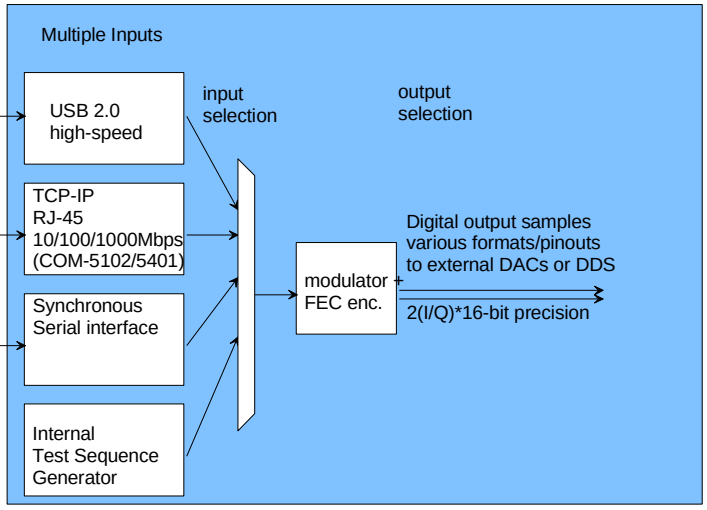
Overall Block Diagrams



Demodulator connectivity



Modulator connectivity

Option	Definition
-A	LAN (TCP-IP) and USB data interface. Left (J6) connector: GbE LAN adapter interface (compatible with COM-5102 adapters) Right (J9) connector: analog baseband I/O. (compatible with COM-3504 dual Analog<->Digital conversion)
-B	synchronous serial (clk + data + cts) and USB interfaces Left (J6) synchronous serial interface Right (J9) connector: analog baseband I/O. (compatible with COM-3504 dual Analog<->Digital conversion)
-C	synchronous serial (clk + data + cts) and USB interfaces. No HDLC. Left (J6) synchronous serial interface Right (J9) connector: analog baseband I/O. (compatible with COM-3504 dual Analog<->Digital conversion)

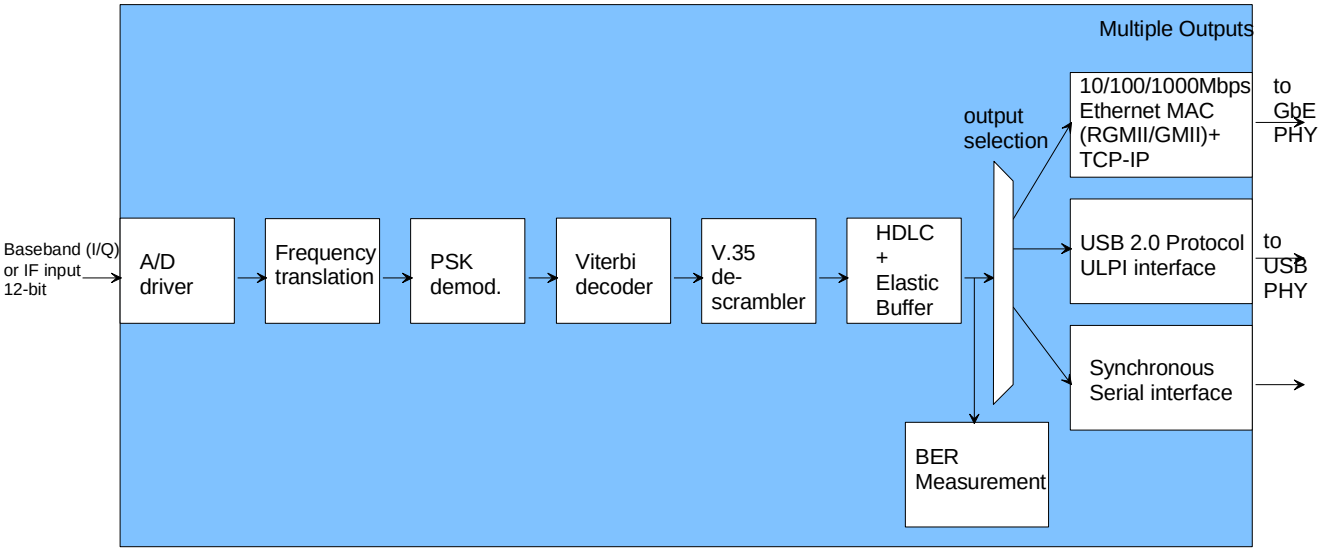
Options

Several interface types are supported through multiple firmware options. All firmware versions can be downloaded from

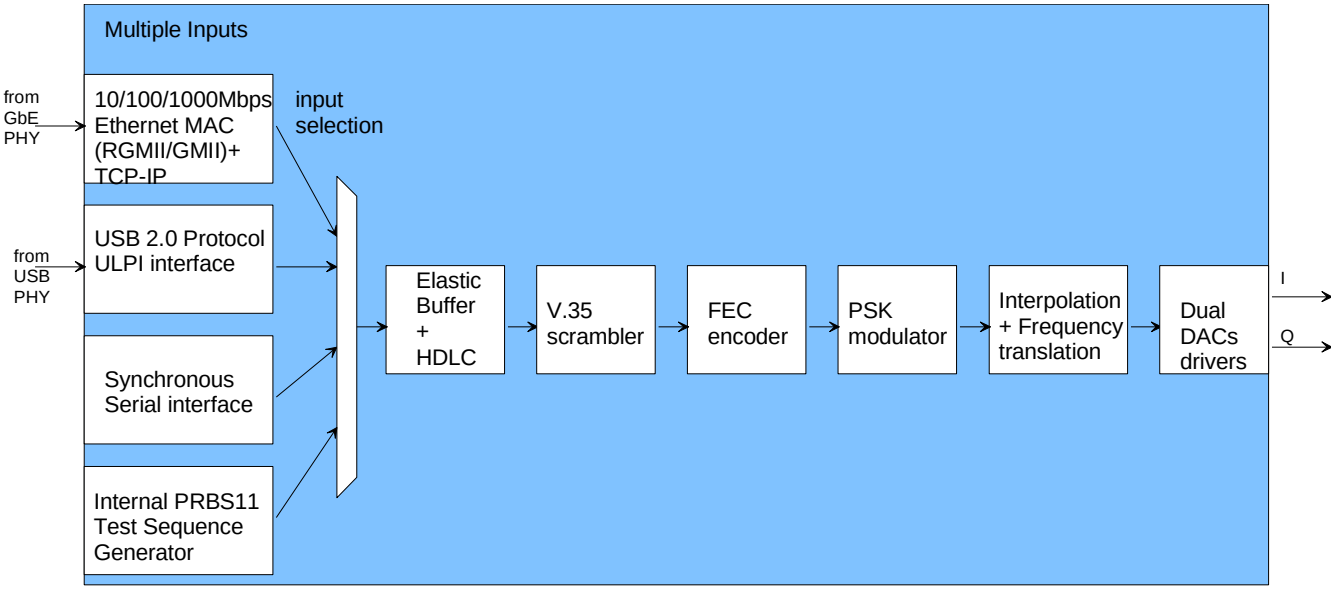
http://www.comblock.com/download.html

Changing the firmware option requires loading the firmware once using the ComBlock control center, then switching between the stored firmware versions The selected firmware option is automatically reloaded at power up or upon software command within 1.2 seconds

Implementation Block Diagram



Receiver



Transmitter

Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

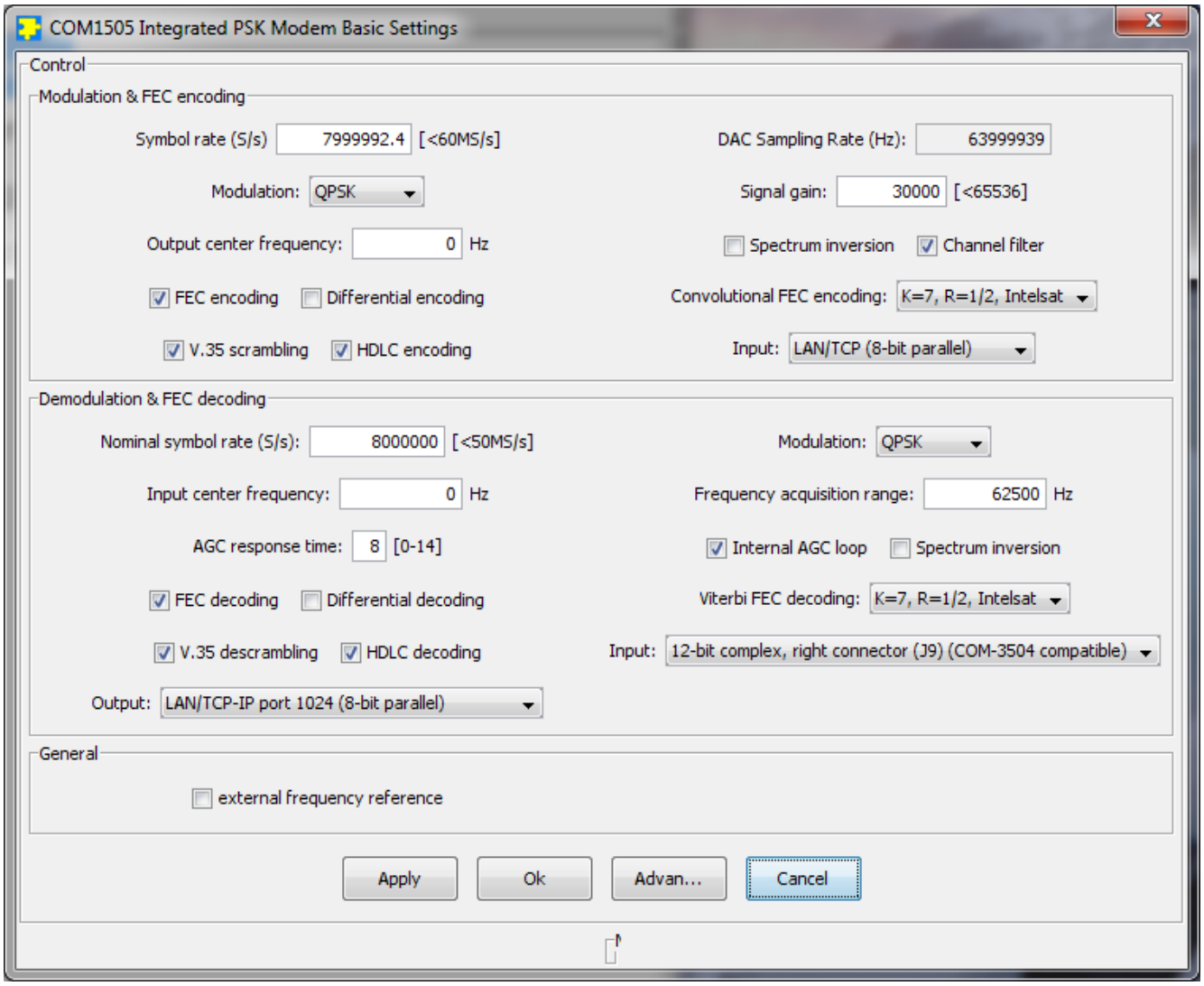
- USB, TCP-IP/LAN, Asynchronous serial (LVTTL),

or connections via adjacent ComBlocks.

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1505 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1505 module to be configured, next click the *Settings* button to display the *Settings* window shown below.



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write. Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

Transmitter	
Parameters	**Configuration**
Input selection / format, test modes	Select the origin of the transmitter input data stream. 0 = high-speed USB, 8-bit parallel 1 = LAN/TCP-IP, port 1024 (through Ethernet adapter), 8-bit parallel 2 = 1-bit synchronous serial 3 = internal PRBS-11 test sequence 5 = unmodulated carrier 8-bit parallel input bytes are transmitted MSb first. REG5(3:0)

FEC convolutional encoder	
Parameters	**Configuration**
Constraint length K and rate R	0001 = (K = 7, R=1/2, Intelsat) 0010 = (K = 7, R=2/3, Intelsat) 0011 = (K = 7, R=3/4, Intelsat) 0100 = (K = 7, R=5/6, Intelsat) 0101 = (K = 7, R=7/8, Intelsat) REG12(4:1)
Differential Encoding	Differential encoding is useful in removing phase ambiguities at the PSK demodulator, at the expense of doubling the bit error rate. When enabled, the differential decoding must be enabled at the receiving end. There is no need to use the differential encoding to remove phase ambiguities at the PSK demodulator when the Viterbi decoder and HDLC decoder are enabled. 0 = disabled 1 = enabled REG12(5)
Bypass FEC encoding	0 = encoding enabled 1 = bypass REG12(6)
V.35/Intelsat IESS 308 scrambling before FEC encoding	0 = enabled 1 = bypass REG12(7)
HDLC encoding	0 = enabled 1 = bypass REG12(0)
PSK Modulator	
Parameters	**Configuration**
Processing clock f_{clk_tx}	Modulator processing clock. Also serves as DAC sampling clock. 20-bit unsigned integer expressed as $f_{clk\_tx} * 2^{20}$ / 300MHz. 120 MHz maximum. 20 MHz recommended minimum REG0 = bits 7-0 (LSB) REG1 = bits 15 – 8 (MSB) REG2(3:0) = bits 19 – 16 (MSB)

Internal/External frequency reference	0 = internal. Use the internal 60 MHz clock (from the USB PHY) as frequency reference. 1 = external. Use the 10 MHz clock externally supplied through the J7 SMA connector as frequency reference. REG2(7)
Symbol rate $\mathbf{f_{symbol\ rate\ tx}}$	The modulator symbol rate is in the form $\mathbf{f_{symbol\ rate\ tx}} = \mathbf{f_{clk\_tx}} / 2^n$ where n ranges from 1 ($\mathbf{f_{clk\_tx}}$ is twice the symbol rate) to 15 (symbol rate = $\mathbf{f_{clk\_tx}}$ / 65536). n is defined in REG3(3:0)
Modulation type	0 = BPSK 1 = QPSK 2 = OQPSK REG4(5:0)
Spectrum inversion	Invert Q bit. This is helpful in compensating any frequency spectrum inversion occurring in a subsequent RF frequency translation. 0 = off 1 = on REG4(6)
Channel filter enabled	0 = enable the spectrum shaping filters (root raised cosine, interpolation) 1 = bypass the spectrum shaping filters. (special use in applications when a root raised cosine filter is not used in the demodulator.) REG4(7)
Signal gain	Signal level. 16-bit unsigned integer. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Therefore, we recommend checking for saturation at the D/A converter when changing either the symbol rate or the signal gain. REG6 = bits 7-0 (LSB) REG7= bits 15-8 (MSB)

Output Center frequency (f_{cout})	Frequency translation. 32-bit signed integer (2's complement representation) expressed as $f_{cout} * 2^{32} / \mathbf{f_{clk\_tx}}$ REG8 = bits 7-0 (LSB) REG9 = bits 15 – 8 REG10 = bits 23 – 16 REG11 = bits 31 – 23 (MSB)
Input bit rate	Option **-C** only Set the nominal input bit rate in order to generate a regular bit clock to the data source. Must be consistent with the modulator symbol rate, modulation type and FEC rate. Example: 2 Mbps : x051EB852 $\mathbf{f_{input\ bit\ rate\ tx}} * 2^{32} / \mathbf{f_{clk\_rx}}$ REG13 = bits 7-0 (LSB) REG14 = bits 15 – 8 REG15 = bit 23 – 16 REG16 = bit 31 – 23 (MSB)
External transmitter gain control	When using an external transceiver such as the COM-350x family, the transmitter gain can be controlled through the TX_GAIN_CNTRL1 analog output signal. Range 0 – 3.3V. REG17 = bits 7-0 (LSB) REG18(3:0) = bits 11-8
External transmitter controls	REG19(0): TX_ENB REG19(1) = RX_TXN

Receiver	
PSK Demodulator	
Parameters	**Configuration**
Processing clock	The demodulator processing clock also serves as A/D converter sampling clock. It can be generated within the FPGA or externally. Code baseline f_{clk_rx} = 100 MHz Note: when using IF undersampling, a dedicated oscillator is recommended as the FPGA-generated clock may show excessive jitter (which translates into phase noise).
Nominal symbol rate $f_{symbol\ rate\ rx}$	The demodulator nominal symbol rate is in the form $f_{symbol\ rate\ rx} * 2^{32} / f_{clk\_rx}$ REG25 = bits 7-0 (LSB) REG26 = bits 15 – 8 REG27 = bit 23 – 16 REG28 = bit 31 – 23 (MSB)
Nominal Center frequency (f_{c_rx})	Expected center frequency of the received signal. 32-bit signed integer (2's complement representation) expressed as $f_{c\_rx} * 2^{32} / f_{clk\_rx}$. In the case of IF undersampling, the residual intermediate frequency is removed here. For example, in the case of a 125 MHz IF signal sampled at 100 Msamples/s, the 25 MHz residual frequency is removed here by entering 0x40000000. REG29 = bit 7-0 (LSB) REG30 = bit 15 – 8 REG31 = bit 23 – 16 REG32 = bit 31 – 23 (MSB)
Modulation type	0 = BPSK 1 = QPSK 2 = OQPSK REG33(5:0)
Spectrum inversion	Invert Q bit. This is helpful in compensating any frequency spectrum inversion occurring during RF frequency translations. 0 = off 1 = on REG33(6)
High SNR	To minimize the false lock probability at high SNR, set this bit to '1' when Eb/No is likely to exceed 10dB. To emphasize operation at very low Eb/No, set this bit to '0' REG33(7)
Frequency acquisition range (scan)	The demodulator natural frequency acquisition range is around 1% of the symbol range (depending on modulation, SNR). The frequency acquisition range can be extended by frequency scanning. Scanning steps are spaced ($f_{symbol\ rate\ rx}$ /128) apart. The user can thus trade-off acquisition time versus frequency acquisition range by specifying the number of scanning steps here. For example, 16 steps yield a frequency acquisition range of +/-($f_{symbol\ rate\ rx}$ *12.5%) REG24
AGC response time	Users can to optimize the AGC response time while avoiding instabilities (depends on external factors such as gain signal filtering at the RF front-end and symbol rate). The response time is approximately: 0 = 8 symbols, 1 = 16 symbols, 2 = 32 symbols, 3 = 64 symbols, etc…. 10 = every thousand symbols. Valid range 0 to 14. REG34(4:0)
AGC internal / external	0 = internal AGC 1 = external AGC When selecting internal AGC mode, the user is responsible for avoiding saturation at or prior to the A/D converter. The internal AGC maximum gain is 256 in amplitude (48 dB in power). Therefore, it is recommended to keep the input samples amplitude between

	maximum and maximum/256. In the input dynamic range is larger, please adjust the INTERNAL_AGC_005 process within *RECEIVER1.vhd*. REG34(7)
Input selection	0 = digital real 12-bit unsigned samples, right connector, COM-3504 transceiver. Use in the case of IF input signal. 1 = digital complex 2*12-bit unsigned samples, right connector, COM-3504 transceiver.. Use in case of baseband (near-zero center frequency) input signal. 7 = internal loopback mode, from modulator. REG35(2:0)
Viterbi FEC decoder	
Parameters	**Configuration**
Constraint length K and rate R	0001 = (K = 7, R=1/2, Intelsat) 0010 = (K = 7, R=2/3, Intelsat) 0011 = (K = 7, R=3/4, Intelsat) 0100 = (K = 7, R=5/6, Intelsat) 0101 = (K = 7, R=7/8, Intelsat) REG37(4:1)
Differential Decoding	0 = disabled 1 = enabled REG37(5)
Bypass FEC decoding	0 = decoding enabled 1 = bypass REG37(6)
V.35/Intelsat IESS 308 descrambling after FEC decoding	0 = enabled 1 = bypass REG37(7)
HDLC decoding	0 = enabled 1 = bypass REG37(0)
Output selection	0 = high-speed USB, 8-bit parallel 1 = LAN/TCP-IP, port 1024 (through Ethernet adapter), 8-bit parallel 2 = 1-bit synchronous serial 3 = exclusively to the BER measurement REG36(2:0)
Enable test points	Enable (1)/Disable (0) test points on J6 connector REG36(7)

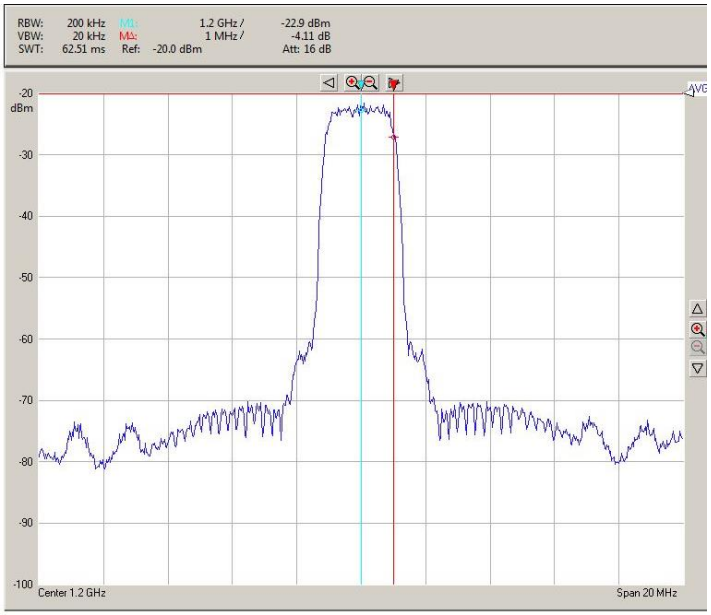
Network Interface	
Parameters	**Configuration**
IP address (when connected to Gbit Ethernet PHY like **COM-5102, COM-5104**)	4-byte IPv4 address. Example : 0x AC 10 01 80 designates address 172.16.1.128 The new address becomes effective immediately (no need to reset the ComBlock). REG41: MSB REG42 REG43 REG44: LSB

(Re-)Writing to the last control register REG44 is recommended after a configuration change to enact the change.

Configuration example

Modulator:

2 Msymbols/s modulation, BPSK, convolutional encoding K=7 R=1/2, PRBS-11 test sequence, baseband (0Hz) complex (I/Q) modulated output signal.



Typical RF output spectrum (after D/A conversion and direct RF modulation)

Status Registers

Digital status registers are read-only.

PSK/QAM/APSK Demodulator Monitoring	
Parameters	**Monitoring**
Front-end AGC	8-bit unsigned value prior to DAC conversion to RX_AGC1. Inverted scale: 0 is for the maximum gain. SREG10
Carrier frequency offset (fcdelta)	Residual frequency offset with respect to the nominal carrier frequency. 24-bit signed integer (2's complement) expressed as fcdelta * 2^{24} / f_{clk_rx}. SREG11 = LSB SREG12 SREG13 = MSB
Carrier tracking loop lock status	Lock is declared if the standard deviation of the phase error is less than 25deg rms. 0 = unlocked 1 = locked SREG14(0)
Inverse SNR	A measure of noise over signal power. 0 represents a noiseless signal. Valid only when demodulator is locked. SREG15
Viterbi FEC decoder monitoring	
Parameters	**Monitoring**
Synchronized	(FEC_DEC_LOCK_STATUS variable) Solid '1' when the Viterbi decoder is locked. '0' or toggling when unlocked. SREG14(1)
Decoder built-in BER	The Viterbi decoder computes the BER on the received (encoded) data stream irrespective of the transmitted bit stream. Encoded stream bit errors detected over a 1000-bit measurement window (unless modified in *com1509pkg.vhd*). SREG16 = bits 7 – 0 (LSB) SREG17 = bits 15 – 8 SREG18 = bits 23 – 16 (MSB)
HDLC decoder monitoring	
Parameters	**Monitoring**
Cumulative number of valid bits at HDLC output	SREG19: LSB SREG20: SREG21: SREG22: MSB
BER Measurement	
Parameters	**Monitoring**
Bit Errors	Bit errors can be counted when a PRBS-11 test sequence is transmitted. Number of bit errors in a 1,000,000 bit window. 32 bit unsigned. SREG23: error_count[7:0] (LSB) SREG24: error_count[15:8] SREG25: error_count[23:16] SREG26: error_count[31:24] (MSB) The bit errors counter is updated once every periodic measurement window. Reading the value will not reset the counter.
BER Synchronization status	0 = not synchronized. 2047-bit pattern is not detected. 1 = synchronized SREG27(0)
TCP-IP Connection Monitoring	
Parameters	**Monitoring**
TCP-IP connection on port 1024 (data stream)	Bit 0 = port 1028 (M&C) connected Bit 1 = port 1024 (data) connected 1 for connected, 0 otherwise SREG28(1:0)
LAN PHY ID	Expect 0x22 when the PHY IC is Micrel KSZ9021. SREG29(LSB)
MAC address	Unique 48-bit hardware address (802.3). In the form SREG30:SREG31:SREG32:…:SREG35 Since the MAC address is unique, it can also be used as a unique identifier in a radio network with many nodes.

Note: multi-words status registers such as frequency offset or BER, are latched upon reading status register SREG10.

Troubleshooting checklist

1. Place modem in loopback mode (REG35 = 0x07) while sending a PRBS-11 test sequence (REG5 = 0x03). Be sure to direct the demodulated bit stream to the BER measurement (REG36 = 0x03).

   Check the status registers for

a. Demodulator and Viterbi decoder are locked:
   SREG14 = 0x03
b. No Viterbi decoder errors:
   SREG16/17/18 = 0
c. BER measurement is synchronized:
   SREG27 = 0x01
d. No BER errors:
   SREG23/24/25/26 = 0
e. Bits are being received at the HDLC decoder output:
   SREG19/20/21/22 counter keeps increasing at a rate consistent with the modulation rate.

ComScope Monitoring 

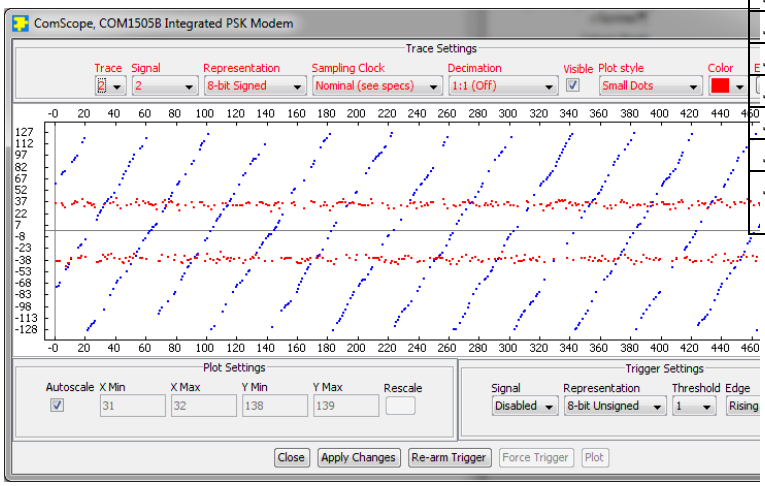
Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-1505 signal traces and trigger are defined as follows:

Trace 1 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Input signal (I-channel) after AGC, frequency translation, CIC decimation	8-bit signed	Input sampling rate/R	512
2: phase after scanning and before final carrier tracking loop	8-bit signed	1 sample / symbol	512
3: Magnitude after final AGC	8-bit signed	1 sample / symbol	512
4: symbol timing tracking correction (accumulated)	8-bit unsigned	1 sample / symbol	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Input signal (Q-channel) after AGC, frequency translation, CIC decimation	8-bit signed	Input sampling rate/R	512
2: Demodulated I channel	8-bit signed	1 sample / symbol	512
3: Input signal I-channel	8-bit signed	Input sampling rate	512
4: PLL Carrier tracking phase correction (accumulated)	8-bit signed	Input sampling rate	512
Trace 3 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Input signal Q-channel	8-bit signed	Input sampling rate	512
2: final AGC gain	8-bit signed	variable	512
Trigger Signal	**Format**		
N/A			

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk_rx} processing clock as real-time sampling clock.

In particular, selecting the $\mathbf{f_{clk\_rx}}$ processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope example: showing demodulated I-channel (red) and received phase after scanning/before tracking (blue)

Digital Test Points

Enabled if REG36(7) = '1', high-impedance otherwise.

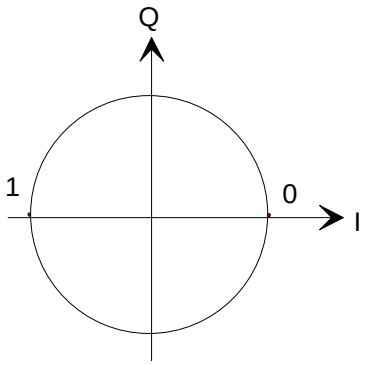
Test Point	Definition
J6/A29	Carrier locked
J6/A30	Recovered carrier: scanner
J6/A31	Recovered carrier: PLL
J6/A32	Overall demodulator lock (STATE=2)
J6/A33	Phase ambiguity removal step (pulse)
J6/A34	Reset demodulator in false lock (pulse)
J6/A35	Viterbi decoder locked
J6/A36	BER tester synchronized
J6/A37	Byte error detected by BER tester
J6/A38	BER tester detecting periodic start of PRBS-11 test sequence

Operation

Constellation: Symbol Mapping

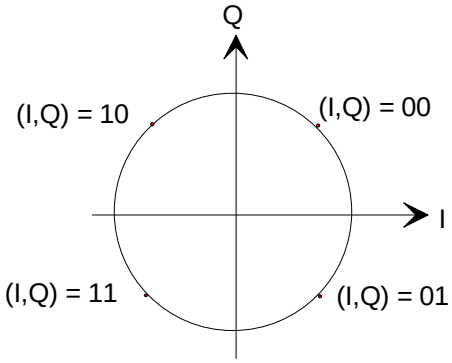
The packing of serial data stream into symbols is done with the Most Significant bit first.

BPSK



QPSK

Gray encoding.

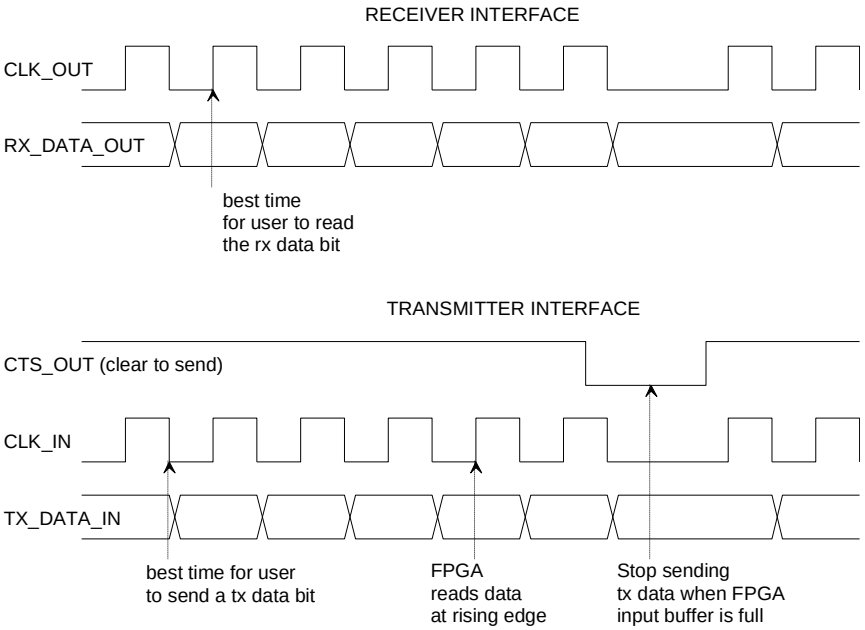


Recovery

This module is protected against corruption by an invalid FPGA configuration file (during firmware upgrade for example) or an invalid user configuration. To recover from such occurrence, connect a jumper in JP1 position 2-3 prior and during power-up. This prevents the FPGA configuration and restore communication. Once this is done, the user can safely re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center.

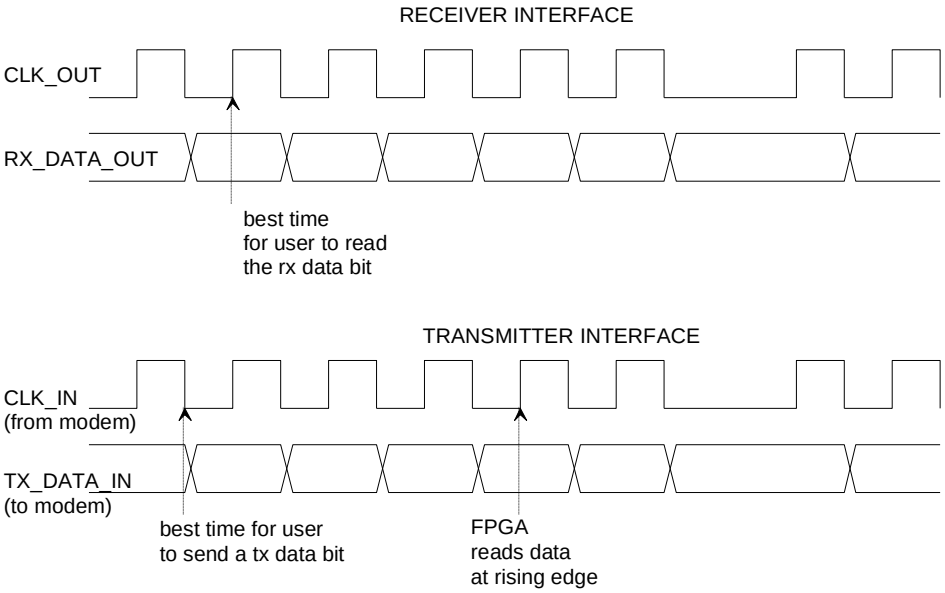
I/Os

1-bit synchronous serial (-B option)



In the transmit direction, the user provides both clock (CLK_IN) and data (TX_DATA_IN). The user should always check the "Clear-To-Send" CTS_OUT flag before sending additional data bits to the modulator. As option **–B** includes HDLC, the user is allowed not to transmit data. When so, the modem will send empty HDLC frames.

1-bit synchronous serial (-C option)



In the transmit direction, the user provides serial data (TX_DATA_IN), preferably at the falling edge of the modem-supplied CLK_IN. The TX_DATA_IN is read at the rising edge of CLK_IN. The user MUST provide data, otherwise an underflow condition will occur. Option **–C** is for continuous-mode operation. No gap in data

transmission is allowed.

TCP-IP (-A option)

The transmit and receive data streams can also be transferred over a TCP-IP network connection. This requires an additional Ethernet PHY with standard RGMII or GMII interface (a COM-5102 plug-in Ethernet adapter for example).

In this case, the modem acts as a TCP server, waiting for connection from a remote client at port 1024. A unique IP address and a unique MAC address must be assigned to the modem (see control registers REG41 through REG50).

The TCP-IP protocol guarantees that no overflow will occur in the user to modem direction. The built-in flow-control mechanism of the TCP-IP will prevent the user application from writing more data than the modem can handle for the specified data rate.

In the receiver to user direction however, it is the user's responsibility to read data as fast as possible to prevent an overflow condition from occurring at the receiver.

The TCP bytes are sent/received serially, most-significant bit first.

The modem monitoring and control information can also be sent over the same physical link, using the TCP server at port 1028.

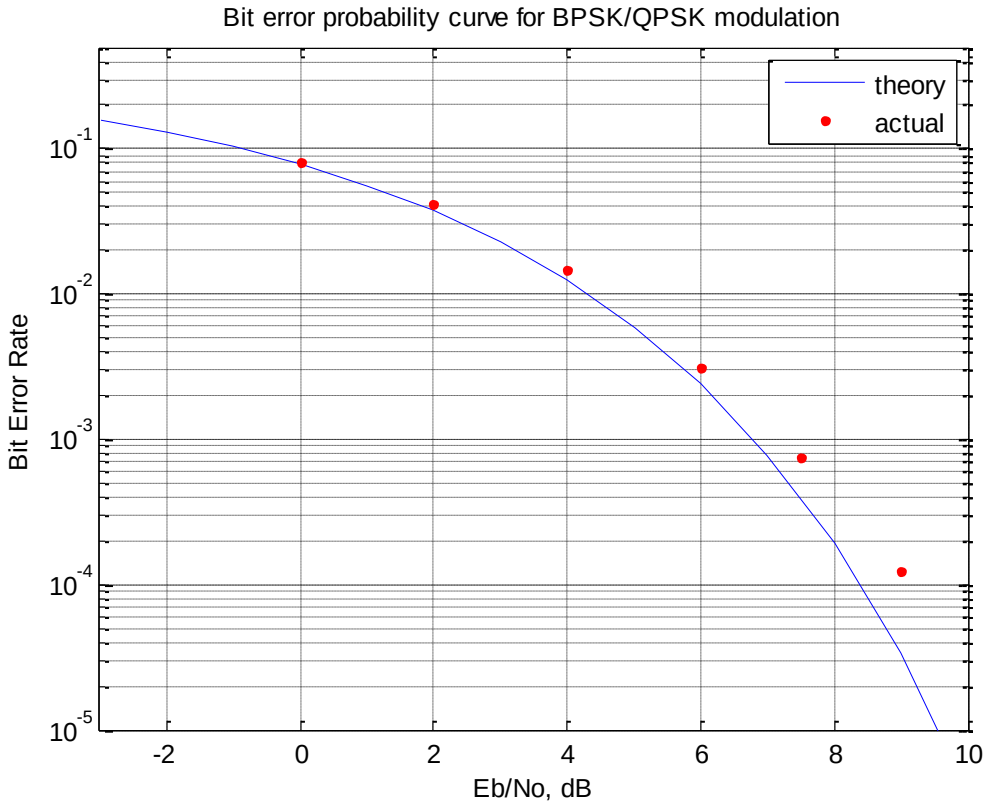
More information regarding the built-in 10/100/1000 Mbps Ethernet MAC and the TCP server can be found here:
www.comblock.com/download/com5401soft.pdf
www.comblock.com/download/com5402soft.pdf

USB

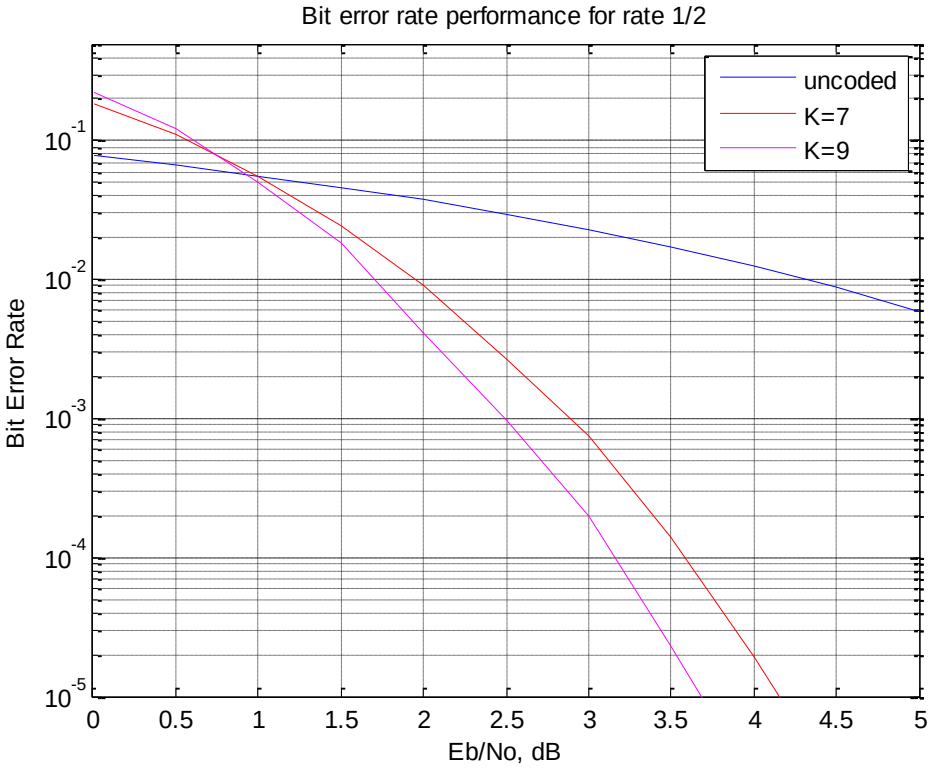
Data streams can also be transmitted over a USB 2.0 cable, together with monitoring and control information. This modem acts as a USB device.
See http://comblock.com/download/USB20_UserManual.pdf for details.

More information regarding the built-in USB 2.0 Serial Interface Engine (SIE) can be found here:
http://comblock.com/download/USB2soft.pdf

Performance



BER performance, demodulator only (no FEC)



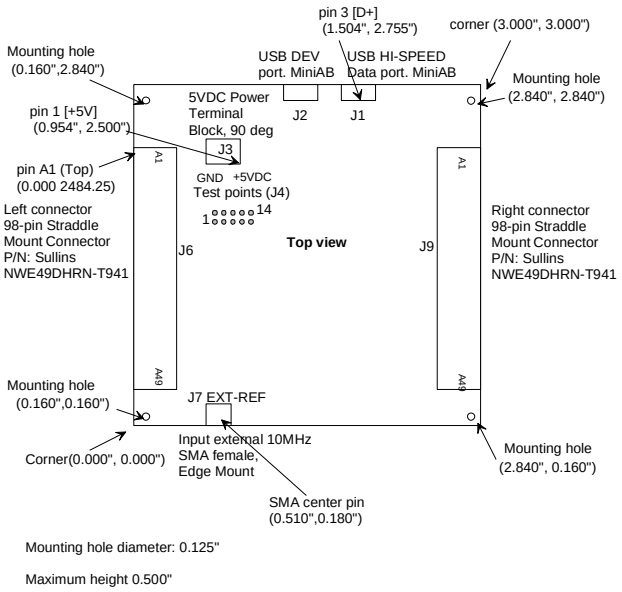
BER performance, FEC only (no demodulator)

Absolute Maximum Ratings

Supply voltage	-0.5V min, +6V max
40-pin connector inputs (when configured as LVTTL)	-0.5V min, +3.6V max

Important: I/O signals are 0-3.3V LVTTL.
Inputs are NOT 5V tolerant!

Mechanical Interface



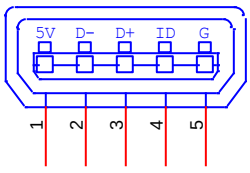
Schematics

The board schematics are available on-line at
http://comblock.com/download/com_1500schematics.pdf

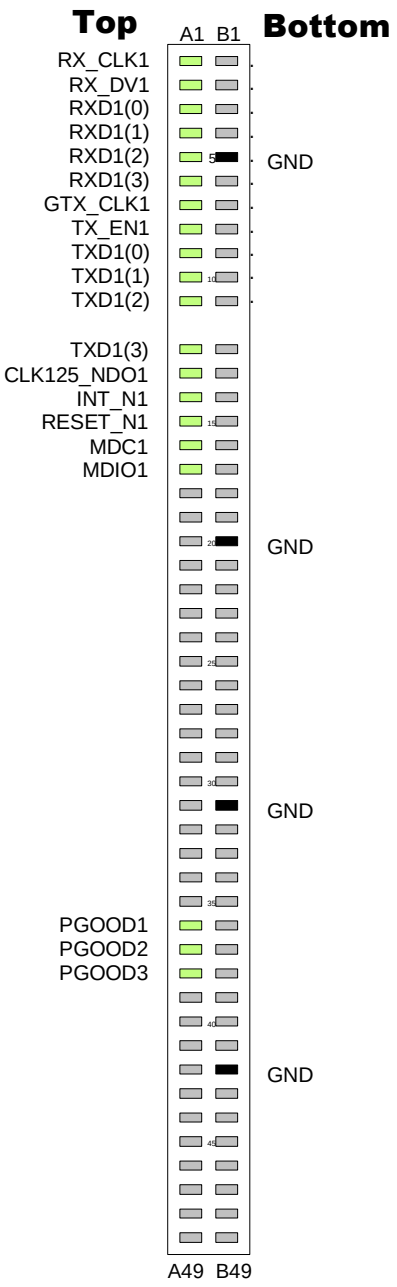
Pinout

USB

Both USB ports are equipped with mini type AB connectors. (G = GND). In both cases, the COM-1524 acts as a USB device.

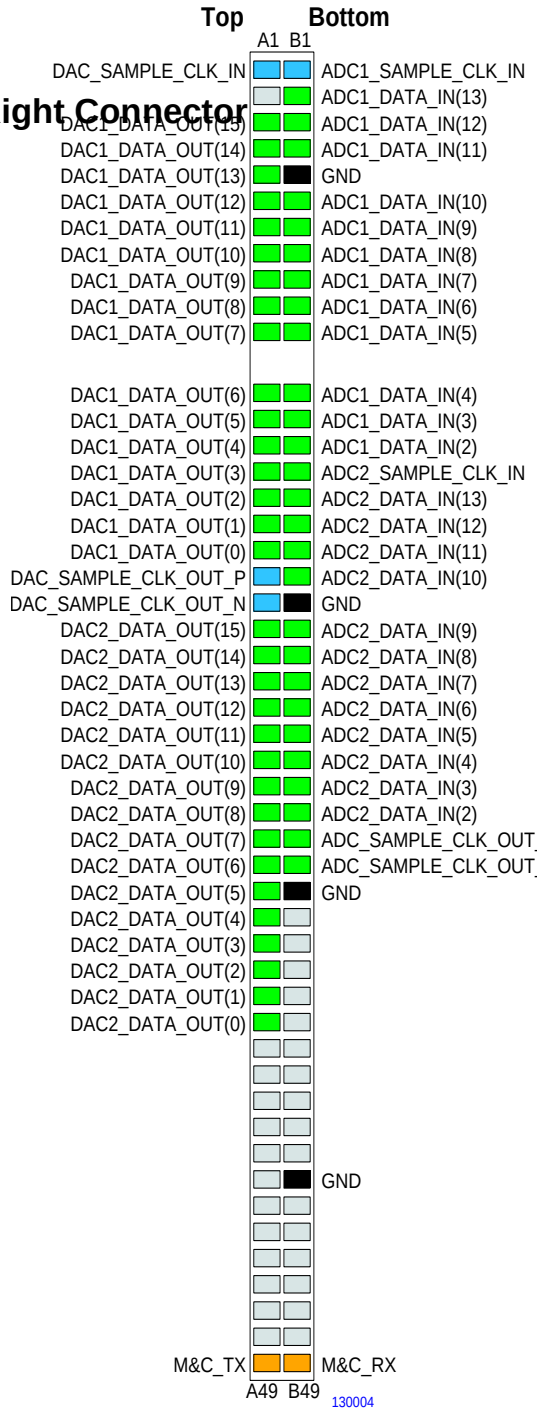


Left Connector J6



This interface is compatible with the COM-5102/COM-5401
10/100/1000 Mbps Ethernet PHY
. **(–A firmware)**

Right Connector



2*16-bit output samples, 2*12-bit input samples. This interface is compatible with the COM-3504 dual Analog<->Digital Conversions.

I/O Compatibility List

(not an exhaustive list)

Left connector (J6)
COM-5102 Gigabit Ethernet + HDMI interface
COM-5401 4-port 10/100/1000 Mbps Ethernet Transceivers (limited to one port)
COM-1500 FPGA + DDR2 SODIMM socket + ARM development platform
Right connector (J9)
COM-3504 Dual Analog <-> Digital Conversions
COM-1524 channel emulator
COM-1500 FPGA + DDR2 SODIMM socket + ARM development platform

Configuration Management

This specification is to be used in conjunction with VHDL software revision 6.

ComBlock Ordering Information

COM-1505 Integrated PSK modem

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