COM-1509SOFT CONVOLUTIONAL FEC ENCODER / VITERBI DECODER
VHDL source code overview / IP core

Overview

The COM-1509SOFT comprises the following components which can be independently instantiated:

- Convolutional FEC encoder,
- Viterbi decoder
- V.35 scrambler
- V.35 descrambler
- Serial HDLC framing
- Serial HDLC deframing

The entire **VHDL source code** is deliverable.

Decoder key features

- Single or parallel implementation for either minimum size or maximum (Gbps) speed.
- Flexible dynamic (i.e. at runtime) user-selected configuration:
  - Hard (1-bit) or soft(4-bit) decision decoding
  - G0,G1,G2 generator polynomials
  - Constraint length K=3,5,7,9
  - Puncturing patterns for rates 2/3,3/4,5/6,7/8
  - 2, 3, 7 parity bits
- Support for erasures (code puncturing)
- Reduced latency: K*25 bits
- Self-synchronizing to automatically align the incoming encoded stream with the periodic encoding/puncturing pattern
- Out-of-sync indicator to synchronize external demodulator (for removing PSK demod phase ambiguity for example)

Ancillary features:

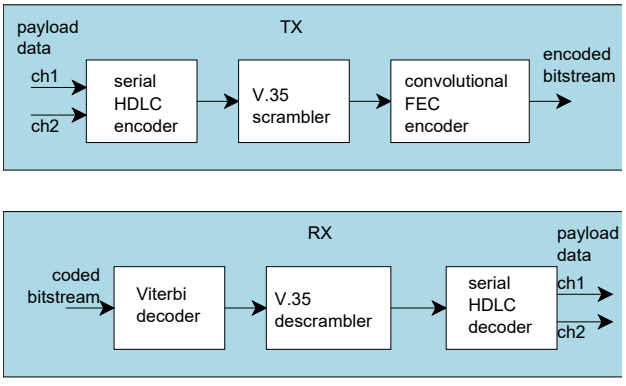
- V.35 scrambling and descrambling
- Serial HDLC framing/deframing. Serial HDLC encapsulates payload data in a frame for transmission over a continuous data stream. 2 virtual channels can be multiplexed over the same stream. A 16-bit CRC is inserted at the end of each frame to detect errors upon reception. HDLC framing transmits empty frames when no payload data is available.
- PRBS11 test sequence generator
- BER testers

- Provided with IP core:
  - VHDL source code
  - Matlab .m file to generate stimulus files for VHDL simulation at various signal to noise ratios
  - VHDL testbench

Target Hardware

The code is written in generic standard VHDL and is thus portable to a variety of FPGAs. The code was developed and tested on a Xilinx 7-series FPGA but is expected to work similarly on other targets. No manufacturer-specific primitive is used.

Overall Block Diagram



MSS • 845-N Quince Orchard Boulevard • Gaithersburg, Maryland 20878 • U.S.A.
Telephone: (240) 631-1111 www.ComBlock.com
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Configuration

Synthesis-time configuration parameters

The following constants are user-defined in the generic section of the component instantiation prior to synthesis. These parameters generally define the size of the embodiment.

Decoder synthesis-time configuration parameters	
Parameters	**Configuration**
Number of parallel decoders instantiated **NDEC**	Typical values: 1 (for minimum size serial architecture), 2,4,8 (for maximum throughput parallel architecture)
Hard/Soft-decision decoding **HARD_SOFTN_DECISION**	'1' for 1-bit width input '0' for 4-bit width input
Maximum constraint length **K_MAX**	Valid values are 3,5,7,9
Maximum number of parity bits **N_PARITY_BITS_MAX**	For example 3 for rate 1/3, or 2 for rate 2/3. Valid range 2 - 7 Size vectors/arrays accordingly. If this decoder is only used with 2-bit parity, smaller implementations may be achieved by setting **N_PARITY_BITS_MAX**= 2
Traceback depth **TB_DEPTH**	Traceback depth. MUST BE LESS THAN 120. Typically := 6***K_MAX** for non-punctured codes or 12***K_MAX** for punctured codes.
HDLC tx/rx synthesis-time configuration parameters	
Maximum HDLC frame size **FRAME_SIZE_MAX**	Maximum frame size (in bytes) before deciding to encode and send Valid range 0 - 2047 bytes

Run-time configuration parameters

The user can set and modify the following controls at run-time through the top level component interface:

Encoder	
Parameters	**Configuration**
Constraint length K and rate R	0000 = (K=5, R=1/7) 0001 = (K = 7, R=1/2, Intelsat) 0010 = (K = 7, R=2/3, Intelsat) 0011 = (K = 7, R=3/4, Intelsat) 0100 = (K = 7, R=5/6, Intelsat) 0101 = (K = 7, R=7/8, Intelsat) 0110 = (K = 9, R=1/3) 0111 = (K = 9, R=1/2) 1000 = (K = 9, R=2/3) 1001 = (TCM, K=7, R=2/3)[1] 1010 = (TCM, K=7, R=3/4)[1] 1011 = (K = 7, R=1/2, CCSDS) 1100 = (K = 7, R=2/3, CCSDS) 1101 = (K = 7, R=3/4, CCSDS) 1110 = (K = 7, R=5/6, CCSDS) 1111 = (K = 7, R=7/8, CCSDS) CONTROL(4:1)
Differential Encoding	0 = disabled 1 = enabled CONTROL(5)
Continuous / Block mode	Determines whether the SOF_RESET mode should be enabled for resetting the encoder at the start of a block. 0 = continuous 1 = block mode. CONTROL(6)
Output sample format	00 = 1 bit serial 01 = 2 bit parallel (I/Q) for connection to QPSK modulator. 10 = 3-bit parallel for connection to 8-PSK modulator. 11 = 4-bit parallel for connection to 16-PSK modulator This field is ignored when TCM mode is selected. CONTROL(9:8)
Internal pattern generation (test mode)	00 = test mode disabled 01 = counting sequence: When set, the baseband input is disabled and a periodic pattern is internally generated at the encoder input. The pattern consists of an 8-bit counter, MSB transmitted first. 10 = PRBS-11. internal generation of 2047-bit periodic pseudo-random

1 Not supported in decoder

	bit sequence as modulator input. (overrides external input bit stream). Useful in measuring BER performances in conjunction with the decoder BER tester. The test pattern bit rate is automatically set by the external sink module (typically a modulator) as part of the flow control mechanism. CONTROL(11:10)
Decoder	
Generator polynomials **G**	Traditionally expressed as a K-bit octal number. For example CCSDS generator polynomials are G0: **G(8 downto 0) <= O"171";** G1: **G(17 downto 9) <= O"133";** Gn: **G(62:18)** <= (others => '0')
Number of parity bits **N_PARITY_BITS**	number of parity bits (i.e. generator polynomials). Valid range: 2 - 7 MUST be less than or equal to the hardware capabilities set by **N_PARITY_BITS_MAX** defined in the generic section
Constraint length **K**	Valid values are 3,5,7,9 Must be less than or equal to **K_MAX**
Convolutional encoding rate **R1/R2**	Valid values are 1/2, 1/3, 1/7, 2/3, 3/4, 5/6, 7/8
STANDARD	There are some minor variations among standards, such as different puncturing scheme or inversion 0 = Intelsat 1 = CCSDS 2 = DVB rate 1/2 only others = yet TBD
DIFF_ENC_ON	input stream is differentially encoded (1) or not (0)
HIGH_SNR	It is sometimes helpful to adjust in-lock/out-of-lock detection thresholds to trade-off probability of missed out of lock and probability of false detection
SKIP1BIT_ PULSE	Skip one encoded input bit for each 1 CLK-wide pulse This feature is used to synchronize the input stream with the periodic encoding/puncturing pattern

Codes

Convolutional codes are defined by the generator polynomials Gx and puncturing pattern if any. Codes defined in various standards are listed below.

0 marks an erasure during puncturing.

K = 5

The generator polynomials for K = 5 R = 1/7 is

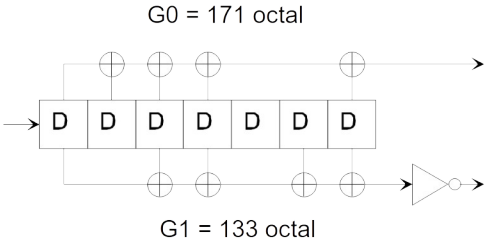
$G_0(x) = 1 + x + x^2 + x^4$
$G_1(x) = 1 + x^2 + x^3 + x^4$
$G_2(x) = 1 + x^2 + x^4$
$G_3(x) = 1 + x^2 + x^3 + x^4$
$G_4(x) = 1 + x + x^3 + x^4$
$G_5(x) = 1 + x + x^2 + x^4$
$G_6(x) = 1 + x + x^2 + x^3 + x^4$

K = 7 (CCSDS)

The generator polynomials for K = 7 R = ½ are

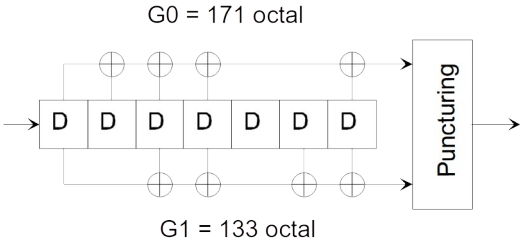
$G_0(x) = 1 + x + x^2 + x^3 + x^6$
$G_1(x) = 1 + x^2 + x^3 + x^5 + x^6$

171(octal) and 133(octal). The implementation is depicted below:



Basic CCSDS convolutional encoder

The basic encoder inverts the G_1 output. When using puncturing, this inverter is removed.



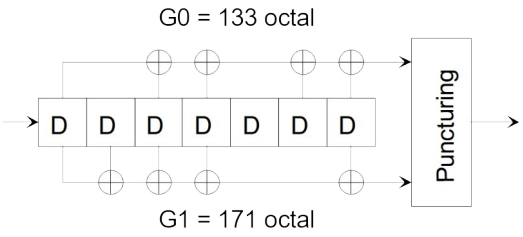
CCSDS convolutional encoder with puncturing

Rates other than ½ are implemented by puncturing the rate ½ encoded data stream. The puncturing pattern is as follows (1 denotes transmission, 0 blocking)

CCSDS puncturing		
Constraint length	K=7	
Generator Polynomials	G0 = o"171" G1 = o"133"	
Puncturing pattern rate 1/2	G0 1 G1 1	
Puncturing pattern rate 2/3	G0 1 0 G1 1 1	
Puncturing pattern rate ¾	G0 1 0 1 G1 1 1 0	
Puncturing pattern rate 5/6	G0 1 0 1 0 1 G1 1 1 0 1 0	
Puncturing pattern rate 7/8	G0 1 0 0 0 1 0 1 G1 1 1 1 1 0 1 0	

K = 7 (Intelsat)

The generator polynomials for K = 7 R = ½ are
$G_0(x) = 1 + x^2 + x^3 + x^5 + x^6$
$G_1(x) = 1 + x + x^2 + x^3 + x^6$
133(octal) and 171(octal). The implementation is depicted below:



Rates other than ½ are implemented by puncturing the rate ½ encoded data stream. The puncturing pattern is as follows (1 denotes transmission, 0 blocking)

Intelsat puncturing		
Constraint length	K=7	
Generator Polynomials	G0 = o"133" G1 = o"171"	
Puncturing pattern rate 1/2	G0 1 G1 1	
Puncturing pattern rate 2/3	G0 1 1 G1 1 0	
Puncturing pattern rate ¾	G0 1 1 0 G1 1 0 1	
Puncturing pattern rate 5/6	G0 1 1 0 1 0 G1 1 0 1 0 1	
Puncturing pattern rate 7/8	G0 1 1 1 1 0 1 0 G1 1 0 0 0 1 0 1	

K = 9 R = 1/3

The generator polynomials for K = 9 R = 1/3 are
$G_0(x) = 1 + x^2 + x^3 + x^5 + x^6 + x^7 + x^8$.
$G_1(x) = 1 + x + x^3 + x^4 + x^7 + x^8$.
$G_2(x) = 1 + x + x^2 + x^5 + x^8$.

K = 9 R = ½, 2/3

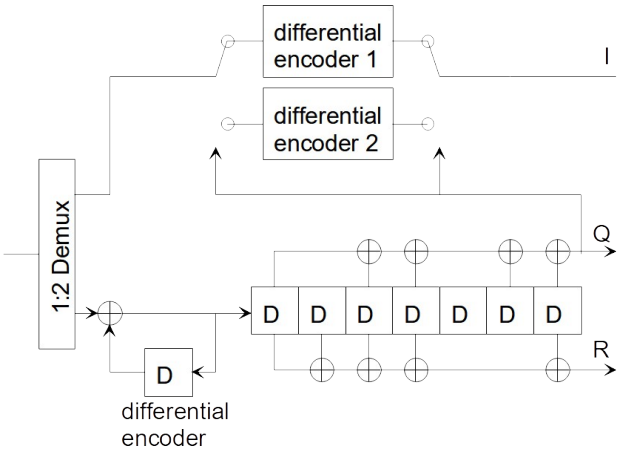
The generator polynomials for K = 9 R = 1/2 are
$G_0(x) = 1 + x + x^2 + x^3 + x^5 + x^7 + x^8$.
$G_1(x) = 1 + x^2 + x^3 + x^4 + x^8$.

The rate 2/3 is implemented by puncturing the rate ½ encoded data stream. The puncturing pattern is as follows (1 denotes transmission, 0 blocking):

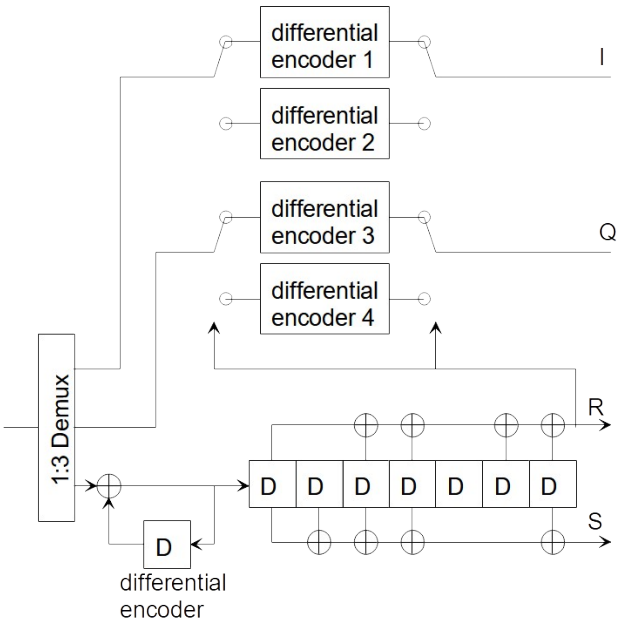
Rate 2/3	G_0	11
	G_1	01

Treillis Coded Modulation (TCM) Encoder[1]

As per Intelsat IESS-310 for rate 2/3 8-PSK.



TCM encoder, rate 2/3 for 8-PSK



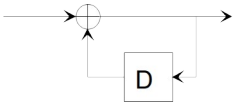
TCM encoder, rate 3/4 for 16-PSK

K = 6 (DVB)[2]

The generator polynomials for K = 6 R = ½ are
$G_0(x) = 1 + x + x^2 + x^3 + x^6$
$G_1(x) = 1 + x^2 + x^3 + x^5 + x^6$
171(octal) and 133(octal).

Differential Encoding

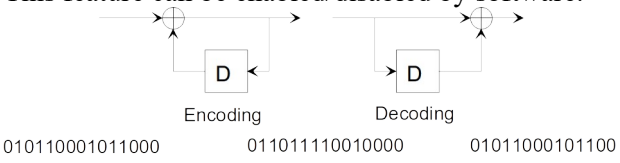
Differential encoding can be used prior to FEC encoding as specified in Intelsat IESS-308/309. This feature can be enabled/disabled by software.



This mode compensates for any bit inversion occurring in the transmission channel (for example at a BPSK demodulator which cannot resolve the inherent 180deg phase ambiguity).

Differential Decoding

Differential decoding can be used following FEC decoding as specified in Intelsat IESS-308/309. This feature can be enabled/disabled by software.



This mode compensates for any bit inversion occurring in the transmission channel (for example at a BPSK demodulator which cannot resolve the inherent 180deg phase ambiguity). This ambiguity resolution mechanism has a cost: the bit error rate is doubled.

I/Os

CLK: input
The synchronous clock. The user must provide a global clock (use BUFG). The CLK timing period must be constrained in the constraint file (.xdc) associated with the project.

SYNC_RESET: input
Synchronous reset. The reset MUST be exercised at least once to initialize the internal variables.

DATAIN(31:0):
32-bit input packing eight soft-quantized samples. Input samples are soft-quantized with 4-bits. Format is offset binary whereby 0000 represents a 'strong' 0, 1111 a strong '1', 0111 the weakest '0' and 1000 the weakest '1'.

When using hard-decision decoding, encoded bits are placed at location at indices 3+i*4 (31,27,…7,3) in the vector. Other locations are ignored.

Packing order for the eight samples is from the most significant side to the least significant side of this array e.g. (DATAIN(31:28) is the first received soft-decision sample)

DATAIN_VALID:
1 CLK-wide pulse indicating that DATAIN is valid.

DATAIN_READY:
A flow-control signal indicating whether the decoder is ready to accept new DATAIN input samples.

There are two types of decoder outputs: 1-bit serial (**DATAOUT1b** / **DATAOUT1b_VALID**) or 8-bit parallel (**DATAOUT8b** / **DATAOUT8b_VALID**) Bit order in 8-bit parallel mode is MSb first.

2 Not supported in encoder

Monitoring

Bit Error Rate Measurement

The decoder estimates the bit error rate **BER(31:0)** on the encoded input bit stream by comparing the actual received bit stream with an estimate of the transmitted bit stream. This estimate is generated by re-encoding the nearly error-free decoded bit stream.

The algorithm is based on the proposition that the decoded bit stream is nearly error-free. If the decoded bit stream were error-free, then the re-encoded bit stream would be the actual transmitted encoded bit stream before bit errors occur in the transmission channel.

The bit error rate is computed over a window of 1000 input bits. This measurement window length **BER_WINDOW_LENGTH** is a constant set in *VA.vhd*. The synchronization thresholds **BER_THRESHOLD_xx** are set on the basis of a 1000-bit window.

Read the **BER** when **BER_VALID** is '1'.

Self Synchronization

When the decoder detects that the bit error is greater than a set threshold, it attempts to re-synchronize. Different thresholds are used for the various encoding rates. See the **BER_THRESHOLD_xx** constants in *VA.vhd*.

IN_SYNC: out std_logic;
OUT_OF_SYNC: out std_logic;
1 CLK-wide pulses every **BER_WINDOW_LENGTH** bits to indicate either synchronization (when **BER** is below threshold) or lack of synchronization (**BER** above threshold)

OUT_OF_SYNC pulse indicates that the input coding groups are not aligned with the transmitted coding groups, i.e. received bit in the G0 bin not actually generated by G0, etc. This information is typically used by external circuitry to realign the received encoded bit stream with the expected parity groups or puncturing pattern, or to correct for PSK demodulator phase ambiguities, etc.

LOCK_STATUS: out std_logic
a continuous '1' when measured **BER** is below the set threshold. Toggling when unlocked

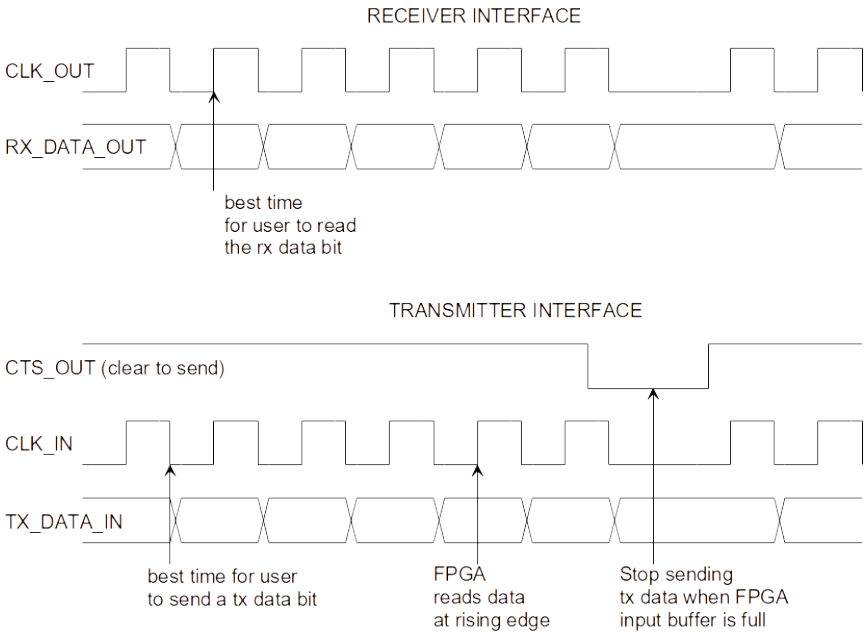
Standards

Support for the following standards:
Intelsat IESS-308/309
Intelsat IESS-310
DVB ETS 300 421[3]
DVB ETS 300 744[3]
CCSDS 101.0-B-6

3 Not supported in encoder

I/Os

1-bit synchronous serial



The user should always check the “Clear-To-Send” CTS_OUT flag before sending additional data bits to the modulator.

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Software Licensing

The COM-1509SOFT is supplied under the following key licensing terms:

1. A nonexclusive, nontransferable license to use the VHDL source code internally, and
2. An unlimited, royalty-free, nonexclusive transferable license to make and use products incorporating the licensed materials, solely in bitstream format, on a worldwide basis.

The complete VHDL/IP Software License Agreement can be downloaded from http://www.comblock.com/download/softwarelicense.pdf

Configuration Management

The current software revision is 005a 101725.

Directory	Contents
/doc	Specifications, user manual, implementation documents
/src	.vhd source code, ..ngc constraint files, .pkg packages. One component per file.
/sim	Test benches for VHDL simulation of Viterbi decoder (from input stimulus file), or back to back FEC codec, V35 scrambling, HDLC framing.
/matlab	Matlab .m files to generate encoded input files with various Eb/N0 and to compute expected BER.

Project files:

Xilinx Vivado v2020 project file:
/project_1/project_1vivado2020.xpr

More generally, a tcl file can help construct the complete project:
/project_1/project_1vivado2020.tcl
It includes all the constituent components.

VHDL development environment

The VHDL software was developed using the following development environment:

Xilinx Vivado 2020 for synthesis, place and route and VHDL simulation

Device Utilization Summary

The decoder implementation size depends essentially on three key user-defined parameters in the Viterbi decoder generic section, namely:

- Hard/Soft-decision decoding **HARD_SOFTN_DECISION**
- Maximum constraint length **K_MAX** (the actual constraint length **K** is dynamically configurable at run-time but cannot exceed the hardware capabilities defined by **K_MAX**)
- Maximum number of parity bits **N_PARITY_BITS_MAX** (the actual number of parity bits **N_PARITY_BITS** is dynamically configurable at run-time but cannot exceed the hardware capabilities defined by **N_PARITY_BITS_MAX**)

Device: Kintex ultrascale+ xcku5p-ffvd900-3-e

Viterbi decoder K=5 or 7 2 parity bits NDEC = 1 4-bit soft decision input traceback depth 84		
LUTs	3526	1.6%
Registers	3235	0.8%
Block RAM/FIFO 36Kb	1.5	0.3%
DSP48	0	0%
GCLKs	1	0.4%

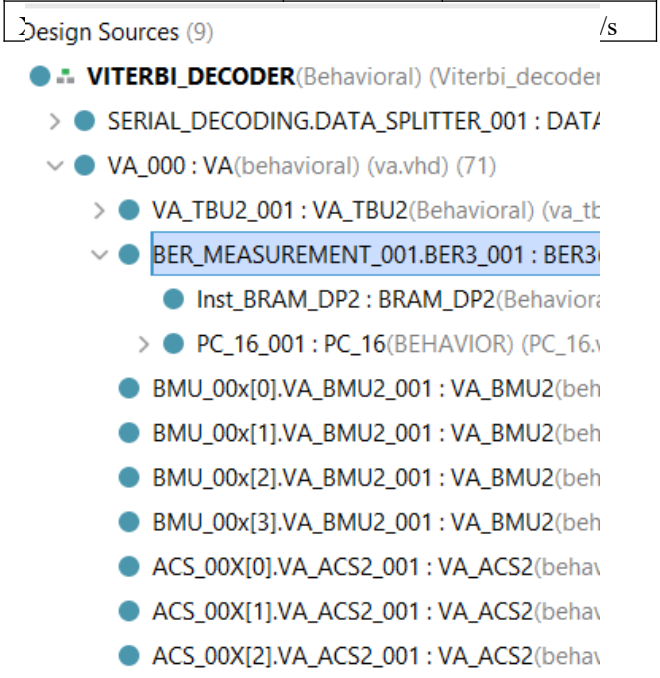
Viterbi decoder K=5 or 7 2 parity bits NDEC = 8 parallel 4-bit soft decision input traceback depth 84		
LUTs	20710	9.6%
Registers	20197	4.7%
Block RAM/FIFO 36Kb	20.5	4.3%
DSP48	0	0%
GCLKs1		0.4%

Encoder		
LUTs	172	0.1%
Registers	162	0.04%
Block RAM/FIFO 36Kb	0	0%
DSP48	0	0%
GCLKs	1	0.4%

Clock speed, bit rates

The entire design uses a single global clock CLK. Typical maximum clock frequencies for various FPGA families are listed below:

Device family - speed grade	**f_{CLK}**	Max encoded/decoded bit rate 1 decoder 2 parity bits
AMD/Kintex ultrascale+ -3	423 MHz	423/211 Mbits/s
Xilinx Kintex 7 -2	344 MHz	344/172 Mbits/s
Xilinx Virtex-6 -2	272 MHz	272/136 Mbits/s



The maximum decoded bit rate is
f_{CLK} *NDEC / N_PARITY_BITS
Where **NDEC** is the number of parallel decoders embodied in the design.

VHDL components overview

Viterbi decoder

VITERBI_DECODER.vhd is the decoder top component in this hierarchical design. It's role is to segment the continuous input stream of encoded (hard or soft-quantized) bits into fixed-length blocks which can be processed by **NDEC** parallel decoders. The decoded bit stream is then reassembled into a seamless output stream. This component also adjusts the alignment of the input encoded bit stream with the coding and puncturing periodic pattern. Indeed, the follow-on Viterbi algorithm (*VA.vhd*) can only work properly if a parity bit encoded by generator polynomial Gx in the transmitter is decoded with the same generator polynomial at the receiver.

DATA_SPLITTER.vhd implements the continuous input stream segmentation.

VA.vhd is the heart of the Viterbi algorithm which includes three key processes: The branch metric unit (*VA_BMU2.vhd*), the Add-Compare-Select (*VA_ACS2.vhd*) and the traceback unit (*VA_TBU2.vhd*).

VA_BMU2.vhd computes the local distance between received soft-quantized bits and the hypothesis being tested. Received bits marked with the erasures flag are ignored in the distance computation.

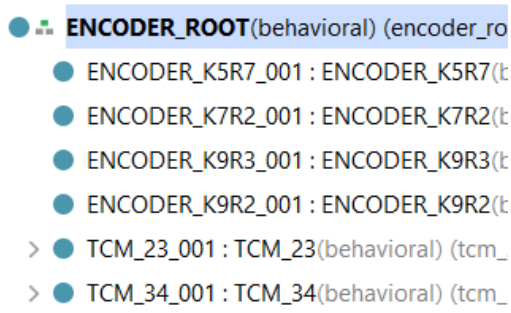
VA_TBU2.vhd segments the stream of add-compare-select outputs into overlapping blocks of length 2* **TB_DEPTH**., long enough for the Viterbi algorithm to converge. The process is repeated every **TB_DEPTH** bits. The **TB_DEPTH** decoded bits are then read in the reverse order.

BER3.vhd estimates the coded input bit error rate by comparing it with the reconstructed encoded input (obtained by re-encoding the decoded sequence).

INFILE2SIM.vhd reads an input file. This component is used by the testbench to read a soft-quantized or hard-quantized encoded bit stream generated by the *viterbi_dec_input_genprbs11.m* Matlab program for various Eb/No cases.

SIM2OUTFILE.vhd writes three 12-bit data variables to a tab delimited file which can be subsequently read by Matlab (load command) for plotting or analysis.

Encoder



Ancillary components

VHDL simulation

Three VHDL testbenches in the /sim directory provide bit-accurate VHDL simulations:

- *TB_VITERBI_DECODER.vhd* is the decoder testbench. Its input consists of soft-quantized noisy samples generated by the supplied Matlab programs `viterbi_dec_input_genprbs11.m` or `viterbi_dec_input_gen.m`

- *TB_ENC_DEC_V35.vhd:* end-to-end simulation testbench encompassing convolutional encoder, Viterbi decoder, scrambling, descrambling, PRBS-11 test sequence generation and BER tester.

- *TB_ENC_DEC_V35_HDLC.vhd:* end-to-end simulation testbench encompassing convolutional encoder, Viterbi decoder, scrambling, descrambling, serial HDLC framing and deframing, PRBS-11 test sequence generation and BER tester.

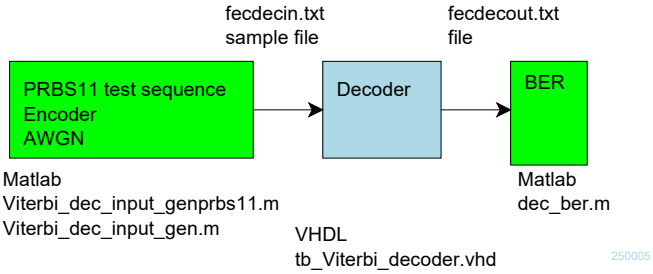
Note: when moving the project folder location, be sure to change accordingly the FILENAME file paths in *TB_VITERBI_DECODER.vhd* INFILE2SIM and SIM2OUTFILE components generic section.

Matlab simulation

The `viterbi_dec_input_genprbs11.m` program

1. generates a pseudo-random PRBS11 test sequence.
2. This test sequence undergoes convolutional encoding.
3. Additive White Gaussian noise is then added according to the user-specified Eb/No.
4. The resulting sum is quantized with 4-bit soft-quantization and saved in the `fecdecin.txt` file for subsequent VHDL simulation using the T*B_VITERBI_DECODER.vhd* testbench.

The `dec_ber.m` program reads a file of decoded data `fecdeccout.txt` generated by VHDL simulation and compare it with the original PRBS-11 test sequence. It counts the number of bit errors. [Note: it is redundant with the bit error rate tester BER2 within the VHDL testbenches]



Reference documents

[1]

Acronyms

Acronym	Definition
AWGN	Additive White Gaussian Noise
BRAM	Block RAM
CCSDS	Consultative Committee For Space Data Systems
BER	Bit Error Rate
BRAM	Dual-port Block RAM
CCSDS	Consultative Committee For Space Data Systems
FEC	Forward Error Correction
FPGA	Field Programmable Gate Array
HDLC	High-Level Data Link Control (framing protocol)
LSb	Least Significant bit
LUT	Lookup table (FPGA resource)
MSb	Most Significant bit
PRBS-11	Pseudo-Random Binary Sequence, 2047-bit period
RX	Receiver
TX	Transmitter
VHDL	VHSIC Hardware Description Language

ComBlock Ordering Information

COM-1509SOFT CONVOLUTIONAL FEC ENCODER / VITERBI DECODER, VHDL SOURCE CODE / IP CORE

ECCN: EAR99

MSS • 845-N Quince Orchard Boulevard•
Gaithersburg, Maryland 20878-1676 • U.S.A.
Telephone: (240) 631-1111
E-mail: sales@comblock.com