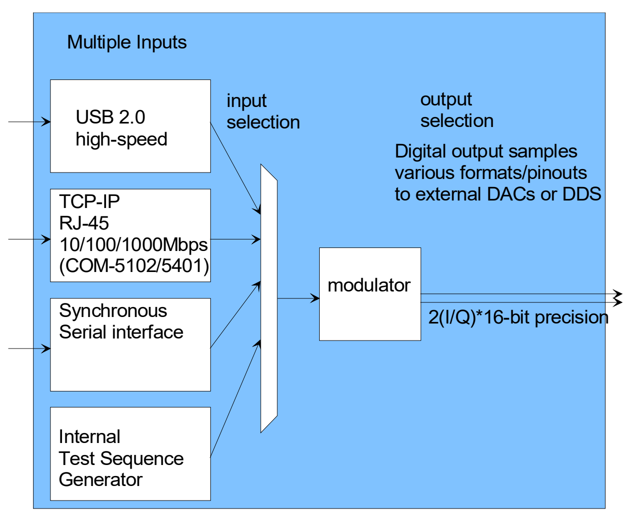
ComBlock

COM-1519 DIRECT-SEQUENCE SPREAD-SPECTRUM MODULATOR 60 Mchip/s

Key Features

- Direct Sequence Spread-Spectrum (DSSS) digital modulator.
- Programmable chip rates up to 60 Mchip/s.
- Spreading factor: 3 to 65535
- Spreading codes:
  - Gold sequences
  - Maximal length sequences
  - Barker codes (length 11, 13).
  - GPS C/A codes.
- Symbol rate selection fully independent of chip rate. Alternatively, symbol can be aligned with code period.
- Code modulation: BPSK/QPSK with output spectral shaping filter: raised cosine square root filter with 20% rolloff. Filter can be bypassed.
- Built-in test features:
  - Pseudo-random bit stream generation (PRBS-11) for end-to-end BER measurements
  - Unmodulated carrier
  - Precise additive white Gaussian noise
  - Frequency offset (Doppler fixed and/or sinusoidal)
- ComScope –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Input for an external, higher-stability 10 MHz frequency reference.
- Connectorized 3"x 3" module for ease of prototyping. High-speed 98-pin PCIe connectors (left, right). Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.



Modulator connectivity

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 Issued 7/27/2016

For the latest data sheet, please refer to the **ComBlock** web site: comblock.com/download/com1519.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

Electrical Interface

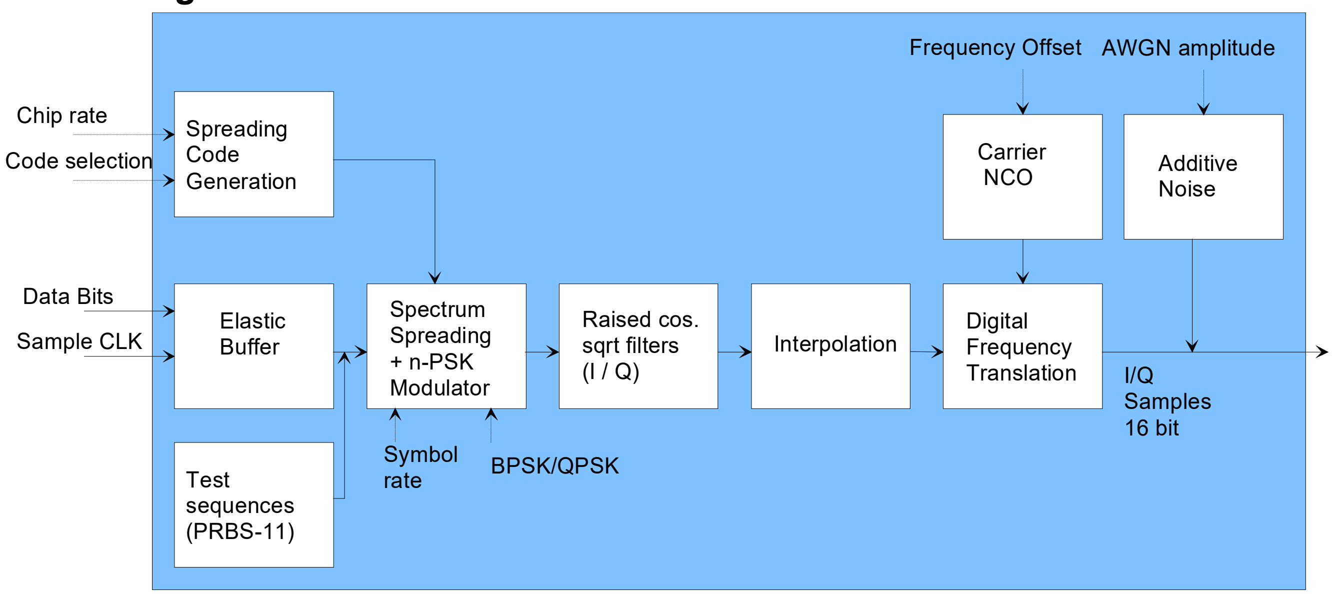
Three basic output types are available on the right J9 connector:

- Dual 10-bit DACs, parallel I and Q samples, output sampling clock.
- Dual 14-bit DACs, multiplexed I and Q samples, input sampling clock.
- Dual 16-bit DACs, parallel I and Q samples, output sampling clock.

Power Interface	4.75 – 5.25VDC. Terminal block. The maximum power consumption is 600mA.

Important: I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Block Diagram



Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- USB

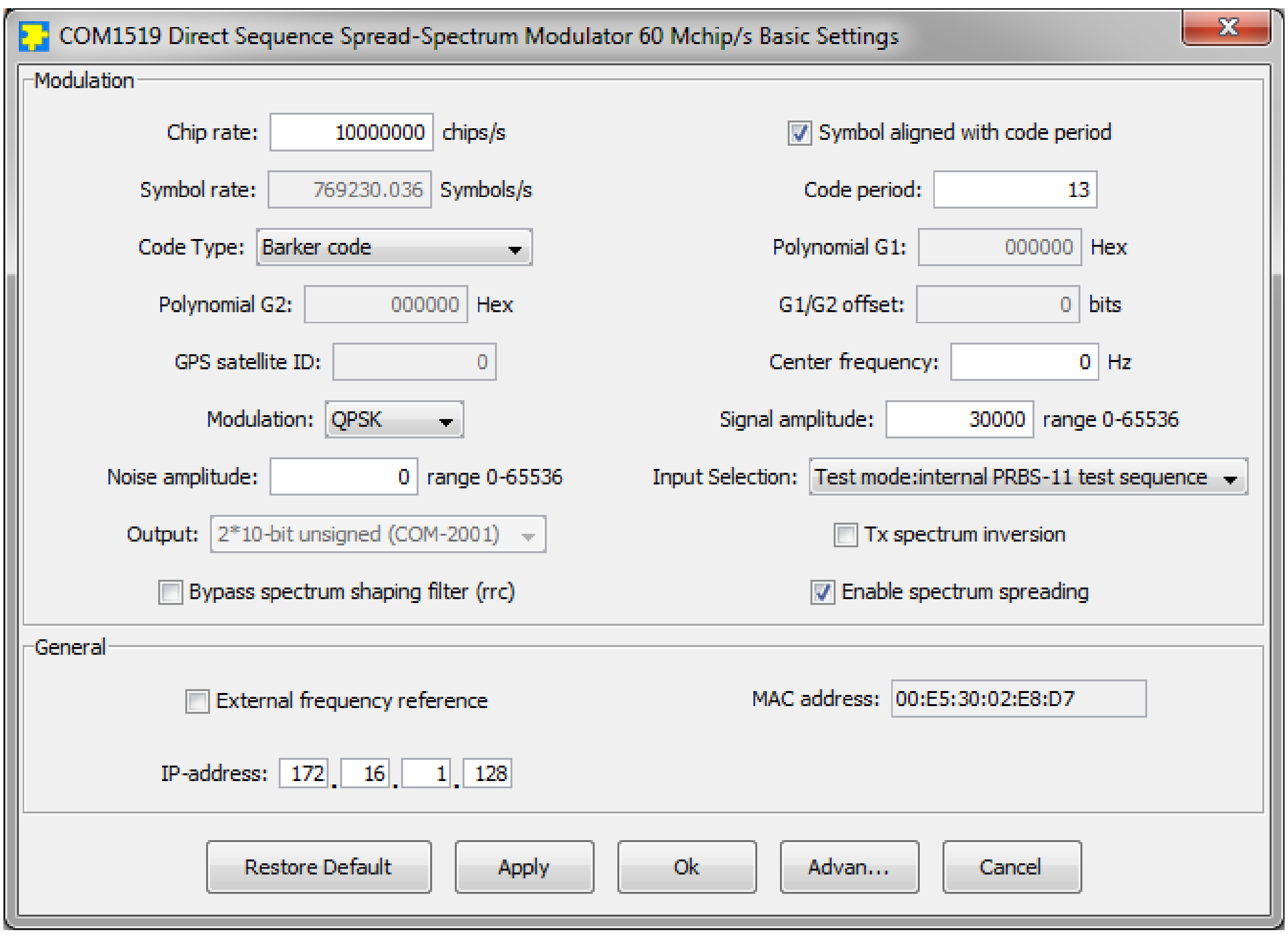
or connections via adjacent ComBlocks:

- USB
- TCP-IP/LAN,
- Asynchronous serial (DB9)
- PC Card (CardBus, PCMCIA).

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1519 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1519 module to be configured, next click the *Settings* button to display the *Settings* window shown below.



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center "Advanced" configuration or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Definitions for the Control registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). It is automatically loaded up at power up. All control registers are read/write.

Parameters	**Configuration**
Processing clock f_{clk_tx}	Modulator processing clock. Also serves as DAC sampling clock 20-bit unsigned integer expressed as $f_{clk\_tx} * 2^{20}$ / 300MHz. 120 MHz maximum. 20 MHz recommended minimum REG0 = bits 7-0 (LSB) REG1 = bits 15 – 8 (MSB) REG2(3:0) = bits 19 – 16 (MSB)
Internal/External frequency reference	0 = internal. Use the internal 60 MHz clock (from the USB PHY) as frequency reference. 1 = external. Use the 10 MHz clock externally supplied through the J7 SMA connector as frequency reference. REG2(7)
Chip rate $f_{chip\ rate\ tx}$	The modulator chip rate is in the form $f_{chip\ rate\ tx} = f_{clk\_tx} / 2^n$ where n ranges from 1 (2 samples per chip) to 15 (chip rate = f_{clk_tx} / 32768). n is defined in REG3(3:0)
Code period	In chips. Valid range 3 – 65535 Can be less than the natural length of the selected code. In which case, the code is truncated. REG4: LSB REG5: MSB
Code selection	1 = Gold code (G1/G2 software selection) 2 = Maximal length sequence (G1 software selection) 3 = Barker code (lengths 11 or 13 only) 4 = GPS C/A code REG6(3:0)
Gold sequence / Maximal Length Sequence generator polynomial G1	24-bit. Describes the taps in the linear feedback shift register 1: Bit 0 is the leftmost tap (2^0 in the polynomial). The largest non-zero bit is the polynomial order n. n determines the code period $2^n - 1$. Example: $G1 = 1 + x + x^4 + x^5 + x^6$ is represented as 0x000039 This field is used only if Gold code or Maximal length sequences are selected. REG7 = LSB REG8 REG9 = MSB
Gold code generator polynomial G2	24-bit. Describes the taps in the linear feedback shift register 2: Same format as G1 above. This field is used only if Gold codes are selected. REG10 = LSB REG11 REG12 = MSB
Gold code G1/G2 phase offset	A Gold code is generated by adding two maximal length sequences (as defined by their generator polynomials G1 and G2). A set of orthogonal Gold codes can be created by changing the phase offset between the two maximal length sequences. REG35 (LSB) – REG37 (MSB)
GPS satellite ID	GPS signals from different satellites are designated by a PRN signal number in the range 1 – 37. This field is used only if GPS C/A codes are selected. REG10(5:0)

LSB = Least Significant Byte
MSB = Most Significant Byte

Symbol rate f_{symbol_rate}	The symbol rate can be set independently of the spreading code period. In this case, set REG13-16 such that $f_{symbol\_rate} * 2^{32} / f_{clk\_tx}$ REG13 = LSB REG14 REG15 REG16 = MSB Alternatively, symbols can be aligned with the spreading code period. In this case, REG16(7) as '1'. REG13-15 are ignored.
Digital Signal gain	16-bit amplitude scaling factor for the modulated signal. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Therefore, we recommend checking for saturation at the D/A converter when changing either the symbol rate or the signal gain. (see status registers SREG8) REG17 = LSB REG18 = MSB
Additive White Gaussian Noise gain	16-bit amplitude scaling factor for additive white Gaussian noise. Because of the potential for saturation, please check for saturation at the D/A converter when changing this parameter. REG19 = LSB REG20 = MSB
Modulation type	Modulation type before applying the direct-sequence spreading. Note: the modulation symbol transitions are not necessarily aligned with the chip transitions. 0 = BPSK 1 = QPSK REG21(5:0)
Spectrum inversion	Invert Q bit. (Inverts the modulated spectrum only, not the subsequent frequency translation) 0 = off 1 = on REG21(6)
Ouput spectrum shaping filter enabled	Enables/Disables raised cosine square root output spectrum shaping filter. 0 = enabled 1 = bypassed REG21(7)

Input selection / format, test modes	Select the origin of the modulator input data stream. 1 = from left J6 connector (Many comblocks), 1-bit serial 2 = high-speed USB, 8-bit parallel 3 = LAN/TCP-IP, port 1024 (through Ethernet adapter), 8-bit parallel 4 = test sequence: internal generation of 2047-bit periodic pseudo-random bit sequence as modulator input. (overrides external input bit stream). 5 = test sequence: unmodulated carrier. This helps checking the follow-on RF modulator. 8-bit parallel input bytes are transmitted MSb first. Test sequences override external input bit stream. REG22(2:0)
Spreading	Enable/Disable spectrum spreading. 0 = disabled 1 = enabled REG22(3)
Enable test points	Enable (1)/Disable (0) test points on J6 connector REG22(4)
Transmit sync word	Insert periodic 32 bit synchronization sequence to assist the demodulator in synchronizing and recovering ambiguities. The unique word is 5A 0F BE 66, transmitted MSb first. 2048 data symbols are transmitted between successive unique words. The unique word is using a simplified BPSK modulation, irrespective of the modulation type. 0 = disabled 1 = periodically insert a sync word. REG22(5)
Reserved	REG22(7) must be 0
Output Center frequency (**f_{c_tx}**)	Fine tuning of center frequency. Typically 0 Hz. 32-bit signed integer (2's complement representation) expressed as **f_{c_tx}** $* 2^{32} /$ **f_{clk_tx}** For a clean output waveform, we recommend keeping the maximum frequency (center frequency + ½ symbol rate) below 1/10th of the processing clock **f_{clk_tx}**. Note: as the AWGN noise samples are not frequency translated, noise tests should only be performed while the center frequency translation is smaller than the modulation bandwidth. REG23: LSB REG24 REG25 REG26: MSB
Sinusoidal frequency offset	In addition to the fixed frequency offset above, a sinusoidal frequency offset can be generated to mimic Doppler rate in highly mobile applications. This offset is characterized by two parameters: amplitude and period. The amplitude (a frequency) is expressed as **$f_{c\_amplitude}$** $* 2^{32} /$ **f_{clk_tx}** in the following control registers: REG27: LSB REG28 REG29 REG30: MSB The period is expressed as $2^{32} /($**f_{clk_tx}** $*T)$ in the following control registers: REG31: LSB REG32 REG33 REG34: MSB
Network Interface	
Parameters	**Configuration**
IP address (when connected to Gbit Ethernet PHY like **COM-5102, COM-5104**)	4-byte IPv4 address. Example : 0x AC 10 01 80 designates address 172.16.1.128 The new address becomes effective immediately (no need to reset the ComBlock). REG41: MSB REG42 REG43 REG44: LSB

(Re-)Writing to the last control register REG44 is recommended after a configuration change to enact the change.

Monitoring

Status Registers

Parameters	Monitoring
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-6 Properly operating hardware will result in the following sequence being displayed: SREG0/1/2/3/4/5/6/7 = 2C F1 95 xx 0F 01 24
Saturation	Denotes saturation in the transmit path. SREG8(0)
TCP-IP Connection Monitoring	
Parameters	**Monitoring**
LAN PHY ID	Expect 0x22 when LAN adapter is plugged in. SREG7
TCP-IP connections	Bit 0 = port 1028 (M&C) connected Bit 1 = port 1024 (data) connected 1 for connected, 0 otherwise SREG9(1:0)
MAC address	Unique 48-bit hardware address (802.3). In the form SREG17:SREG18:SREG19:…:SREG22
SNR calibration	
Parameters	**Monitoring**
Measured modulated signal power	SREG11(LSB) SREG12 SREG13(MSB)
Measured AWGN power (Noise bandwidth is twice the modulated spread-spectrum signal bandwidth)	SREG14(LSB) SREG15 SREG16(MSB)

Digital Test Points

Enabled if REG22(4) = '1', high-impedance otherwise.

Test Point	Definition
J6 connector pin A31	Start of periodic spreading code
J6 connector pin A32	Spreading sequence
J6 connector pin A33	Chip rate
J6 connector pin A34	Symbol rate
J6 connector pin A35	PRBS-11 (test sequence) start of sequence.
DONE	FPGA DONE pin. High indicates proper FPGA configuration

ComScope Monitoring

Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-1519 signal traces are defined as follows:

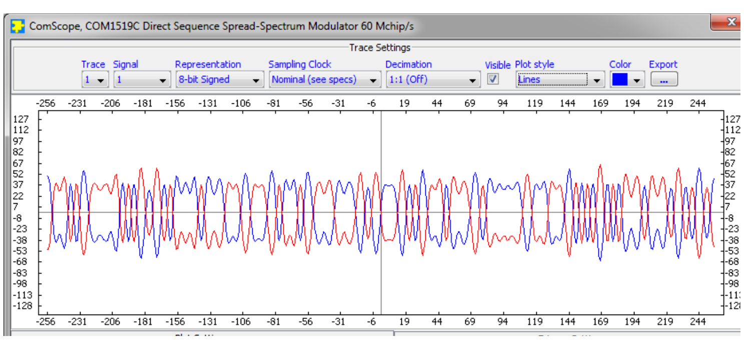
Trace 1 signals	Format	Nominal sampling rate	Capture length (samples)
1: baseband modulated I-channel	8-bit signed	f_{clk_tx}	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: baseband modulated Q-channel	8-bit signed	f_{clk_tx}	512
Trace 3 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
N/A			

Trigger Signal	Format
N/A	

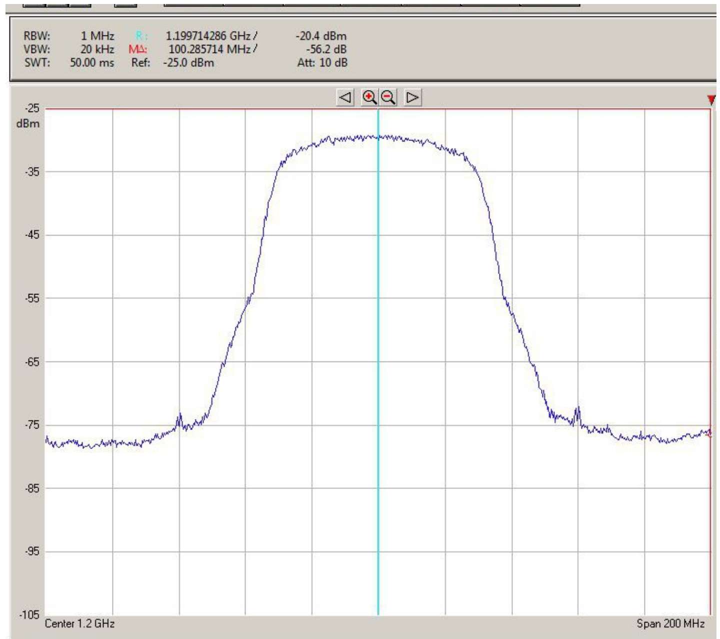
Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk_tx} processing clock as real-time sampling clock.

In particular, selecting the f_{clk_tx} processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

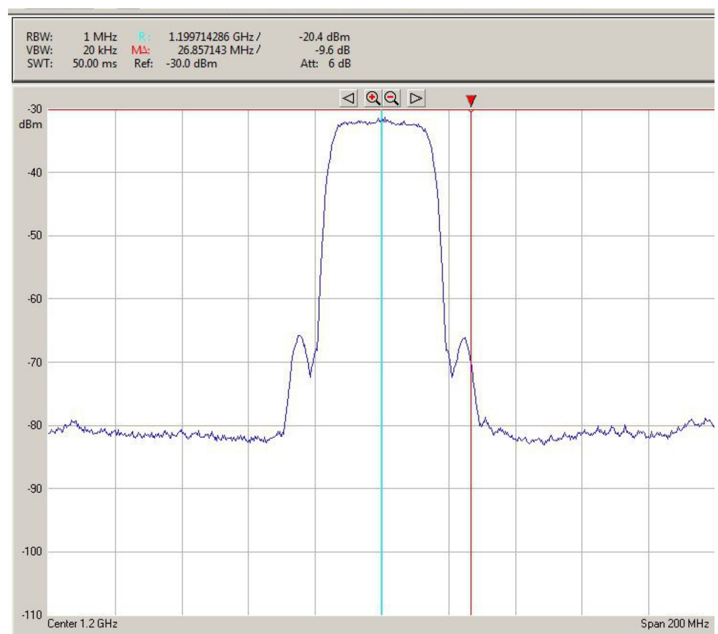
The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



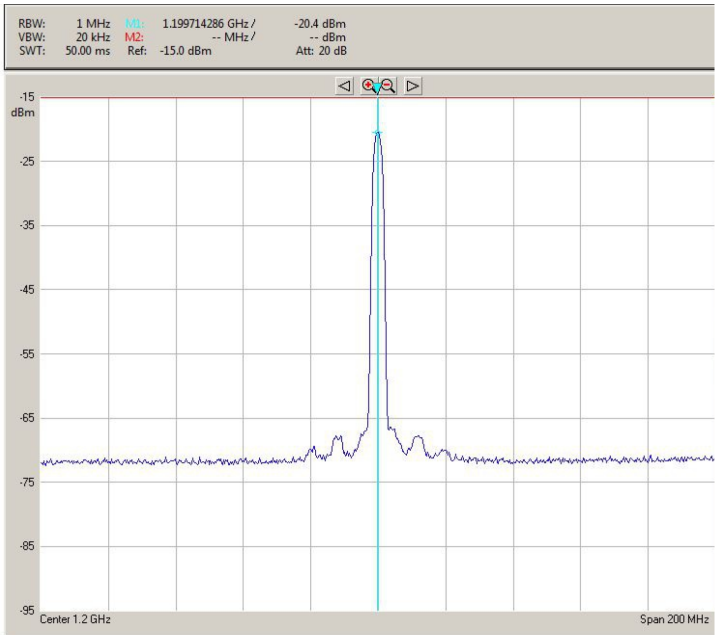
ComScope Window Sample: showing the modulated output waveform: blue for I-channel, red for Q-channel.



Output spectrum (after D/A conversion and RF modulation): 59.999 Mchips/s



Output spectrum (after D/A conversion and RF modulation): 30 Mchips/s



Output spectrum (after D/A conversion and RF modulation): 2 Mchips/s

Operation

Spreading codes

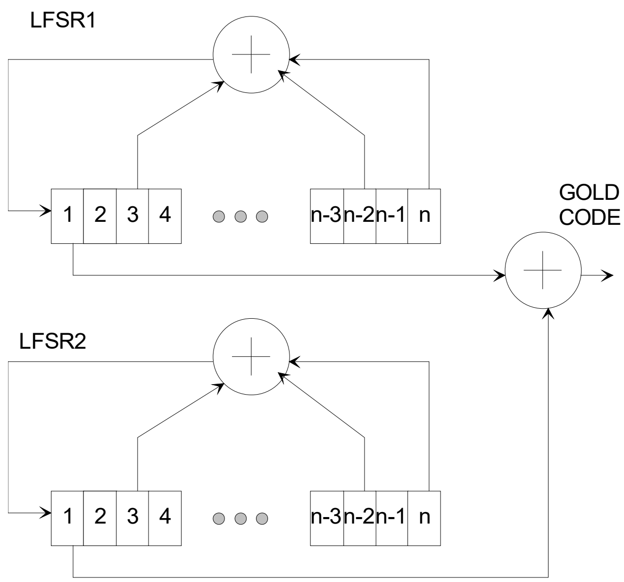
Spreading codes are pseudo random sequences which falls within the following categories:

- Gold sequences, for best autocorrelation properties
- Maximal length sequences
- Barker codes (length 11, 13)
- GPS C/A codes.

The same spreading code is used on both the in-phase (I) and quadrature (Q) channels.

Gold sequences

Gold sequences are generated using two linear feedback shift registers LFSR1 and LFSR2 as illustrated below:



The code period is 2^n-1, where n is the number of taps in the shift register. The LFRSa are initialized to all 1's at the start of each period. The LFRSs will generate all possible n-bit combinations, except the all zeros combination.

Each sequence is uniquely described by its two generator polynominals. The highest order is n. The generator polynominals are user programmable.

A few commonly used Gold sequences are listed below:

n = 5 (length 31):
$G1 = 1 + x^2 + x^5$ (0x000012)
$G2 = 1 + x + x^2 + x^4 + x^5$ (0x00001B)

n = 6 (length 63):
$G1 = 1 + x^5 + x^6$ (0x000030)
$G2 = 1 + x + x^4 + x^5 + x^6$ (0x000039)

n = 7 (length 127):
$G1 = 1 + x^3 + x^7$ (0x000044)
$G2 = 1 + x + x^2 + x^3 + x^4 + x^5 + x^7$ (0x00005F)

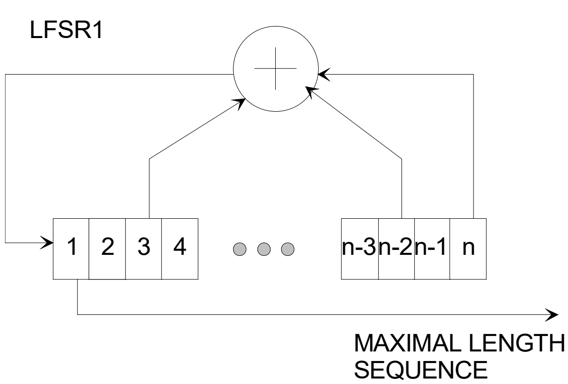
n = 9 (length 511):
$G1 = 1 + x^5 + x^9$ (0x000110)
$G2 = 1 + x^3 + x^5 + x^6 + x^9$ (0x000134)

n = 10 (length 1023):
$G1 = 1 + x^7 + x^{10}$ (0x000240)
$G2 = 1 + x^2 + x^7 + x^8 + x^{10}$ (0x0002C2)

n = 11 (length 2047):
$G1 = 1 + x^9 + x^{11}$ (0x000500)
$G2 = 1 + x^3 + x^6 + x^9 + x^{11}$ (0x000524)

Maximal length sequences

Maximal length sequences are generated using one linear feedback shift register LFSR1 as shown below:



The code period is 2^n-1, where n is the number of taps in the shift register. The LFRSa are initialized to all 1's at the start of each period. The LFRSs will generate all possible n-bit combinations, except the all zeros combination.

Each sequence is uniquely described by its generator polynominal. The highest order is n. The generator polynominal is user programmable.

A few commonly used maximal length sequences are listed below:

n = 4 (length 15):
$G1 = 1 + x + x^4$ (0x000009)
n = 5 (length 31):
$G1 = 1 + x^2 + x^5$ (0x000012)
n = 6 (length 63):
$G1 = 1 + x + x^6$ (0x000021)
n = 7 (length 127):
$G1 = 1 + x + x^7$ (0x000041)
n = 8 (length 255):
$G1 = 1 + x^2 + x^3 + x^4 + x^8$ (0x00008E)
n = 9 (length 511):
$G1 = 1 + x^4 + x^9$ (0x000108)
n = 10 (length 1023):
$G1 = 1 + x^3 + x^{10}$ (0x000204)

Barker Codes

11 bit Barker code: 101 1011 1000, or 0x5B8
13 bit Barker code: 1 1111 0011 0101, or 0x1F35

GPS C/A Codes

GPS C/A codes are modified Gold codes of length 1023 with generator polynomials:
$G1 = 1 + x^3 + x^{10}$
$G2 = 1 + x^2 + x^3 + x^6 + x^8 + x^9 + x^{10}$

The G2 generator output is slightly modified so as to create a distinct code for each satellite. The G2 output is generated by summing two specific taps of the shift register. In the case of Satellite ID 1 for example, taps 2 and 6 are summed.

The G2 output taps are listed below:

Satellite ID / GPS PRN Signal Number	G2 output taps selection	Satellite ID / GPS PRN Signal Number	G2 output taps selection
1	2 xor 6	21	5 xor 8
2	3 xor 7	22	6 xor 9
3	4 xor 8	23	1 xor 3
4	5 xor 9	24	4 xor 6
5	1 xor 9	25	5 xor 7
6	2 xor 10	26	6 xor 8
7	1 xor 8	27	7 xor 9
8	2 xor 9	28	8 xor 10
9	3 xor 10	29	1 xor 6
10	2 xor 3	30	2 xor 7
11	3 xor 4	31	3 xor 8
12	5 xor 6	32	4 xor 9

13	6 xor 7	33	5 xor 10
14	7 xor 8	34	4 xor 10
15	8 xor 9	35	1 xor 7
16	9 xor 10	36	2 xor 8
17	1 xor 4	37	4 xor 10
18	2 xor 5		
19	3 xor 6		
20	4 xor 7		

Compliant with "Navstar GPS Space Segment / Navigation User Interfaces" specifications, ICD-GPS-200, Revision C. IRN-200C-004, 12 April 2000.

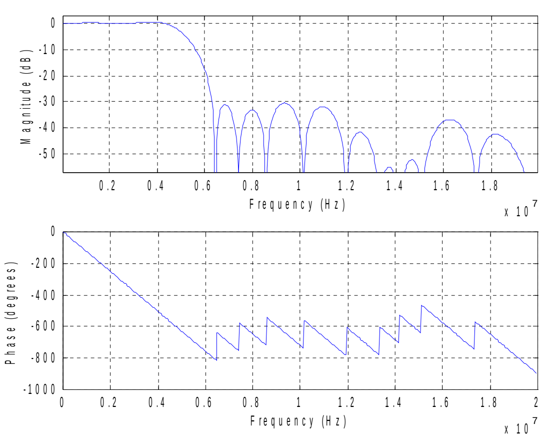
Data Rate

The symbol rate is set independently of the chip rate. In order to get the best spread-spectrum processing gain at the receiver, it is important to select a spreading code period of length greater or equal to the symbol period. In such cases, the processing gain is the ratio of symbol rate over chip rate.

Filter Response

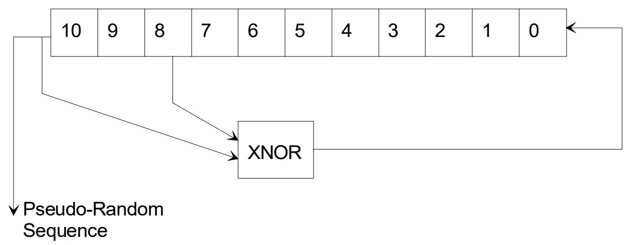
This module is configured at installation with a 20% rolloff filter.

Filter Response (20% rolloff)



Pseudo-Random Bit Stream (Test Pattern)

A periodic pseudo-random sequence can be used as modulator source instead of the input data stream. A typical use would be for end-to-end bit-error-rate measurement of a communication link. The sequence is 2047-bit long maximum length sequence generated by a 11-tap linear feedback shift register:



The first 100 bits of the PN sequence are as follows:
0000000000 0111111111 0011111110 0001111100 1100111000 0000010011 1111010001 1110110100 1101001100 0011000001

Interfaces

Several interface types are supported through multiple firmware options. All firmware versions can be downloaded from www.comblock.com/download.html

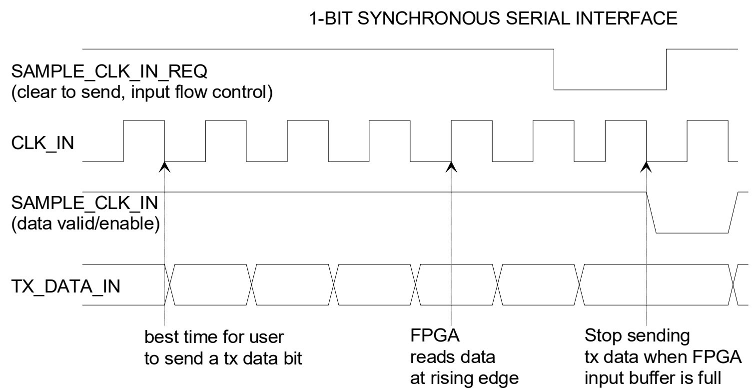
Changing the firmware option requires loading the firmware once using the ComBlock control center, then switching between the stored firmware versions The selected firmware option is automatically reloaded at power up or upon software command within 1.2 seconds

Option	DAC Type	Input
–A	2*10-bit unsigned (COM-2001) 26 Mchips/s max	USB or LAN (TCP-IP)
–C	2*16-bit signed (COM-3504) 60 Mchips/s max	USB or LAN (TCP-IP)
–G	2*12-bit signed (COM-2802) 30 Mchips/s max	USB or LAN (TCP-IP)
–D	2*10-bit unsigned (COM-2001) 26 Mchips/s max	USB or 1-bit synchronous serial
–H	2*12-bit signed (COM-2802) 30 Mchips/s max	USB or 1-bit synchronous serial

Inputs

1-bit synchronous serial

The input data stream can be injected through the left (J6) connector. The timing diagram is show below:



Maximum input clock rate: 125 MHz.

TCP-IP

The input data stream can also be transmitted over a TCP-IP network connection. This requires an additional COM-5102 plug-in Ethernet adapter. In this case, the modulator acts as a TCP server, waiting for connection from a remote client at port 1024. A static IP address is assigned by the user through the graphical user interface or control registers.

It is the client's responsibility to send enough data to the modulator so as to prevent underflow conditions. The client's strategy is thus to write data to a standard TCP socket as fast as possible and let the TCP protocol regulate the data flow.

At the modulator, received TCP bytes are sent serially, most-significant bit first.

USB

The input data stream can also be transmitted over a USB 2.0 cable, together with monitoring and control information. USB data transfer is only supported through the J1 HIGH-SPEED mini type AB connector. The other USB port labeled DEVelopment can be used for Monitoring and Control only. It cannot convey payload data.

This modulator acts as a USB device.

See
http://comblock.com/download/USB20_UserManual.pdf
for details.

Additive White Gaussian Noise (Test Mode)

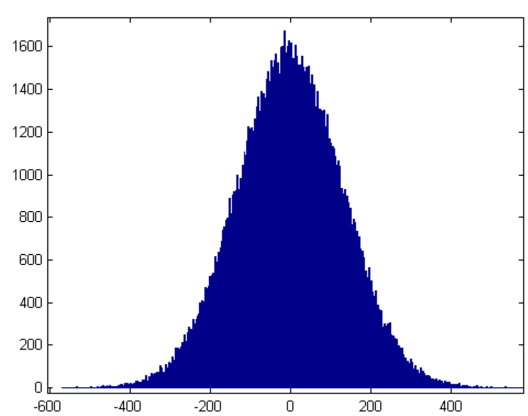
To help simulating link impairements, an accurate additive white Gaussian noise is digitally generated.

The AWGN has the following properties:

- random distribution up to +/- 4.5σ (4.5*standard deviation) .
- resolution: 16 bits
- periodicity greater than 2^{32} samples.
- bandwidth equals to twice the chip rate. Its wideband spectrum tends towards a sin(x)/x function but can be considered flat within the spread-spectrum bandwidth.

In order to help with the SNR calibration process, the noise power and the modulated signal power are measured and reported in the status registers.

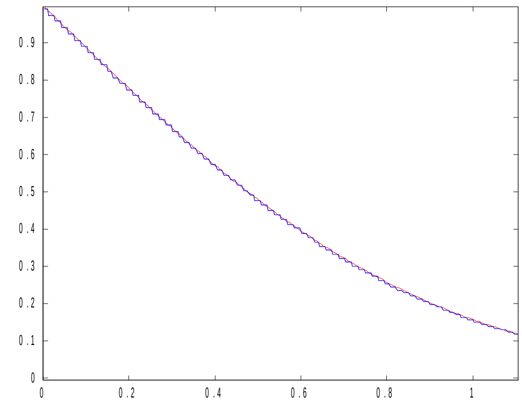
The resulting noise sample distribution is shown below:



Noise sample histogram (130K samples)

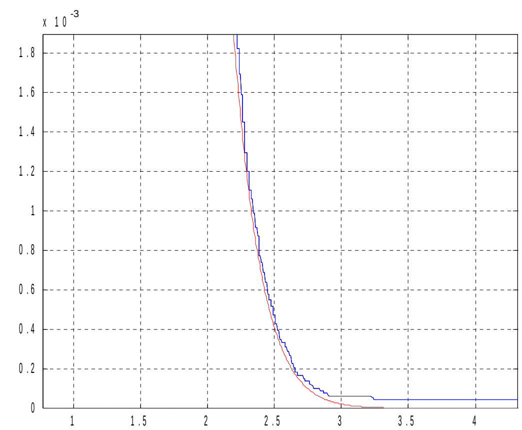
Mean = 0.
Standard deviation = 128

The plots below illustrate how accurate the noise generation is, by comparing the erfc function (red) with the AWGN normalized distribution (blue)



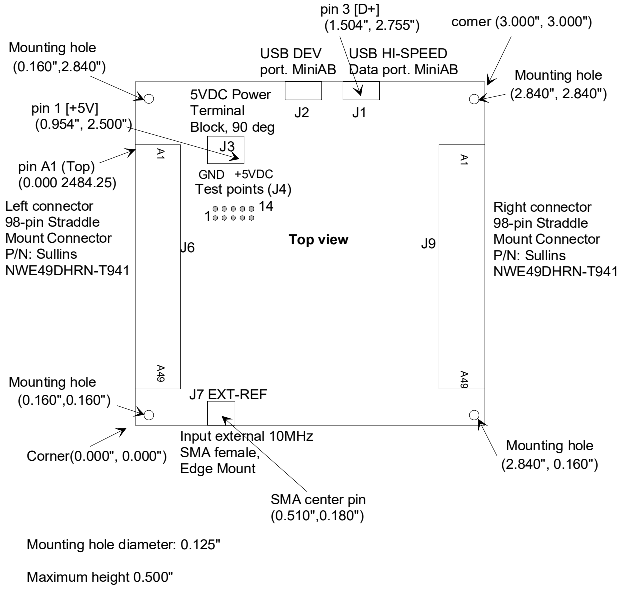
Theoretical erfc function (red) vs actual AWGN normalized distribution measurements (blue). Range 0 – 1, 130K samples.

The theoretical curve and the measured statistical distribution of noise samples are nearly superposed.



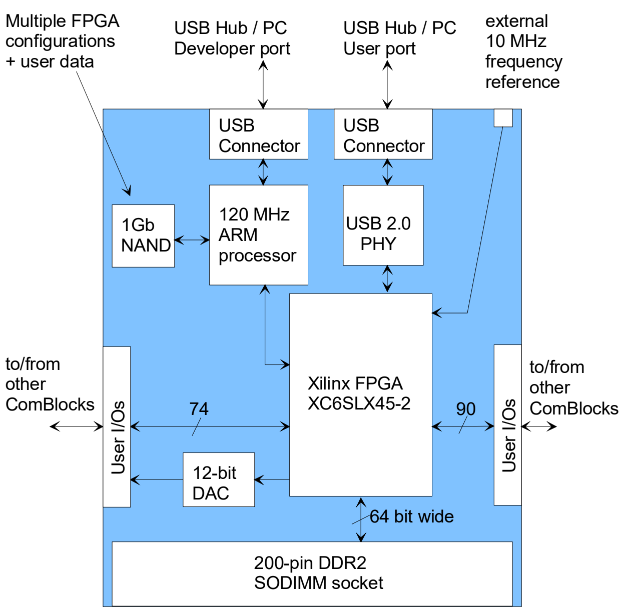
Theoretical erfc function (red) vs actual AWGN normalized distribution measurements (blue). Range 1-4, 130K samples.

Mechanical Interface



Schematics

The board schematics are available on-line at
http://comblock.com/download/com_1500schematics.pdf

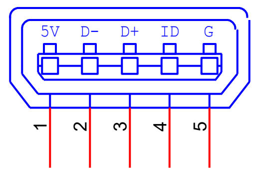


COM-1519 Hardware Block Diagram

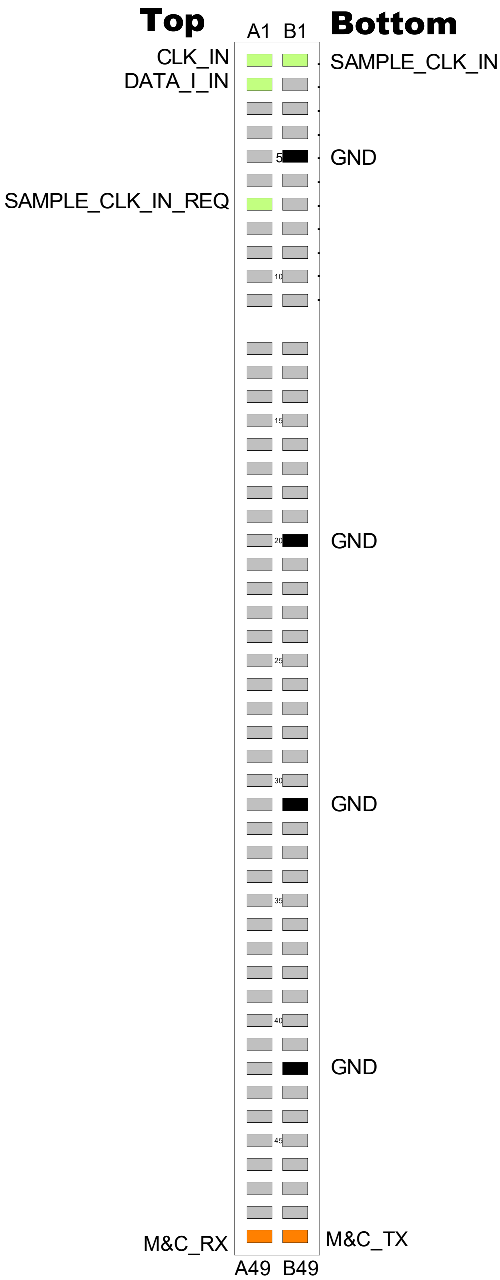
Pinout

USB

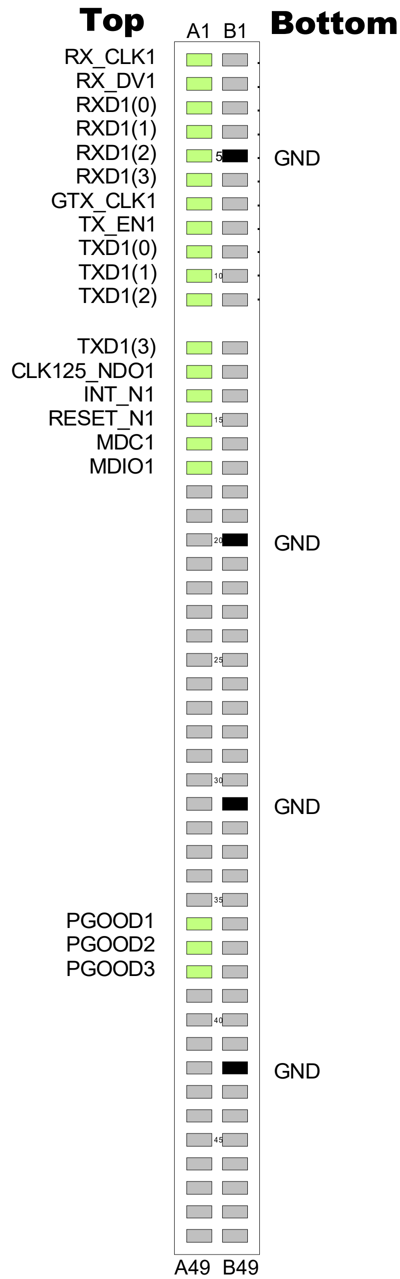
The USB port labeled HIGH-SPEED is equipped with a mini type AB connector. (G = GND).



Left Connector J6

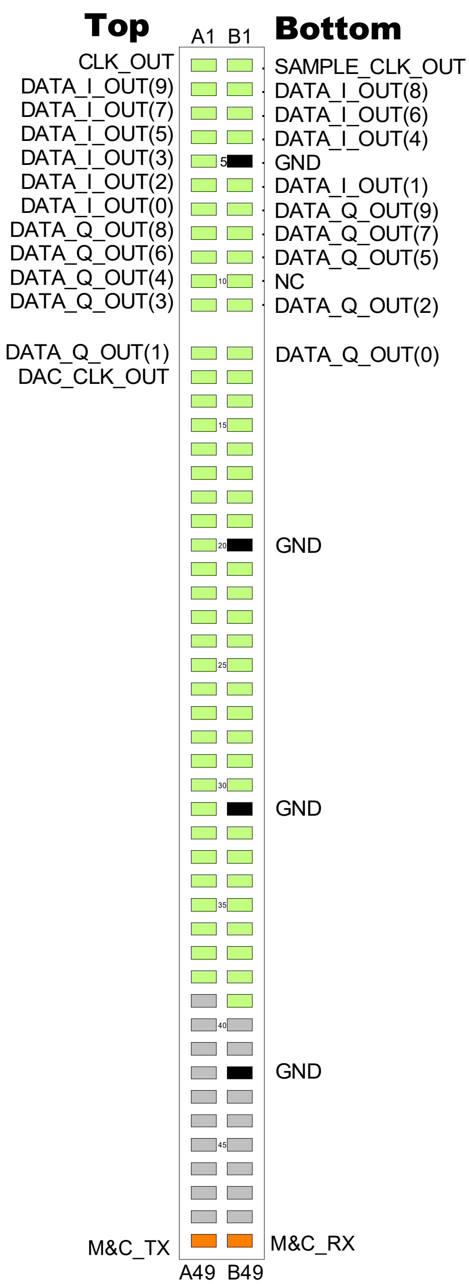


This interface is compatible with Comblock modules with 1-bit synchronous serial interface.
. **(–D, -H firmware)**

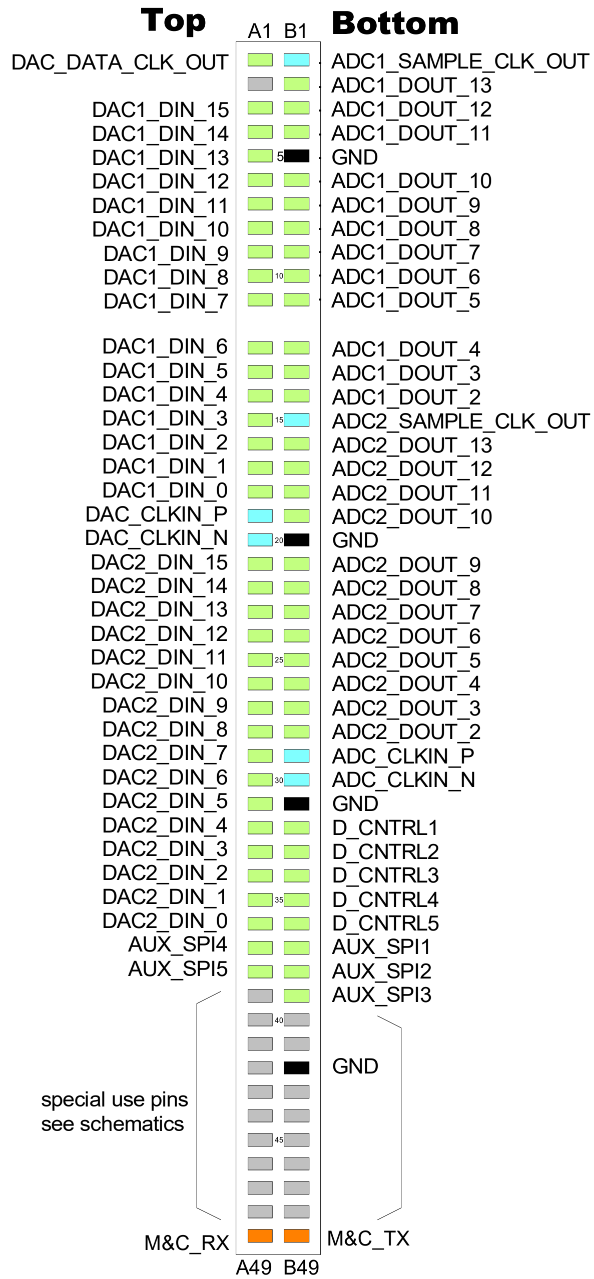


This interface is compatible with the COM-5102/COM-5401
10/100/1000 Mbps Ethernet PHY
. **(–A, -C firmware)**

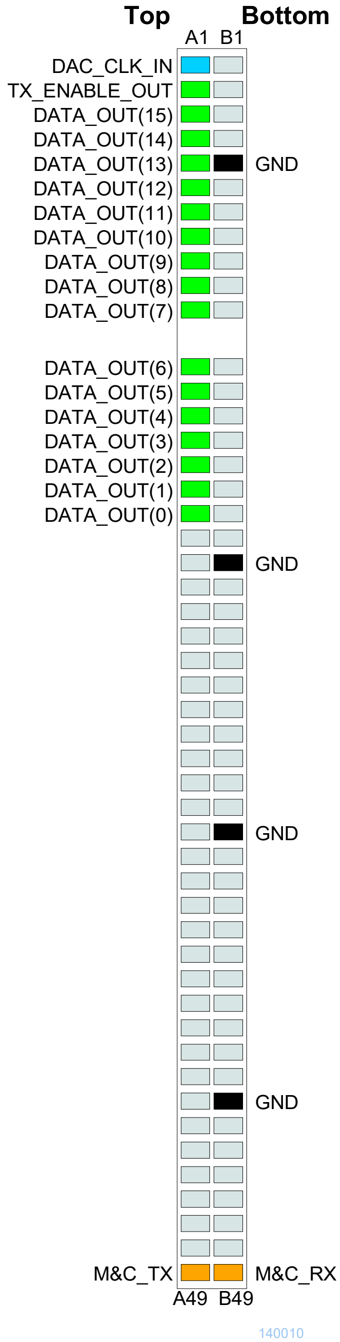
Right Connector J9



This interface is compatible with the COM-2001 dual DACs. **(–A, -D firmware)**



This interface is compatible with the COM-3504 dual Analog<->Digital Conversions.
(–C firmware)



This interface is compatible with the COM-2802 DDS modulator running at 480 MHz (x8 interpolation, 60 MSamples/s at baseband, 0 – 200 MHz IF out)
(–G, -H firmware)

I/O Compatibility List

(not an exhaustive list)

Left connector
COM-5102 Gigabit Ethernet + HDMI interface
COM-1500 FPGA + ARM development platforms
COM-1509 Error correction codec
COM-7002 Turbo Code Error correction encoder
COM-8001 Arbitrary waveform generator 256MB
COM-5003 TCP-IP / USB Gateway
COM-5404 IP router
Right connector
–A, -D firmware
COM-2001 digital-to-analog converter (baseband).
COM-1518 DSSS Demodulator 60 Mchips (back to back)
COM-1524 Channel emulator (Doppler, delay, fading, noise)
–C firmware
COM-3504 Dual Analog <-> Digital Conversions
–G, -H firmware
COM-2802 DDS modulator

Configuration Management

This specification document is consistent with the following software versions:

- COM-1519 FPGA firmware: Version 6 and above.
- ComBlock Control Center graphical user interface: Revision 3.08n and above.

The option and version of the FPGA configuration currently active can be read from the ComBlock Control Center in the configuration panel (advanced).

ComBlock Ordering Information

COM-1519
Direct-sequence spread-spectrum modulator 60 Mchips/s.

ECCN 5A001.b.3

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