COM-1600
FPGA + ARM + USB2 + DDR2 + NAND DEVELOPMENT PLATFORM

Key Features

- Powerful digital signal processing platform comprising
  - Spartan-6 (XC6SLX16-2) FPGA for parallel computing
  - ARM 32-bit co-processor @120MHz (LPC1759) for complementary sequential computing[1]
  - 1Gbit 16-bit wide DDR-2 memory to complement FPGA's memory. 4 Gbits/s sustained read or write throughput.
  - 1Gbit NAND for non-volatile storage of 8 FPGA configurations and user data
- High-speed connectivity:
  - Two USB 2.0 connections:
    - High-speed (480 Mbits/s) connection through FPGA
    - Full-speed (12-Mbits/s) connection through ARM processor
  - 74 differential LVDS connections
  - 4-port 10/100/1000 Ethernet connections (requires COM-5401)
  - Input for an external higher-stability 10 MHz frequency reference.
- The COM-1600 is compatible with a comprehensive development environment of industry-standard free tools:
  - Xilinx ISE WebPACK for development from VHDL or Verilog source code to FPGA binary. [free]
  - Eclipse IDE + GNU ARM toolchain from C/C++ source code to ARM binary. [free]
  - ComBlock flashloader to program the FPGA and ARM binaries into the board non-volatile flash memory over USB. [included]
  - Optional JTAG USB pod (for ARM in-circuit debugging)
- The COM-1600 is interface-compatible with numerous other ComBlock modules (RF, Analog, Network, modem, error correction) via standard high-speed 98-pin PCIe connectors.
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.

[1] Use of the ARM processor is at the user's discretion. The ARM processor is pre-programmed with all basic functions.

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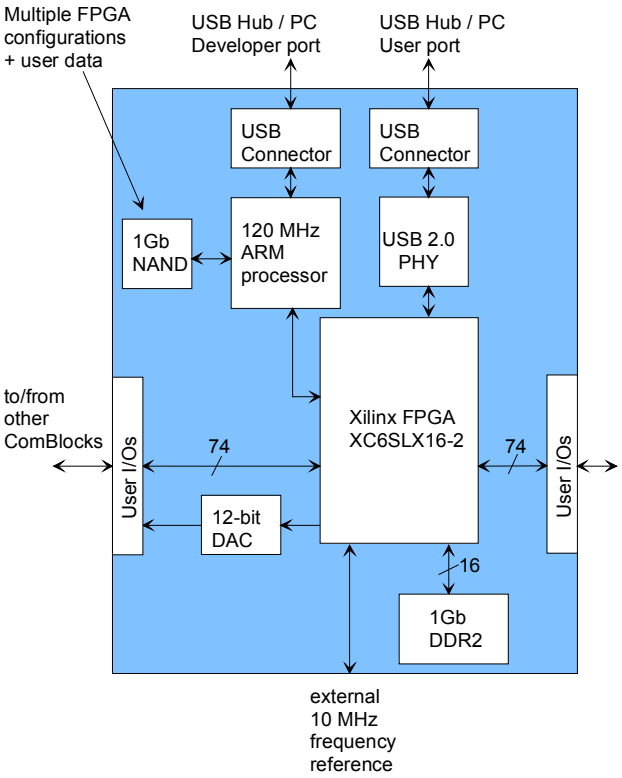
For the latest data sheet, please refer to the **ComBlock** web site: comBlock.com/com1600.html.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to ComBlock.com/product_list.html.



COM-1600 Hardware Block Diagram

Nominal Operation

Supply voltage	+4.9 to +5.5 VDC

Absolute Maximum Ratings

Supply voltage	-16V min, +16V max
98-pin connector inputs	-0.5V min, +3.6V max

Simple Development Setup

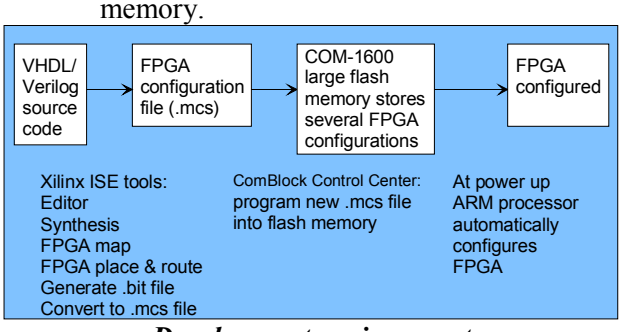
The COM-1600 is designed to simplify the development setup and yet allow unrestricted access to all hardware features.

- Simply connect a USB cable between the COM-1600 USB development port and a PC. No power supply needed.
- Install the ComBlock Control Center software for monitoring, control and programming.
- Download and install the free industry-standard tools for FPGA and optional ARM development.
- Download the source code templates from www.comblock.com/download.html

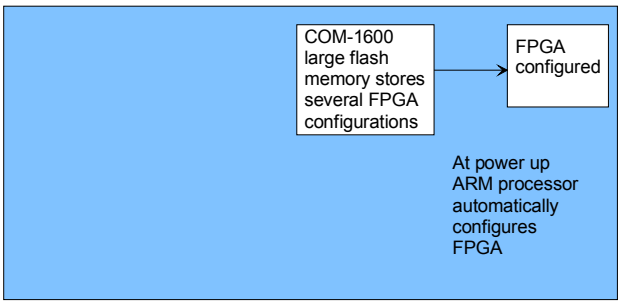
Getting Started with FPGA Development

Developing a custom FPGA-based application requires six key steps:

1) The user writes VHDL or Verilog source code.
2) The Xilinx synthesis tool (XST), part of the Xilinx Integrated Software Environment (ISE) design suite, converts the source code into hardware primitives (.ngc file)
3) The constituent .ngc files are then mapped into the target FPGA and net routing takes place, again under the supervision of the Xilinx ISE. The output is a binary .bit file.
4) The Xilinx iMPACT tool reformat the .bit file into a .mcs PROM file.
5) The ComBlock Control Center programs the .mcs file into the board non-volatile (flash) memory.
6) At power-up, the ARM processor configures the FPGA using the designated .mcs configuration file stored on the flash memory.



Development environment



Run-time environment

Any new FPGA design should start with the VHDL template project which includes drivers and the framework for remote monitoring and control using the ComBlock Control Center.

Getting Started with ARM Development

Writing code for the ARM co-processor is *optional*. The ARM processor is factory programmed with the full set of functions described in this document. In many application cases, the processor could be left as is.

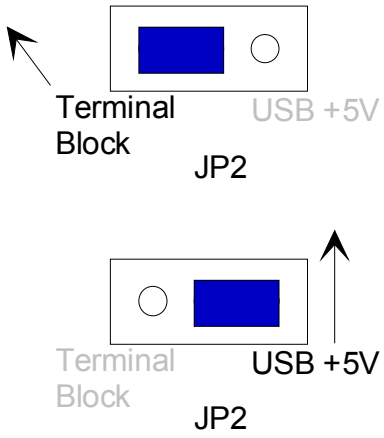
However, since the processor resources are significantly underutilized after the initial configuration, it is made available for developers to implement additional digital signal processing algorithms.

The ARM co-processor code template is available for download at www.comblock.com/download.html#Latest_ARM_firmware

Operations

Power

The COM-1600 can be powered through the USB (DEVelopment port) or through the green terminal block. Selection is by way of the JP2 jumper located near the terminal block.



Power entry selection

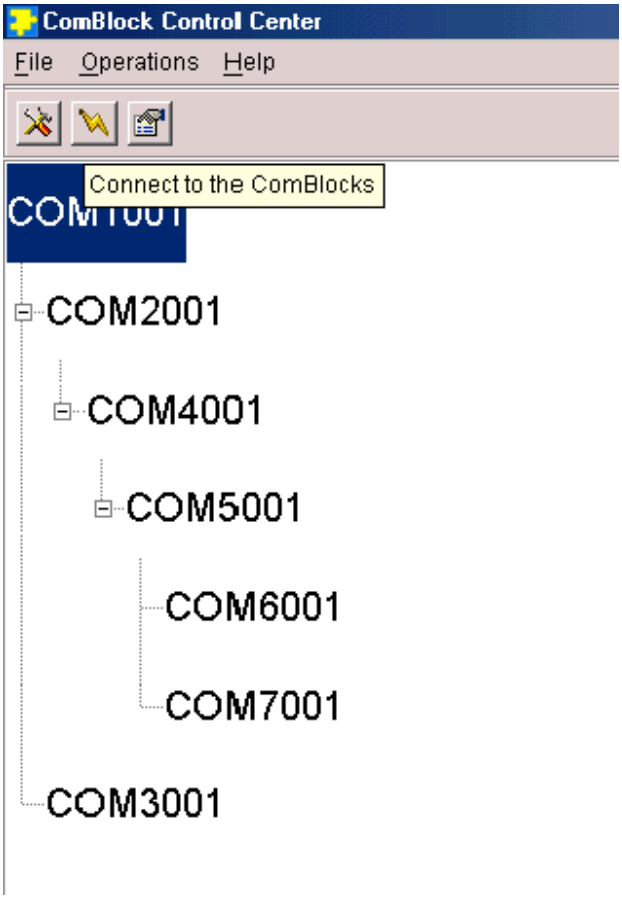
Graphical User Interface

A user-friendly graphical user interface (hereafter named ComBlock Control Center) is supplied with the COM-1600. The ComBlock Control Center runs on any Windows PC (running XP or above). It allows the user to communicate with the COM-1600 over the USB 2.0 interface and when other ComBlocks are connected, via serial link, LAN or PCMCIA/Cardbus.

The primary use of the ComBlock Control Center is to:

(a) Download new FPGA firmware (into non-volatile Flash memory)
(b) Set control registers
(c) Monitor status registers
(d) Capture and display internal signals (ComScope)

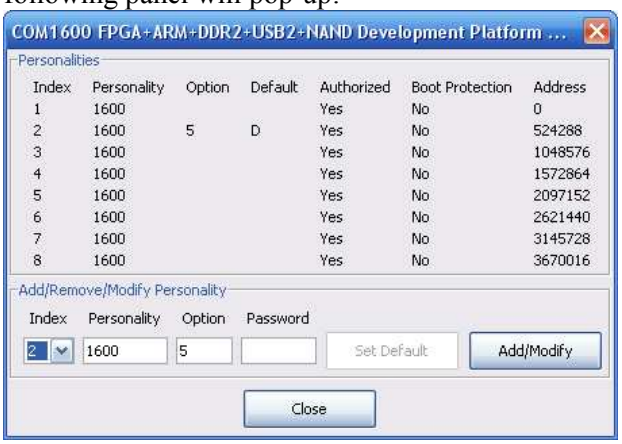
When activated, the ComBlock Control Center detects the ComBlock modules within the assembly. The modules are identified by their name in a tree-like structure. Each module can be configured and monitored remotely.



The ComBlock Control Center software is provided with all ComBlock modules. The user's manual can be found at ComBlock.com/download/ccchelp.pdf.

Flash Memory

The FPGA configurations are stored in the COM-1600 non-volatile (Flash) memory. The ComBlock Control Center includes the utility to (re)write the FPGA .mcs file into the flash memory over USB. Upon clicking on the  button the following panel will pop-up:



From this panel, one can select the default personality index and program the FPGA .mcs configuration file into the board flash memory.

Instructions on how to generate a .mcs formatted file from a Xilinx .bit file are available here:

The COM-1600 Supports **multiple personalities** and **dynamic reconfiguration**:

- Up to 8 FPGA configurations can be stored in non-volatile flash memory. Programming a new FPGA configuration into the on-board flash memory via USB takes 11 seconds.
- The selected configuration is automatically reloaded at power up or upon software command within 0.5s.

USB

The COM-1600 comprises two USB ports labeled USB HI SPEED and DEV/+5V. The development port is the recommended port for flash programming, as it does not depend on the FPGA being properly configured. The USB data port could be inaccessible in the case of an invalid FPGA configuration.

A driver must be installed prior to using USB to communicate with ComBlocks for the first time. In summary, connect the ComBlock to power and a Windows OS PC via USB, then go to the Control Panel | Device Manager and add the driver by pointing to the driver located in the CD-ROM /Windows Drivers/USB 2.0/Windows Driver folder. Detailed instructions are available in the USB user manual www.comblock.com/download/USB20_UserManual.pdf

Accidental FPGA file corruption

The COM-1600 is protected against corruption by an invalid FPGA configuration file. To recover from such occurrence, connect a jumper in JP1 position 2-3 prior and during power-up. The COM-1600 will be automatically configured with a default FPGA configuration. This boot file is un-erasable. Once this is done, the user can safely re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center GUI.

DDR2 SDRAM

A 1 Gbit DDR2 memory is directly connected to the FPGA. The memory controller (.ngc file) is supplied. It is capable of a sustained throughput (read or write) of 4 Gbits/s. The user manual can be downloaded from www.comblock.com/download/DDR2soft.pdf.

Alternatively, the user can make use of the hardware-based memory controller. See Xilinx user guide UG388 "Spartan-6 FPGA Memory Controller".

Analog I/Os

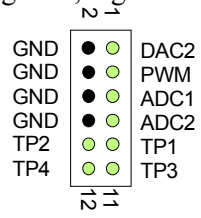
The COM-1600 includes multiple ADCs and DACs as listed below:

Function	Precision	Speed	Under control by
DAC1	12-bit	1 MS/s	FPGA
DAC2	10-bit	TBD	ARM
PWM	10-bit	TBD	ARM
ADC1	12-bit	100KS/s	ARM
ADC2	12-bit	100KS/s	ARM

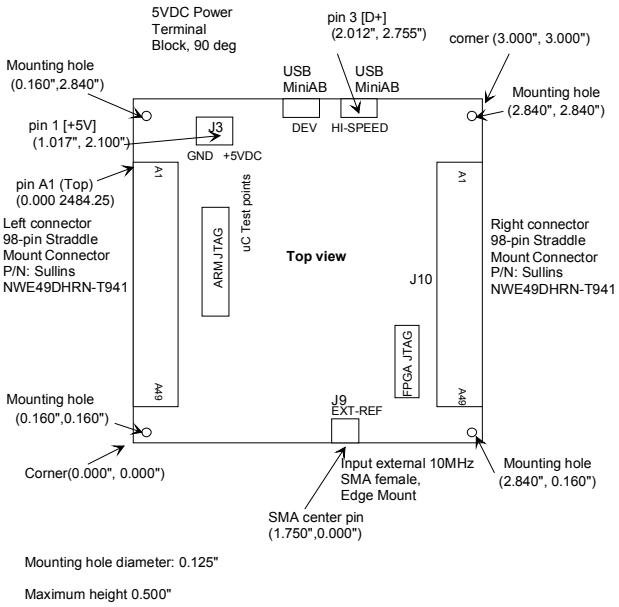
Most of these signals are accessible through a 12-pin header.

ARM Co-processor Test Points

A 12-pin header (J4) is provided for easy access to several key analog I/Os, digital I/Os and interrupt.



Mechanical Interface



Schematics

The board schematics are available on-line at ComBlock.com/download/com_1600schematics.pdf

VHDL code template

A VHDL template project is available from the ComBlock CD or on-line at ComBlock.com/download/com1600_000.zip
The template project includes:

- the VHDL source code (.vhd)
- the constraint file (.ucf) listing all pin assignments
- The Xilinx ISE project with the synthesis and implementation settings
- The resulting bit file (.mcs) is ready to be loaded into flash memory

The sample code describes how the application interfaces with the ComBlock Control Center graphical user interface through control and monitoring registers. Monitoring and control messages and syntax are described in ComBlock.com/download/m&c_reference.pdf.

It also describes how to capture key internal signals in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The ComScope user manual is available at ComBlock.com/download/Comscope.pdf.

Finally, the code template includes the following binary (.ngc) drivers:

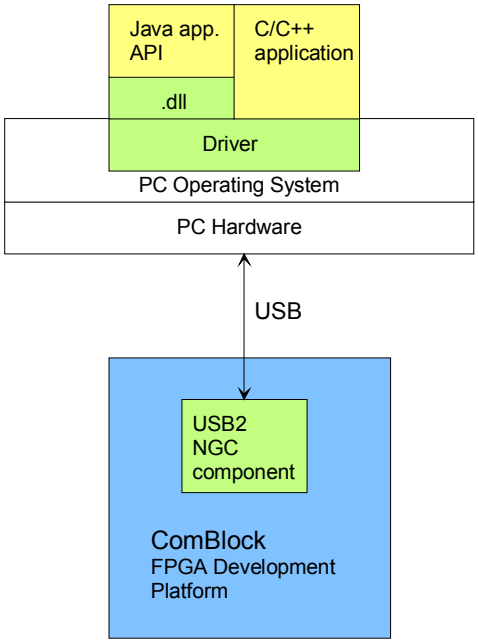
- DDR2 driver
- 12-bit auxiliary DAC driver
- USB 2.0 driver
- Tri-mode 10/100/1000 Mbps Ethernet MAC

USB 2.0 Driver

Software to help developers create USB high-speed communications between the COM-1600 platform and a host PC is provided. The **USB 2.0 software package** includes the following:

- USB20 NGC component for integration within the VHDL code.
- VHDL top-level code template
- Windows device driver (.sys, .inf files)
- Java API, .dll and application sample code
- C/C++ application sample code

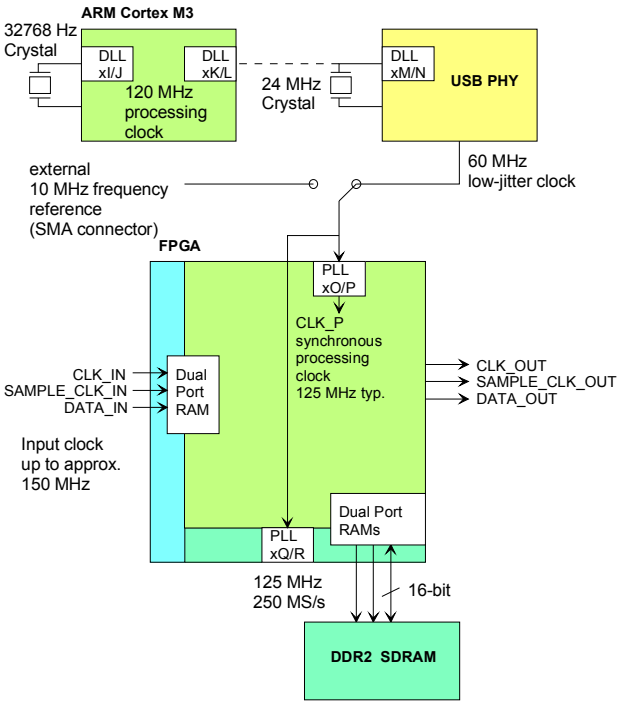
The **USB 2.0 software package** is available in the ComBlock CD and can also be downloaded from ComBlock.com/download/usb20.zip.
The user manual is available at ComBlock.com/download/USB20_UserManual.pdf



Blue: supplied hardware
Green: supplied ready-to-use software
Yellow: source code examples

Clock Architecture

The clock distribution scheme embodied in the COM-1600 is illustrated below.



The FPGA internal frequencies are locked onto a single 24 MHz crystal oscillator. This oscillator (part of the USB PHY) serves as reference for the 60 MHz USB PHY interface clock, and the 125 MHz FPGA clocks.

A 32.768 KHz crystal is the primary frequency reference for the 120 MHz ARM processor clock (thus allowing very low-power operation). Alternatively, the 24 MHz crystal oscillator can also serve as frequency reference after modifying the ARM processor software.

The VHDL code template generates the following FPGA clocks:

- 125 MHz processing clock
- 125 MHz DDR2 interface clock

The internal reference clock frequency stability is typically in the range [-100, 0] ppm.

Other clock architectures and frequencies are possible by changing the FPGA source code. For example, in applications requiring a higher frequency accuracy, the FPGA code can be written to select a user-supplied ultra-stable 10 MHz frequency signal as its frequency reference.

I/O Standards

The digital signals on connectors J6 and J10 are LVTTL (0 – 3.3V) single-ended signals by default. However, the I/O types can be easily changed by software to other types such as differential LVDS_33.

See Xilinx user guide ug381 for details.

Digital to Analog Converter (DAC)

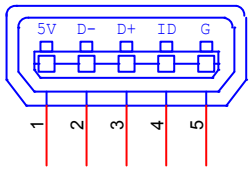
A 12-bit DAC/Analog output is built-in for gain control. The DAC operates under the direct control of the FPGA The DAC output is connected to pin "B13" of the J6 connector. The DAC can be disabled in software to a high impedance state or physically disabled by removing the 0Ω R51 resistor.

The DAC can typically operate at a 0.5V/µsec slew rate. The output voltage range is from 0 to 3.3 V. The driver provided in the code template allows for approximate refresh rate of up to 1.765 MHz (slew rate limited.)

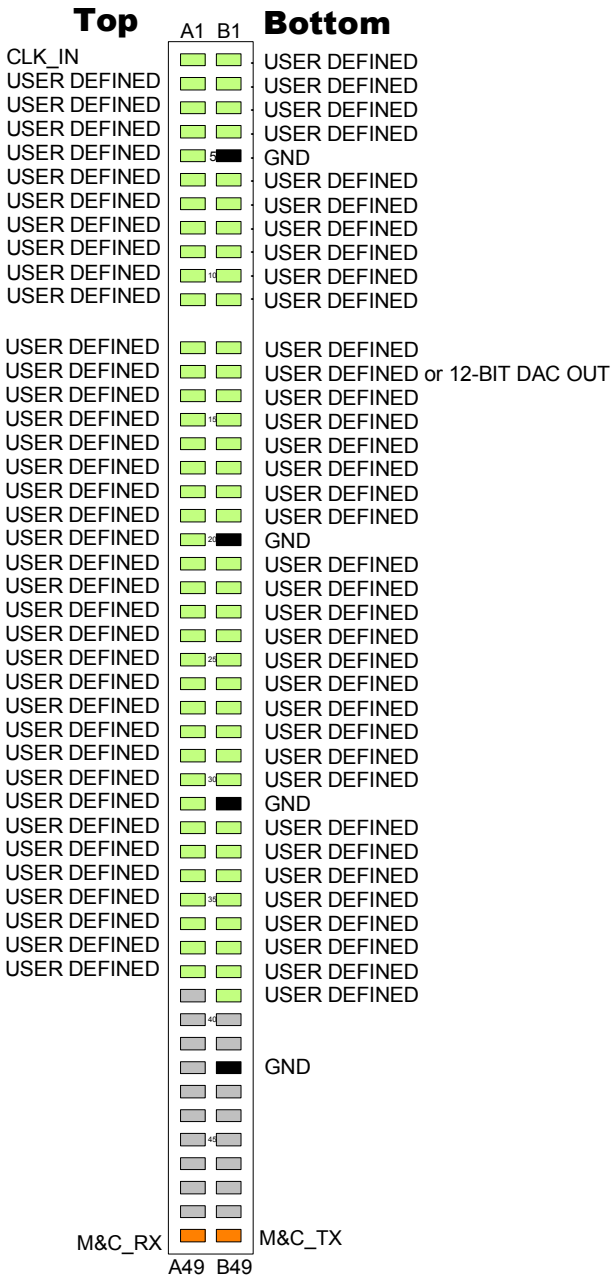
Pinout

USB

Both USB ports are equipped with mini type AB connectors. (G = GND). In both cases, the COM-1600 acts as a USB device.

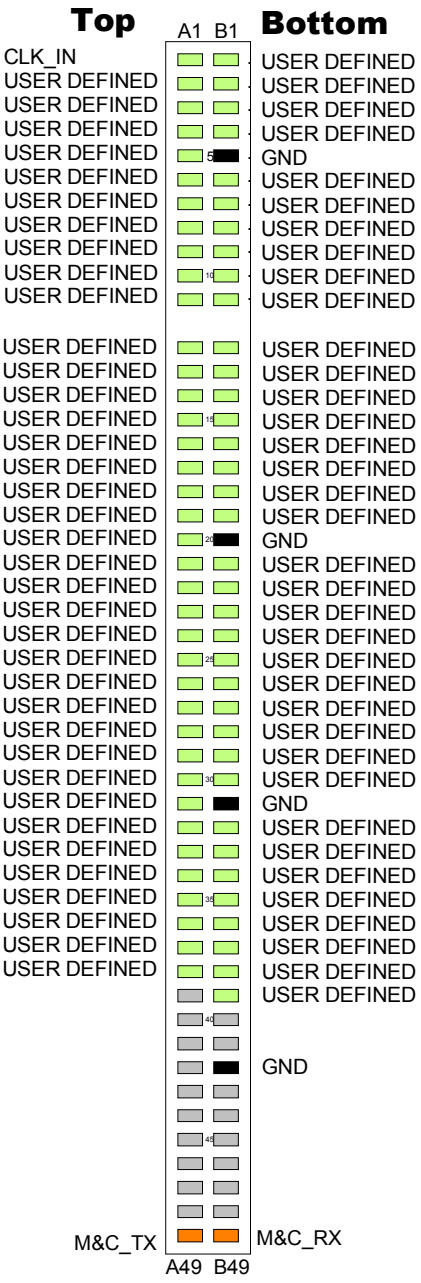


Left Connector J6



98-pin to 40-pin adapters to interface with other Comblocks are supplied free of charge. Please let us know about your interface requirements at the time of order.

Right Connector J10



Compatibility List

(Not an exhaustive list)

Compatible modules
COM-3002/3/4/5/6/7/8/9/10 RF/IF/Baseband receivers.
COM-2802 Synchronized 8-channel 900 MSamples/s Digital-to-Analog conversion
COM-3504 Dual Analog <-> Digital Conversions
COM-1600/1500 FPGA + ARM development platforms
COM-5401 4-port 10/100/1000 Mbps Ethernet Transceivers
Software
COM-5401SOFT Tri-mode 10/100/1000 Mbps Ethernet MAC, VHDL source code

ComBlock Ordering Information

COM-1600 FPGA (Spartan-6 LX16) + ARM + USB2 + DDR2 + NAND development platform

ARM-USB-OCD JTAG debugger (optional)

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