COM-1700 LOW-POWER SDR DEVELOPMENT PLATFORM
40-700 MHz IF receive / baseband transmit

Key Features

- Low-power (2W typ.) signal processing platform comprising:
  - Large Xilinx Spartan-6 (XC6SLX45-L1) FPGA for massive parallel computing
  - ARM 32-bit co-processor @120MHz (LPC1759) for complementary sequential computing[1]
  - 1Gbit NAND for non-volatile storage of numerous FPGA configurations and user data.
- Analog/IF interface:
  - Input option **–A**: dual I/Q baseband, 2Vpp differential.
  - Input option **–B**: 70 MHz IF input: -50 to +5 dBm, 50 Ohm, 20 MHz bandwidth.
  - Input option **–C**: 140 MHz IF input: -50 to +5 dBm, 50 Ohm, 20 MHz bandwidth.
  - Customizable receive IF center frequency (up to 700 MHz) and filter bandwidth (up to 20 MHz). Please contact us for a quotation.
  - Outputs: dual I/Q baseband outputs, 1Vpp differential
  - 80 MSamples/s 10-bit ADCs
    125 MSamples/s 12-bit DACs
- High-speed connectivity:
  - Gigabit Ethernet LAN
  - Two USB 2.0 connections:
    - High-speed (480 Mbits/s) connection through FPGA
    - Full-speed (12-Mbits/s) connection through ARM processor
  - 76 LVTLL or 38 differential LVDS connections
  - RS-422 (4 Tx/4 Rx)
  - Input for an external, higher-stability frequency reference.
- Frequency reference: internal TCXO or external frequency reference via UMCC [2]connector, selectable by solder bridge.

[1] Use of the ARM processor is at the user's discretion. The ARM processor is pre-programmed with all basic functions.

[2] Ultra Miniature Coaxial Connector.

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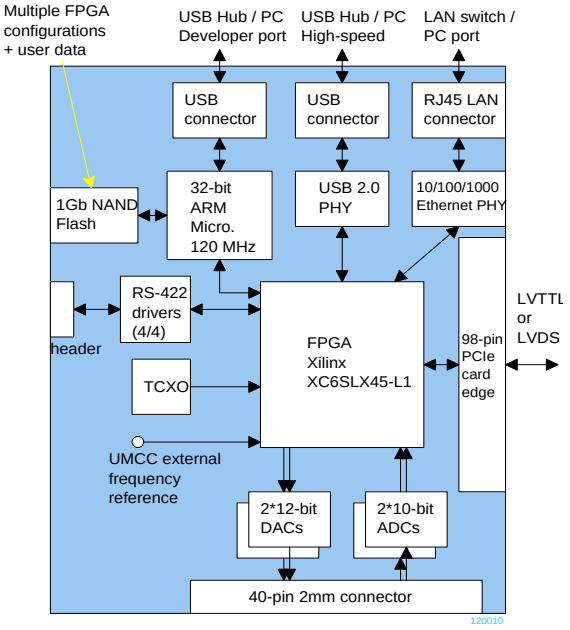
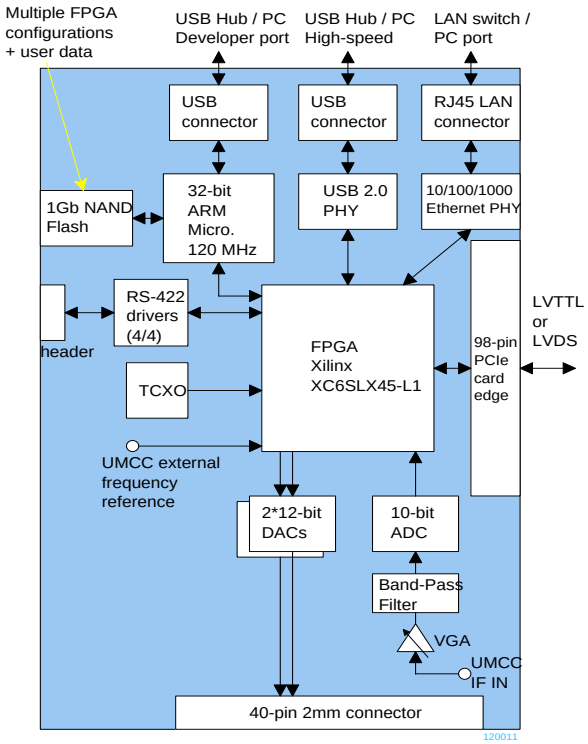
- The COM-1700 is compatible with a comprehensive development environment of free industry-standard tools:
    - Xilinx ISE Webpack for development from VHDL or Verilog source code to FPGA binary [from Xilinx]
    - Eclipse IDE + GNU ARM tool chain from C/C++ source code to ARM binary [from yagarto.de]
    - ComBlock flashloader to program the FPGA and ARM binaries into the board non-volatile flash memory over USB. [included]
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.

For the latest data sheet, please refer to the **ComBlock** web site: comblock.com/com1700.html.
These specifications are subject to change without notice.



COM-1700 (Option –A Hardware Block Diagram



COM-1700 (Options –B/C Hardware)

Nominal Operation

Supply voltage	+4.9 to +5.5 VDC unregulated, or +3.0 to +3.6V regulated depending on hardware configuration.
ADCs inputs	2Vpp differential (1Vpp single-ended) max. Input common mode: 0.5 to 1.3V recommended.
DACs output	2Vpp differential (1Vpp single-ended) Output common mode: 0.5V
IF input	-50 to +5 dBm for maximum ADC range. 50 Ohm input impedance.

Absolute Maximum Ratings

Supply voltage (when configured for +5V unregulated)	-16V min, +16V max
Supply voltage (when configured for +3.3V regulated)	-0.5V min, +3.6V max
98-pin connector inputs	-0.5V min, +3.6V max
ADCs inputs	-0.3 to 2.1V single-ended

Getting Ready

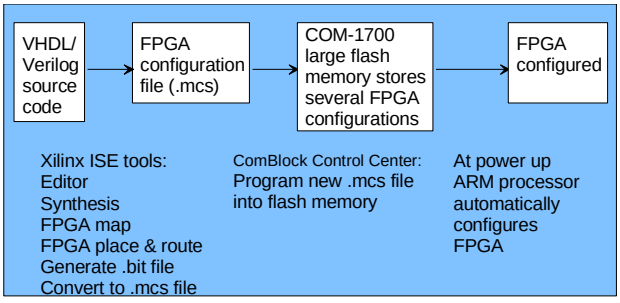
The COM-1700 is designed to simplify the development setup and yet allow unrestricted access to all hardware features.

- Connect a +5VDC (or 3.3V depending on hardware configuration) supply to the green terminal block.
- Install the ComBlock Control Center software on a PC for monitoring, control and programming FPGA configurations.
- Install the industry-standard tools for FPGA and optional ARM development on a PC.
- Download the source code templates from www.comblock.com/download.html

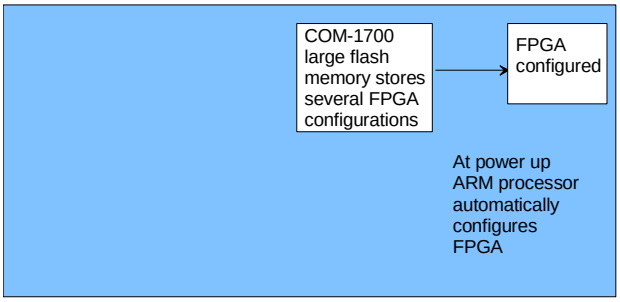
FPGA Development Steps

Developing a custom FPGA-based application requires six key steps:

1) The user writes VHDL or Verilog source code.
2) The Xilinx synthesis tool (XST), part of the Xilinx Integrated Software Environment (ISE) design suite, converts the source code into hardware primitives (.ngc file).
3) The constituent .ngc files are then mapped into the target FPGA and net routing takes place, again under the supervision of the Xilinx ISE. The output is a binary .bit file.
4) The Xilinx iMPACT tool reformats the .bit file into a .mcs PROM file.
5) The ComBlock Control Center programs the .mcs file into the board non-volatile (flash) memory.
6) At power-up, the ARM processor configures the FPGA using the designated .mcs configuration file stored on the flash memory.



Development environment



Run-time environment

ARM Development Steps

Writing code for the ARM co-processor is *optional*. The ARM processor is factory programmed with the full set of functions described in this document. In many application cases, the processor could be left as is.

However, since the ARM processor resources are significantly underutilized after the initial configuration, it is made available for developers to implement additional digital signal processing algorithms or customize the power profile.

Operations

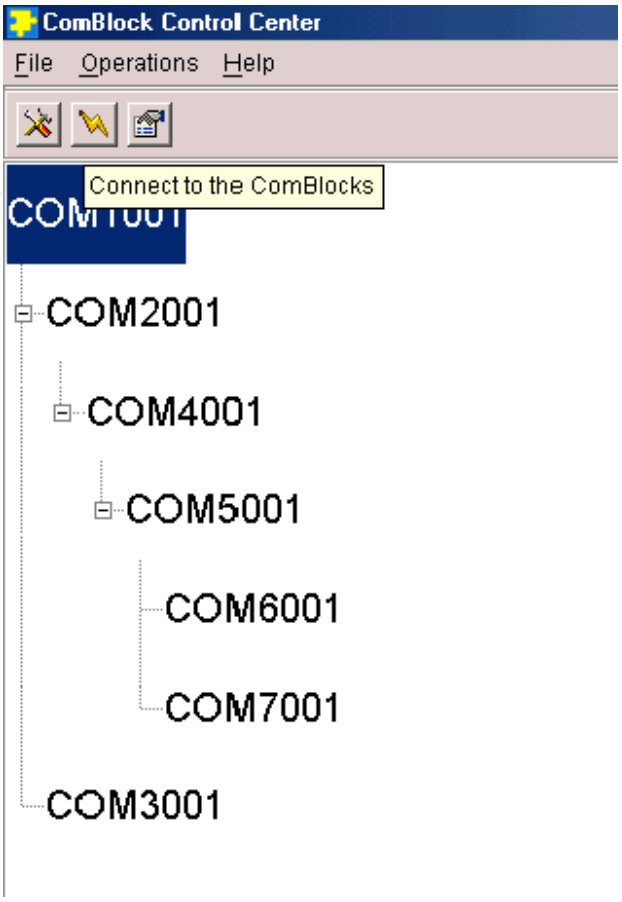
Graphical User Interface

A user-friendly graphical user interface (hereafter named ComBlock Control Center) is supplied with the COM-1700. The ComBlock Control Center runs on any Windows PC. It allows the user to communicate with the COM-1700 over the USB 2.0 interface, LAN or through adjacent ComBlocks.

The primary use of the ComBlock Control Center is to:

(a) Download new FPGA firmware (into non-volatile Flash memory)
(b) Set control registers
(c) Monitor status registers
(d) Capture and display internal signals (ComScope).

When activated, the ComBlock Control Center enumerates the ComBlock modules within the assembly. The modules are identified by their name in a tree-like structure. Each module can be configured and monitored remotely.



The ComBlock Control Center software is provided with all ComBlock modules. The user's manual can be found at www.comblock.com/download/ccchelp.pdf.

Flash Memory

The FPGA configurations are stored in the COM-1700 non-volatile (NAND Flash) memory. The ComBlock Control Center includes the utility to (re)write the FPGA .mcs PROM file into the flash memory over USB or LAN. Click on the  button and follow the instructions.

The COM-1700 Supports **multiple personalities** and **dynamic reconfiguration**:

- Up to 8 FPGA configurations can be stored in non-volatile flash memory.
- The selected configuration is automatically reloaded at power up or upon software command within 2 seconds.

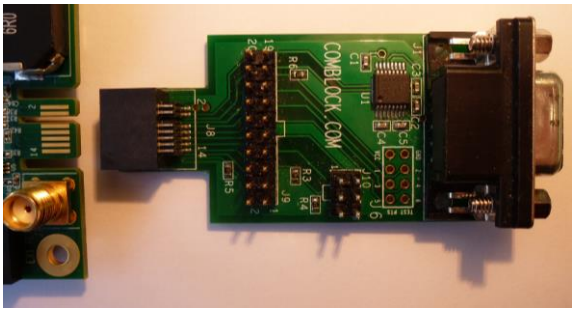
The COM-1700 comprises two USB ports labeled DATA and J7. The development port J7 is the recommended port for flash programming, as it does not depend on the FPGA being properly configured. The USB DATA port could be inaccessible in the case of an invalid FPGA configuration.

FPGA JTAG

The FPGA can also be programmed through the 14-pin J8 JTAG connector. This method requires a special programming cable (such as the Xilinx platform cable USB II DLC-10). Please note that such cable does not allow programming of the board NAND flash.

ARM Programming

The ARM microcontroller can be programmed in two ways, both requiring an external adapter (not included) to keep the board size small. The adapter (model Y03007R4) includes a standard 20-pin ARM JTAG connector and a RS-232 DB9 connector. The latter, when used in conjunction with the flashmagictool.com tool, is a fast and reliable way to program the ARM controller flash memory with a new executable file.



Optional adapter for programming the flash-based microprocessor via serial link to a PC, or through a 20-pin ARM JTAG pod.

Power Supply

The board can be powered by unregulated +5VDC supply or regulated +3.3V DC. The selection is made by the R60/R61 solder bridge below the J3 terminal block. The board is shipped for operation at +5VDC by default.

When powered by unregulated +5VDC supply, the board includes over-voltage, reverse voltage and surge protections as well as voltage regulation. No such protections exist when powered by regulated +3.3VDC.

Supply is through the J3 3.81mm pitch pluggable terminal block.

USB

The COM-1700 comprises two USB ports labeled USB DATA and J7. The development port (J7) is the recommended port for flash programming, as it does not depend on the FPGA being properly configured. The USB high-speed data port (USB DATA) could be inaccessible in the case of an invalid FPGA configuration.

A driver must be installed prior to using USB to communicate with ComBlocks for the first time. In summary, connect the ComBlock to power and a Windows OS PC via USB, then go to the Control Panel | Device Manager and add the driver by pointing to the driver located in the CD-ROM /Windows Drivers/USB 2.0/Windows Driver folder. Detailed instructions are available in the USB user manual
www.comblock.com/download/USB20_UserManual.pdf

Accidental FPGA file corruption

The COM-1700 is protected against corruption by an invalid FPGA configuration file. To recover from such occurrence, connect a jumper in JP1 position 2-3 prior to and during power-up. This prevents the FPGA configuration. Once this is done, the user can safely re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center GUI.

Analog I/Os

The COM-1700 includes multiple ADCs and DACs as listed below:

Function	Precision	Speed (MS/s)	Under control by	Connect
DAC1	12-bit	125	FPGA	J4/A11,B11
DAC2	12-bit	125	FPGA	J4/A13,B13
ADC1	10-bit	80	FPGA	J4/A2,B2
ADC2	10-bit	80	FPGA	J4/A4,B4
AUX_DAC1 (PWM)	10-bit	0.2	ARM	J4/A6
AUX_DAC2 (PWM)	10-bit	0.2	ARM	J4/A15
IF_GAIN_ CTRL (PWM)	10-bit	0.2	ARM	IF receiver gain control
AUX_ADC1	12-bit	0.2	ARM	J4/A16

Two 10-bit auxiliary DACs (actually pulse-width modulators) can be used for transmit and receive gain control of an external transceiver under ARM processor control. Output voltage ranges from 0 to 3.3 V.

A 12-bit auxiliary ADC can be used to detect received power of an external transceiver, under ARM processor control.

Auxiliary DACs

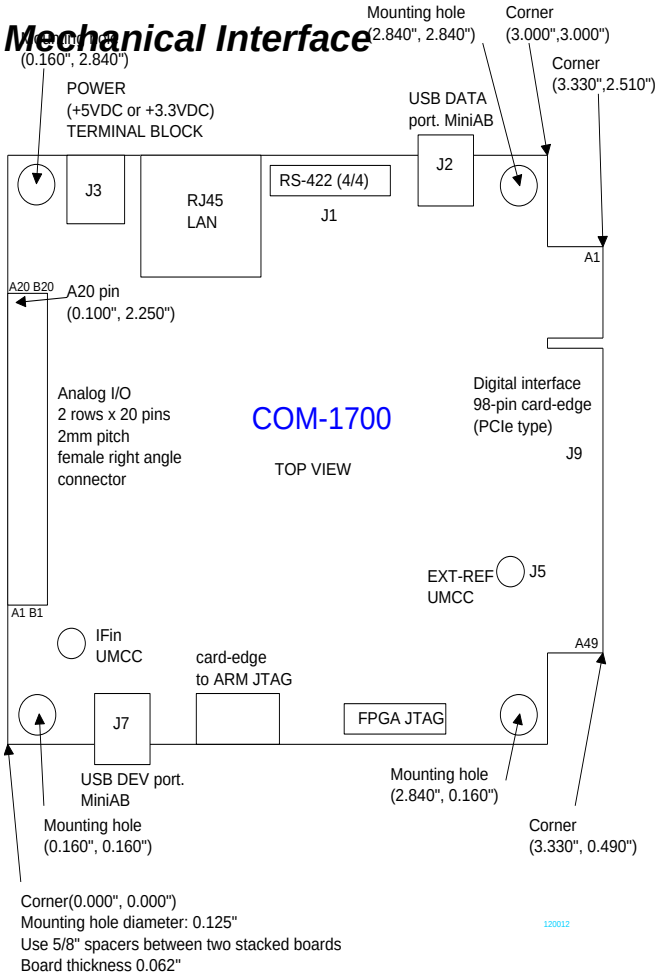
Several lower-speed auxiliary DACs can be used for external analog controls (transmit level for example) and internal IF receiver gain control. The ARM processor baseline code is structured to allow user-defined values in control registers or adaptive values under algorithms implemented in the FPGA.

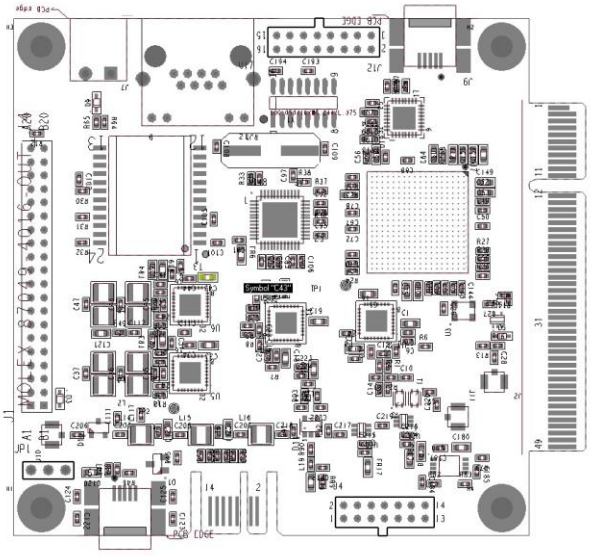
Parameters	Configuration
AUX_DAC1 control mode	0 = set in control register REG1/2 1 = set by FPGA algorithm and reported through status registers SREG9/10 REG0(0)
IF_GAIN_CTRL control mode	0 = set in control register REG5/6 1 = set by FPGA algorithm and reported through status registers SREG9/10 REG0(2)
AUX_DAC1	10-bit value REG1 = LSB[3] REG2(1:0) = MSbs
AUX_DAC2	10-bit value REG3 = LSB REG4(1:0) = MSbs
IF_GAIN_CTRL	10-bit value. 0x3FF for maximum gain. REG5 = LSB REG6(1:0) = MSbs

Schematics

The board schematics are available on-line at http://comblock.com/download/com_1700schematics.pdf

Mechanical Interface





For precise 2D mechanical dimensions, a Gerber file is available upon request.

[3] LSB = Least Significant Byte
MSbs = Most Significant bits.

VHDL code template

A VHDL template project is available on the ComBlock CD or on-line at www.comblock.com/download/com1700_000.zip
The template project includes:

- The VHDL source code (.vhd)
- The constraint file (.ucf) listing all pin assignments
- The Xilinx ISE project with the synthesis and implementation settings
- The resulting bit file (.mcs) is ready to be loaded into flash memory.

The sample code describes how the application interfaces with the ComBlock Control Center graphical user interface through control and monitoring registers. Monitoring and control messages and syntax are described in www.comblock.com/download/m&c_reference.pdf.

It also describes how to capture key internal signals in real-time and display on a host computer using the ComScope feature of the ComBlock Control Center. The ComScope user manual is available at www.comblock.com/download/comscope.pdf

Finally, the sample code includes the following drivers:

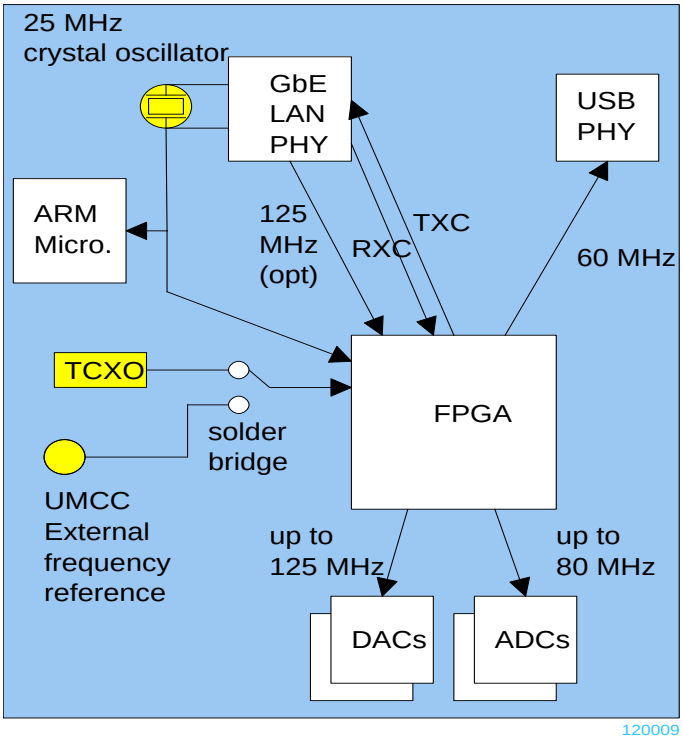
- 12-bit DAC driver
- 10-bit ADC driver
- USB 2.0 driver.
- GbE MAC layer

USB 2.0 Driver

Using any USB port requires the prior installation of the supplied ComBlock driver for Windows operating systems (XP, Win 7, Win 8). See the user manual at www.comblock.com/download/USB20_UserManual.pdf

Clock Architecture

The clock distribution scheme embodied in the COM-1700 is illustrated below.



The FPGA has access to three different frequency sources:

- 25 MHz oscillator (part of the LAN PHY), also used as frequency reference for the ARM micro.
- 26 MHz temperature-compensated crystal oscillator (TCXO) with the following frequency stability:
    - Frequency tolerance at manufacturing: ±2ppm
    - Frequency stability over temperature: ±0.5ppm from –30°C to +85°C
    - Aging: ±1ppm/year.
- External frequency reference via UMCC connector.

Selection of the TCXO versus external frequency reference is done through a solder bridge.

I/O Standards

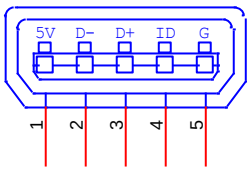
The digital signals on connector J5 are LVTTL (0 – 3.3V) single-ended signals by default. However, the I/O types can be easily changed by software to other types such as differential LVDS_33.

See Xilinx user guide ug381 for details.

Pinout

USB

Two USB ports labeled USB DATA and J7 are equipped with a mini type AB connector2. (G = GND). The COM-1700 acts as a USB device.



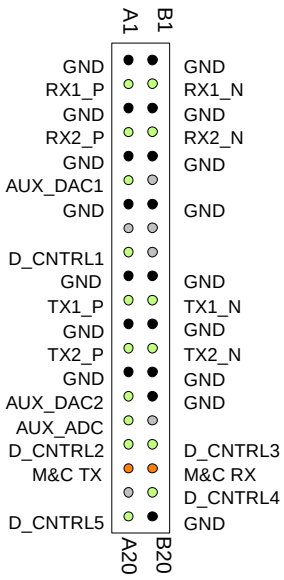
Right Connector J5

Top	A1	B1	Bottom
CLK_IN			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED	5		GND
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED	10		USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED	15		USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED	20		GND
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED	25		USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED	30		USER DEFINED
USER DEFINED			GND
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED			USER DEFINED
USER DEFINED	35		FPGA programming RDWR_B
USER DEFINED			FPGA programming CCLK
USER DEFINED			FPGA programming D7
USER DEFINED			FPGA programming D6
USER DEFINED			FPGA programming D5
USER DEFINED	40		FPGA programming D4
USER DEFINED			FPGA programming D3
USER DEFINED			GND
USER DEFINED			FPGA programming D2
USER DEFINED			FPGA programming D1
USER DEFINED	45		FPGA programming D0
USER DEFINED			FPGA programming DONE
			FPGA programming CSI_B
			FPGA programming PROG_B
M&C_TX			M&C_RX
	A49	B49	

Analog Differential I/O Connector J4

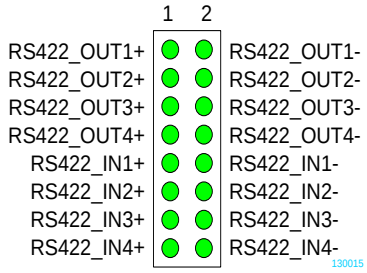
40-pin (2 rows x 20) 2mm male connector.

This connector is designed for a direct connection to the COM-350x transceivers.



RS422 Interface J1

16-pin (2 rows x 8) 0.1" through-hole (uninstalled)



I/O Compatibility List

(Not an exhaustive list)

Baseband Interface
COM-1500 Development platforms
Analog Interface
COM-3501 UHF transceiver
COM-3505 2.4/5 GHz transceiver
COM-4001/2/3/5/6/8 RF Quadrature Modulators (requires a simple harness: electrically compatible interface but not mechanically plug-in compatible)

ComBlock Ordering Information

COM-1700 LOW-POWER SDR DEVELOPMENT PLATFORM,
40-700 MHz IF receive / baseband transmit

Ordering options:

- option **–A**: dual I/Q baseband
- option **–B**: 70 MHz IF input
- option **–C**: 140 MHz IF input
- internal TCXO vs external frequency reference
- +5V unregulated supply vs +3.3V regulated

Optional accessory: **Y03007R4** JTAG/Serial adapter for optional ARM micro programming

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