

COM-1705 LOW-POWER PSK MODEM + VITERBI FEC + IP ROUTER

Key Features

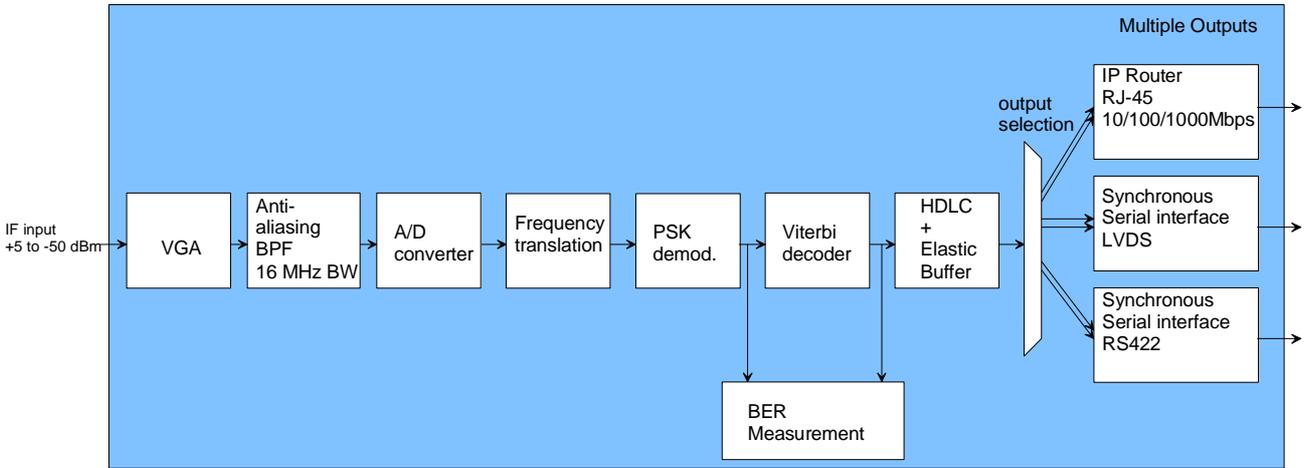
- Full duplex integrated PSK modem, including modulation, demodulation, convolutional error correction, scrambling, HDLC framing and GbE IP routing.
- Programmable symbol rates 2.4Ksymbols/s up to 14 Msymbols/s.
- Analog/IF interface:
 - dual I/Q baseband inputs, 1Vpp differential.
 - 70 MHz IF input: -50 to +5 dBm, 50 Ohm
 - 140 MHz IF input: -50 to +5 dBm, 50 Ohm
 - Outputs: dual I/Q baseband outputs, 2Vpp differential, 0.5V common mode.
- Convolution error correction, rates 1/2, 2/3, 3/4, 5/6 and 7/8.
- Serial HDLC to transmit empty frames over the synchronous link when no payload data is available.
- V.35 scrambling to randomize the modulated data stream.
- Data interface:
 - 10/100/1000 Ethernet LAN with built-in IP router
 - Synchronous serial interfaces: RS-422, LVDS
- Small size (3"x3"x0.3") and small power (2W)
- Modulation: BPSK/QPSK/OQPSK with output spectral shaping filter: raised cosine square root filter with 20% rolloff.
- Built-in test features:
 - Pseudo-random bit stream generation (PRBS-11) and BER measurement
 - Unmodulated carrier
 - Frequency offset (Doppler)
-  **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Input for an external, higher-stability 10 MHz frequency reference.
- Supply voltage (to be specified at the time of order)
 - Direct 3.3V or
 - 5V supply with reverse voltage and overvoltage protection.



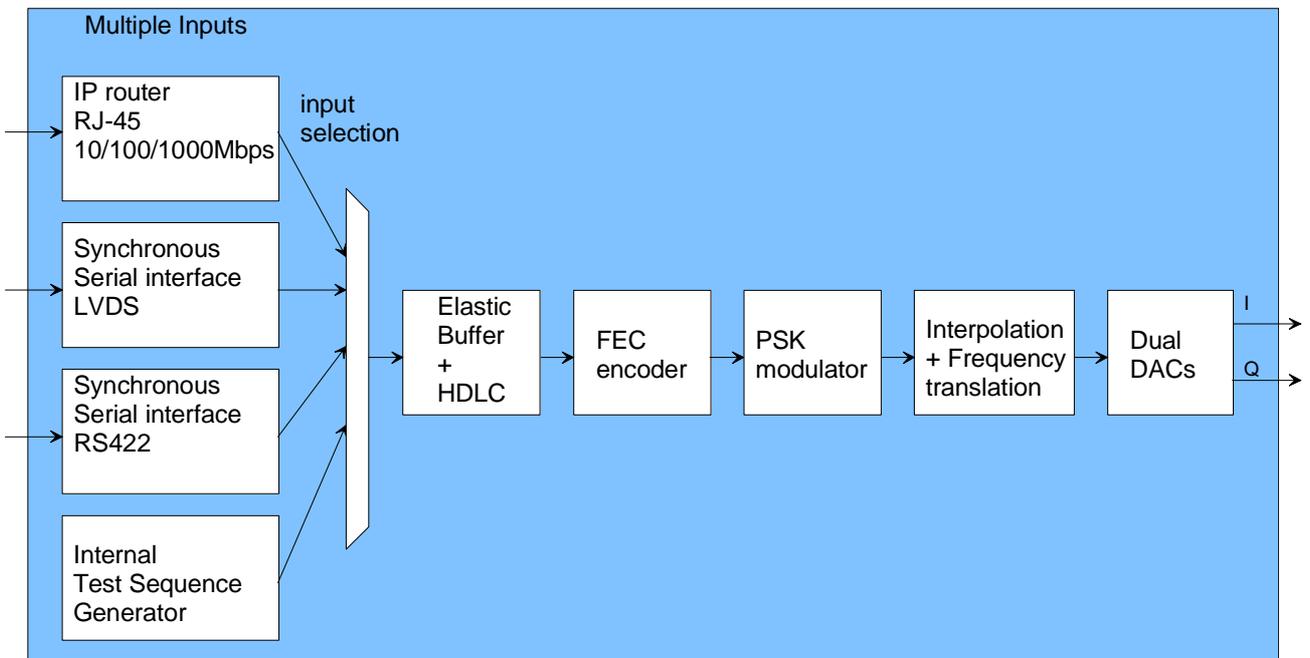
For the latest data sheet, please refer to the **ComBlock** web site: comblock.com/download/com1705.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html.

Block Diagram



Demodulator



Modulator

Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- USB
- TCP-IP/LAN,

Other connection types are also available through adjacent ComBlocks.

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1705 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the  *Detect* button, next click to highlight the COM-1705 module to be configured, next click the  *Settings* button to display the *Settings* window shown below.

COM1705 LOW-POWER PSK MODEM + VITERBI FEC + IP ROUTER Basic Settings

Control

Modulation & FEC encoding

Symbol rate (S/s): 1999997.3 [<20MS/s] Transmit serial bit rate (bits/s): 2000000

DAC Sampling Rate (Hz): 63999913.4 Modulation: QPSK

Signal gain: 30000 [<65536] External transmitter gain: 700 [<1024]

Output center frequency: 0 Hz Spectrum inversion Channel filter

FEC encoding Differential encoding Convolutional FEC encoding: K=7, R=1/2, Intelsat

V.35 scrambling HDLC encoding Input: PRBS-11 test sequence

TX_ENB RX_TXN

Demodulation & FEC decoding

Nominal symbol rate (S/s): 2000000 [<14MS/s] Modulation: QPSK

Input center frequency: 14000000 Hz Frequency acquisition range: 0 Hz

AGC response time: 10 [0-14] Spectrum inversion

FEC decoding Differential decoding Viterbi FEC decoding: K=7, R=1/2, Intelsat

V.35 descrambling HDLC decoding Input: Analog baseband/IF

Output: Synchronous serial RS-422 (J1)

General

IP-address: 172.16.1.128

Apply Ok Advan... Cancel

Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center “Advanced” configuration or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Definitions for the [Control registers](#) are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). It is automatically loaded up at power up. All control registers are read/write.

Transmitter	
Parameters	Configuration
Input selection / format, test modes	Select the origin of the transmitter input data stream. 0 = USB 2.0 (8-bit) 1 = RJ-45 GbE IP router (8-bit) 2 = 1-bit synchronous serial LVDS 3 = 1-bit synchronous serial RS-422 4 = internal PRBS-11 test sequence 5 = internal unmodulated carrier 8-bit parallel input bytes are transmitted MSb first. REG19(3:0)
TX_ENB	Transmit enable digital control on J4/A17 Typically used to turn on/off an external power amplifier. REG19(4)
RX_TXN	Digital control on J4/B17. Typically used to fast switch a half-duplex external transceiver between receive and transmit modes. REG19(5)
FEC convolutional encoder	
Parameters	Configuration
Constraint length K and rate R	0001 = (K = 7, R=1/2, Intelsat) 0010 = (K = 7, R=2/3, Intelsat) 0011 = (K = 7, R=3/4, Intelsat) 0100 = (K = 7, R=5/6, Intelsat) 0101 = (K = 7, R=7/8, Intelsat) REG12(4:1)

Differential Encoding	Differential encoding is useful in removing phase ambiguities at the PSK demodulator, at the expense of doubling the bit error rate. When enabled, the differential decoding must be enabled at the receiving end. There is no need to use the differential encoding to remove phase ambiguities at the PSK demodulator when the Viterbi decoder and HDLC decoder are enabled. 0 = disabled 1 = enabled REG12(5)
Bypass FEC encoding	0 = encoding enabled 1 = bypass REG12(6)
V.35/Intelsat IESS 308 scrambling before FEC encoding	0 = enabled 1 = bypass REG12(7)
HDLC encoding	0 = enabled 1 = bypass REG12(0)
PSK Modulator	
Parameters	Configuration
Processing clock f_{clk_tx}	Modulator processing clock. Also serves as DAC sampling clock. 20-bit unsigned integer expressed as $f_{clk_tx} * 2^{20} / 225.3333\text{MHz}$ when 26MHz frequency reference, or $f_{clk_tx} * 2^{20} / 220\text{MHz}$ when 10MHz frequency reference. Recommended range: 45-90 MHz REG20 = bits 7-0 (LSB) REG21 = bits 15 – 8 (MSB) REG22(3:0) = bits 19 – 16 (MSB)
Symbol rate $f_{symbol\ rate\ tx}$	The modulator symbol rate is in the form $f_{symbol\ rate\ tx} = f_{clk_tx} / 2^n$ where n ranges from 1 (f_{clk_tx} is twice the symbol rate) to 15 (symbol rate = $f_{clk_tx} / 65536$). n is defined in REG23(3:0)
Modulation type	0 = BPSK 1 = QPSK 2 = OQPSK REG7(5:0)
Spectrum inversion	Invert Q bit. This is helpful in compensating any frequency spectrum inversion occurring in a subsequent RF frequency translation. 0 = off 1 = on

	REG7(6)
Channel filter enabled	0 = enable the spectrum shaping filters (root raised cosine, interpolation) 1 = bypass the spectrum shaping filters. (special use in applications when a root raised cosine filter is not used in the demodulator.) REG7(7)
Signal gain	Signal level. 16-bit unsigned integer. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Therefore, we recommend <u>checking for saturation at the D/A converter</u> when changing either the symbol rate or the signal gain. REG17 = bits 7-0 (LSB) REG18 = bits 15-8 (MSB)
External transceiver tx gain control	10-bit value for analog gain control TX_GAIN_CNTRL1 (J4 pin A15) REG3 = LSB REG4(1:0) = MSBs
Output Center frequency (f _{cout})	Frequency translation. 32-bit signed integer (2's complement representation) expressed as $f_{cout} * 2^{32} / f_{clk_tx}$ REG8 = bits 7-0 (LSB) REG9 = bits 15 – 8 REG10 = bits 23 – 16 REG11 = bits 31 – 23 (MSB)
Serial tx bit rate	Set the nominal input bit rate in order to supply a regular bit clock to the user data source. Must be consistent with the modulator symbol rate, modulation type, FEC rate, HDLC overhead (when enabled). When HDLC is disabled, this field MUST be set to be at least slightly greater than the transmitter throughput (or else an underflow condition will occur). $f_{input\ bit\ rate\ tx} * 2^{32} / f_{clk_rx}$ REG13 = bits 7-0 (LSB) REG14 = bits 15 – 8 REG15 = bit 23 – 16 REG16 = bit 31 – 23 (MSB)
Receiver	
PSK Demodulator	
Parameters	Configuration
Processing clock	The demodulator processing clock also serves as A/D converter sampling clock. It can be generated within the FPGA or externally. Baseline $f_{clk_rx} = 80$ MSamples/s (for complex input, 140 MHz IF undersampling), or 56 MSamples/s (for 70 MHz IF undersampling)
Nominal	The demodulator nominal symbol rate is in

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LSB = Least Significant Byte
MSB = Most Significant Byte

Nominal Center frequency (f_{c_rx})	<p>Expected center frequency of the received signal. 32-bit signed integer (2's complement representation) expressed as $f_{c_rx} * 2^{32} / f_{clk_rx}$.</p> <p>In the case of IF undersampling, the residual intermediate frequency is removed here. For example, in the case of a 70 MHz IF signal sampled at 56Msamples/s, the 14 MHz residual frequency is removed here by entering 0xC0000000.</p> <p>REG29 = bit 7-0 (LSB) REG30 = bit 15 – 8 REG31 = bit 23 – 16 REG32 = bit 31 – 23 (MSB)</p>
Modulation type	<p>0 = BPSK 1 = QPSK 2 = OQPSK REG33(5:0)</p>
Spectrum inversion	<p>Invert Q bit. This is helpful in compensating any frequency spectrum inversion occurring during RF frequency translations.</p> <p>0 = off 1 = on REG33(6)</p>
Frequency acquisition range (scan)	<p>The demodulator natural frequency acquisition range is around 1% of the symbol range (depending on modulation, SNR). The frequency acquisition range can be extended by frequency scanning. Scanning steps are spaced ($f_{symbol\ rate\ rx} / 128$) apart. The user can thus trade-off acquisition time versus frequency acquisition range by specifying the number of scanning steps here.</p> <p>For example, 16 steps yield a frequency acquisition range of $\pm(f_{symbol\ rate\ rx} * 12.5\%)$</p> <p>REG24</p>
AGC response time	<p>Users can to optimize the AGC response time while avoiding instabilities (depends on external factors such as gain signal filtering at the RF front-end and symbol rate). The response time is approximately:</p> <p>0 = 8 symbols, 1 = 16 symbols, 2 = 32 symbols, 3 = 64 symbols, etc.... 10 = every thousand symbols.</p> <p>Valid range 0 to 14. REG34(4:0)</p>
Rx AGC enable	REG0 = always 0x05

Input selection	<p>0 = analog input 7 = internal loopback mode, from modulator. REG35(2:0)</p>
Viterbi FEC decoder	
Parameters	Configuration
Constraint length K and rate R	<p>0001 = (K = 7, R=1/2, Intelsat) 0010 = (K = 7, R=2/3, Intelsat) 0011 = (K = 7, R=3/4, Intelsat) 0100 = (K = 7, R=5/6, Intelsat) 0101 = (K = 7, R=7/8, Intelsat) REG37(4:1)</p>
Differential Decoding	<p>0 = disabled 1 = enabled REG37(5)</p>
V.35/Intelsat IESS 308 descrambling after FEC decoding	<p>0 = enabled 1 = bypass REG37(7)</p>
Bypass FEC decoding	<p>0 = decoding enabled 1 = bypass REG38(7)</p>
HDLC decoding	<p>0 = enabled 1 = bypass REG37(0)</p>
Output selection	<p>0 = USB 2.0 (8-bit) 1 = RJ-45 GbE IP router (8-bit) 2 = synchronous serial LVDS 3 = synchronous serial RS-422 REG36(2:0)</p>
Network Interface	
Parameters	Configuration
IP address	<p>4-byte IPv4 address. Example : 0x AC 10 01 80 designates address 172.16.1.128 The new address becomes effective immediately (no need to reset the ComBlock). REG41: MSB REG42 REG43 REG44: LSB</p>
Reserved	<p>REG45 through 50 are reserved for the LAN MAC address. These registers are set at the time of manufacturing. Since the MAC address is unique, it can also be used as a unique identifier in a radio network with many nodes.</p>

(Re-)Writing to the last control register REG44 is recommended after a configuration change to enact the change.

Monitoring

Status Registers

Digital status registers are read-only.

PSK/QAM/APSK Demodulator Monitoring	
Parameters	Monitoring
Front-end AGC	12-bit unsigned value controlling the internal IF gain and external receiver gain control RX_AGC1. Inverted scale: 0 is for the maximum gain. SREG9 = LSB SREG10(3:0) = MSBs
Carrier frequency offset (fcdelta)	Residual frequency offset with respect to the nominal carrier frequency. 20-bit signed integer (2's complement) expressed as $fcdelta * 2^{20} / fsymbol\ rate$. SREG11 = LSB SREG12 SREG13(3:0) = MSBs
Carrier tracking loop lock status	Lock is declared if the standard deviation of the phase error is less than 25deg rms. 0 = unlocked 1 = locked SREG14 bit 0
Inverse SNR	A measure of noise over signal power. 0 represents a noiseless signal. Valid only when demodulator is locked. SREG15
Viterbi FEC decoder monitoring	
Parameters	Monitoring
Synchronized	(FEC_DEC_LOCK_STATUS variable) Solid '1' when the Viterbi decoder is locked. '0' or toggling when unlocked. SREG14(1)
Decoder built-in BER	The Viterbi decoder computes the BER on the received (encoded) data stream irrespective of the transmitted bit stream. Encoded stream bit errors detected over a 1000-bit measurement window. SREG16 = bits 7 – 0 (LSB) SREG17 = bits 15 – 8 SREG18 = bits 23 – 16 (MSB)
HDLC decoder monitoring	
Parameters	Monitoring
Cumulative number of valid bits at HDLC output	SREG19: LSB SREG20: SREG21: SREG22: MSB

BER Measurement	
Parameters	Monitoring
Bit Errors	Bit errors can be counted when a PRBS-11 test sequence is transmitted. Number of bit errors in a 1,000,000 bit window. 32 bit unsigned. SREG23: error_count[7:0] (LSB) SREG24: error_count[15:8] SREG25: error_count[23:16] SREG26: error_count[31:24] (MSB) The bit errors counter is updated once every periodic measurement window. Reading the value will not reset the counter.
BER Synchronization status	0 = not synchronized. 2047-bit pattern is not detected. 1 = synchronized SREG27(0)
TCP-IP Connection Monitoring	
Parameters	Monitoring
TCP-IP connection on port 1024 (data stream)	Bit 0 = port 1028 (M&C) connected Bit 1 = port 1024 (data) connected 1 for connected, 0 otherwise SREG28(1:0)
MAC address	Unique 48-bit hardware address (802.3). In the form SREG30:SREG31:SREG32:....SREG35 Since the MAC address is unique, it can also be used as a unique identifier in a radio network with many nodes.
Parameters	Monitoring
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-7. Properly operating hardware will result in the following sequence being displayed: SREG0/1/2/3/4/5/6/7 = 2C F1 95 xx 0F 01 24 22
Saturation	Denotes saturation in the transmit path. SREG8(0)

A dummy read to status register SREG8 is required to latch multi-byte status fields (to preserve their integrity).

Test Points

Test Point	Definition
J9 connector pin A3	'1' when the BER tester is synchronized with the received PRBS-11 test sequence
J9 connector pin A4	'1' when BER tester detects a byte error. Assumes that a PRBS-11 test sequence is being transmitted. Valid only when the BER tester is synchronized.
J9 connector pin A7	BER measurement: Start of PRBS-11 periodic test sequence detected with less than 10% bit errors. Periodic pulses every 2047 bits.
J9 connector pin A8	Scan frequency (coarse measurement of the received frequency)
J9 connector pin A15	Carrier tracking loop frequency (fine measurement of the received frequency)
DONE	FPGA DONE pin. High indicates proper FPGA configuration

ComScope Monitoring

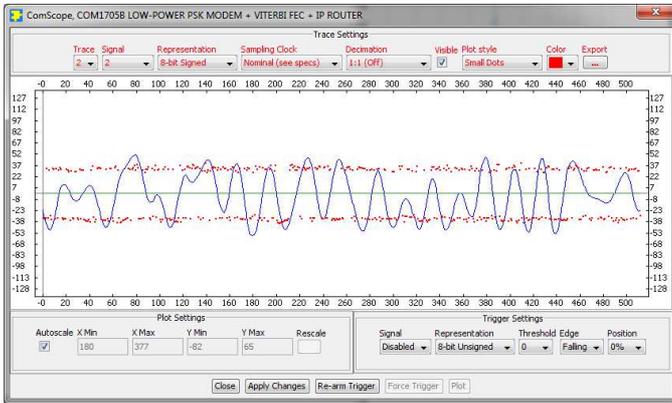
Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-1705 signal traces are defined as follows:

Trace 1 signals	Format	Nominal sampling rate	Buffer length (samples)
1: Input signal (I-channel) after AGC, frequency translation, CIC decimation	8-bit signed	Input sampling rate f_{clk_rx} / R	512
2: phase after scanning and before final carrier tracking loop	8-bit signed	1 sample / symbol	512
3: Magnitude after final AGC	8-bit signed	1 sample / symbol	512
4: symbol timing tracking correction (accumulated)	8-bit unsigned	1 sample / symbol	512
Trace 2 signals	Format	Nominal sampling rate	Buffer length (samples)
1: Input signal (Q-channel) after AGC, frequency translation, CIC decimation	8-bit signed	Input sampling rate f_{clk_rx} / R	512
2: Demodulated I channel	8-bit signed	1 sample / symbol	512
3: Input signal I-channel	8-bit signed	Input sampling rate f_{clk_rx}	512
4: PLL Carrier tracking phase correction (accumulated)	8-bit signed	Input sampling rate f_{clk_rx}	512
Trace 3 signals	Format	Nominal sampling rate	Buffer length (samples)
1: Input signal Q-channel	8-bit signed	Input sampling rate f_{clk_rx}	512
2: final AGC gain	8-bit signed	Variable	512
Trigger Signal	Format		
N/A			

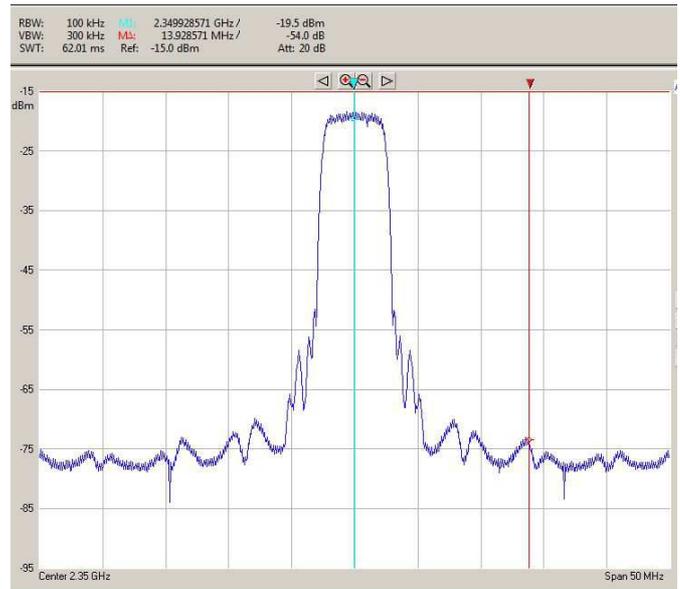
ComScope signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk_rx} processing clock as real-time sampling clock.

In particular, selecting the f_{clk_rx} processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

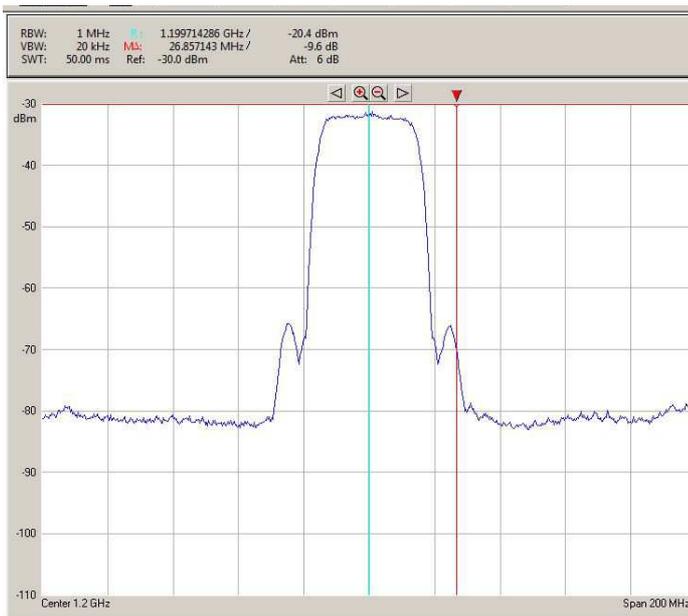
The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope Window Sample: showing the received baseband (I-channel, blue trace) and demodulated bits (I-channel, center of symbol, red dots)



Output spectrum (after D/A conversion and RF modulation): 5 Msymbols/s



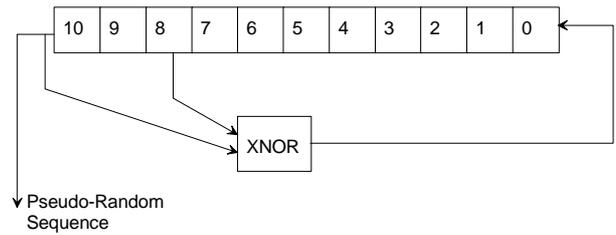
Output spectrum (after D/A conversion and RF modulation): 10 Msymbols/s

Operation

A/D sampling rate

The Analog to Digital converter sampling rate f_{clk_rx} is fixed for a given hardware option.

- Options **-A,-D**: complex baseband input. 80 MSamples/s
- Option **-B,-E**: 70 MHz IF input : 56 MSamples/s
- Option **-C,-F**: 140 MHz IF input: 80 MSamples/s



The first 100 bits of the PN sequence are as follows:

```
000000000 011111111 001111110 000111110
110011100 000001001 111101000 111011010
110100110 001100001
```

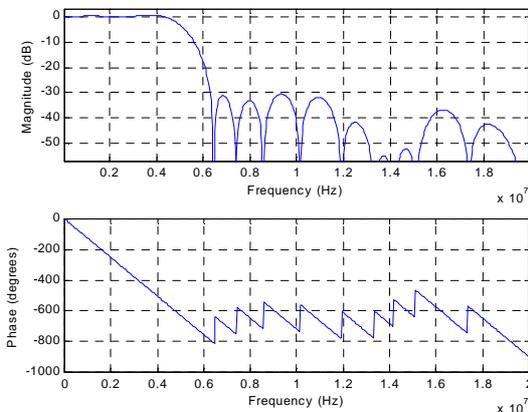
Demodulator frequency acquisition

The center frequency acquisition window is programmable. The natural acquisition window is 1% of the symbol rate. This window can be extended through frequency scanning, at the expense of a longer acquisition time.

Filter Response

This module is configured with a 20% rolloff filter.

Filter Response (20% rolloff)



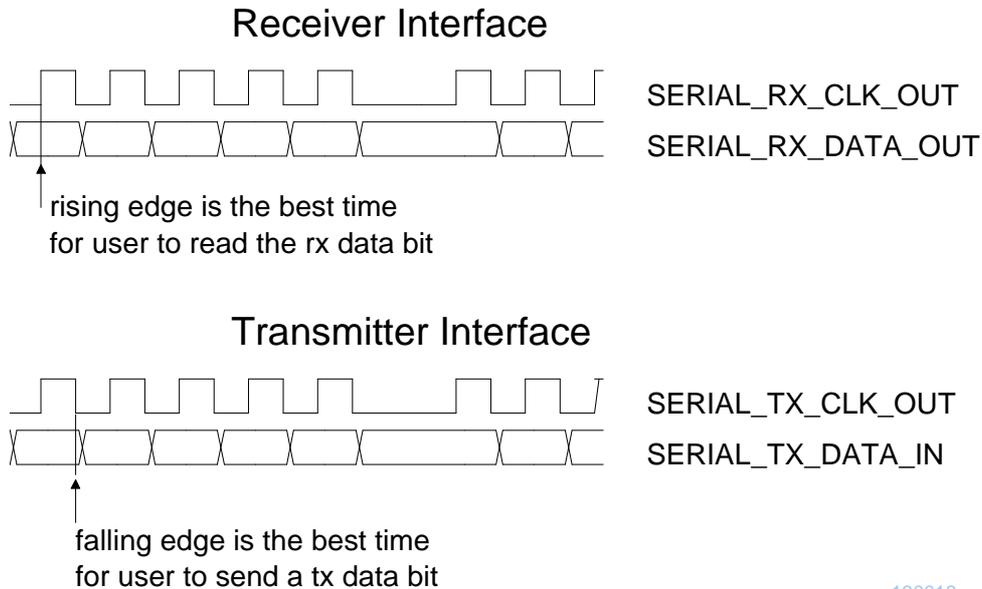
Pseudo-Random Bit Stream (Test Pattern)

A periodic pseudo-random sequence can be used as modulator source instead of the input data stream. A typical use would be for end-to-end bit-error-rate measurement of a communication link. The sequence is 2047-bit long maximum length sequence generated by a 11-tap linear feedback shift register:

Interfaces

1-bit synchronous serial

Clock synchronous 1-bit serial interfaces are available at the modulator data input and demodulator data output as LVDS or RS-422 electrical signals. The timing diagram is show below:



The modem provides the transmit and receive clocks to the user. When HDLC encoding is enabled, the user can decide not to transmit any data by setting the `SERIAL_TX_DATA_VALID_IN` signal to '0'. When the user supplies no data, the modem will send empty HDLC frames over the synchronous modulated link. When HDLC encoding is disabled, the user must supply a new data bit before every `SERIAL_TX_CLK_OUT` rising edge.

IP Routing

Concept: On the transmit side, IP packets from the RJ-45 10/100/1000Mbps LAN interface are forwarded to the modulated link if the IP destination address is deemed remote.

The IP packets received over the LAN are stripped of their link layer information: Ethernet source address, destination address and type are removed, keeping only the IP fields.

TCP, UDP, ICMP and IGMP packets are processed since they are transmitted as IP datagrams.

Non IP packets are rejected.

IP packets whose Time-To-Live field has reached zero are discarded. For the other packets, the TTL is decremented.

Limited broadcasts (those with destination IP address 255.255.255.255) are not forwarded.

Packets received while the IP router is busy are also discarded without notification.

The IP packet maximum size (maximum transmission unit (MTU)) is 1500 bytes. No datagram fragmentation is necessary nor used.

The IP packets are then encapsulated within a byte-wise HDLC frame, one packet per frame. A 16-bit CRC is inserted at the end of each frame to detect errors upon reception.

The reverse process is performed at the receiving end. Erroneous packets which do not pass the CRC test are rejected.

The forwarding rules are specified in the RFC1812 document “Requirements for IP Version 4 Routers”.

When an IP packet is received over the modulated link interface, the IP router will check whether the packet destination is for this local subnet or not. If not, the packet will be forwarded to the default gateway IP. To determine whether a packet is destined to this subnet, the router compares the masked destination address (Destination IP address & subnet mask) with the masked router address (IP router own IP address & subnet mask).

Example:

- Router IP address: 172.16.1.1
- Router subnet mask: 255.255.255.0
- Packet destination IP address is 74.54.97.66

Masked packet destination: 74.54.97.0

Masked router address: 172.16.1.0

Since the masked packet destination does not match the masked router address, the packet is not for a local destination. Consequently the router will forward the packet to the default gateway.

Valid IP packets are re-encapsulated inside an Ethernet packet, one IP packet per Ethernet packet.

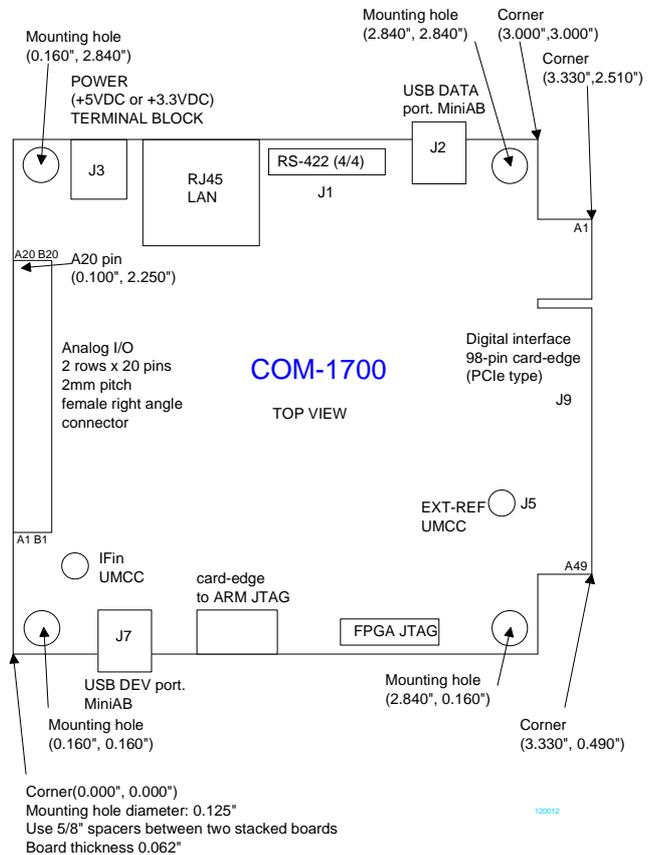
The IP to Ethernet MAC address association is determined by means of an Address Resolution Protocol (ARP) query-reply transaction. The COM-1705 will send an ARP request asking “whois the destination IP address?” and will wait for the ARP reply with the MAC information.

The IP address – MAC address relationships are stored within two ARP cache memories to expedite the Ethernet packet construction. The ARP cache memories are refreshed every 5 minutes on average. The total cache capacity is 170 entries. The user can clear the ARP cache without wait: see control register REG22 bit 5.

USB

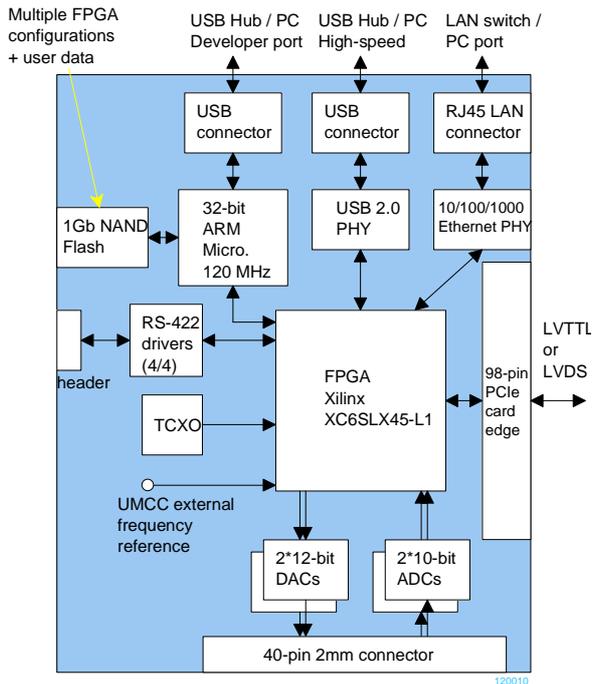
A USB port is available for monitoring and control purposes only. It cannot be used for transferring payload data.

Mechanical Interface

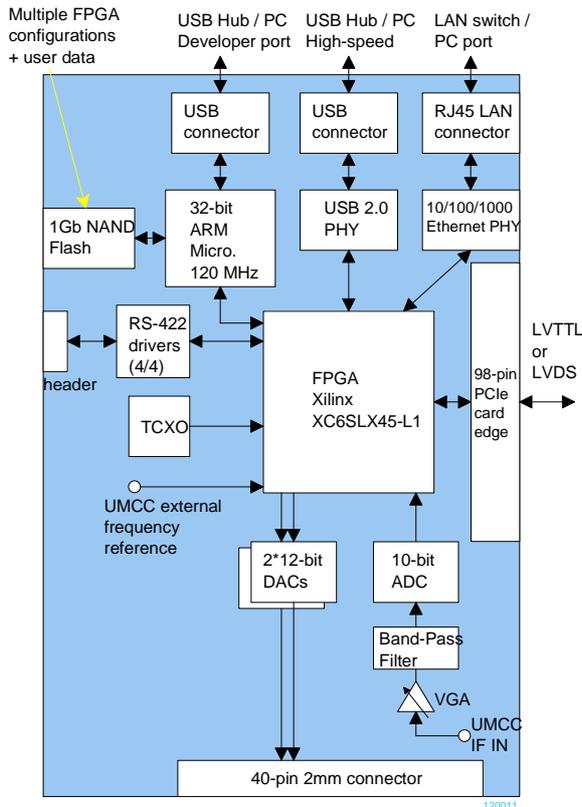


Schematics

The board schematics are available on-line at http://comblock.com/download/com_1700schematics.pdf



COM-1705 (Options –A/D Hardware Block Diagram



COM-1705 (Options –B/C/E/F Hardware Block Diagram

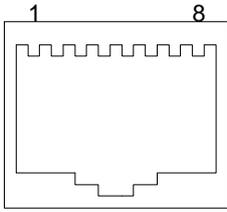
Electrical Interfaces

Signal	Connector
Power	Right-angle 3.81mm terminal block. 3.1 – 3.5V DC regulated or 4.75 – 5.25V DC unregulated (select at the time of order) 2W typ.
10/100/1000 Ethernet LAN for data, monitoring and control	RJ45 Supports auto MDIX to alleviate the need for crossover cable.
USB monitoring and control	Mini-USB connector Type AB Full speed / Low Speed
IF input	70 MHz center frequency -50 to +5 dBm AC coupled. 50 Ohm UMCC female connector J6
Modulated baseband outputs	2Vpp differential (1Vpp single ended), 0.5V common-mode voltage. Because of the high source impedance (1KOhm), these signals should 'see' a high input impedance. 40-pin 2mm connector J4
External 10 MHz frequency reference	Hardware options –D,E,F. External 10 MHz frequency reference for frequency synthesis. Sinewave, clipped sinewave or squarewave. UMCC female connector (J5). Input is AC coupled. Minimum level 0.6Vpp. Maximum level: 3.3Vpp.
Synchronous serial, LVDS	98-pin card edge, PCIe., J9
Synchronous serial, RS-422	16-pin header J1

Pinout

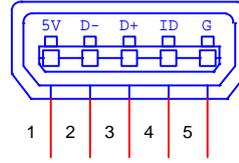
LAN Connector RJ1

The RJ45 Jack is wired as a standard PC network interface card. As the Ethernet PHY supports auto-MDIX, there is no need for special crossover cables when connecting directly to a PC.



1 Tx+
2 Tx-
3 Rx+
6 Rx-

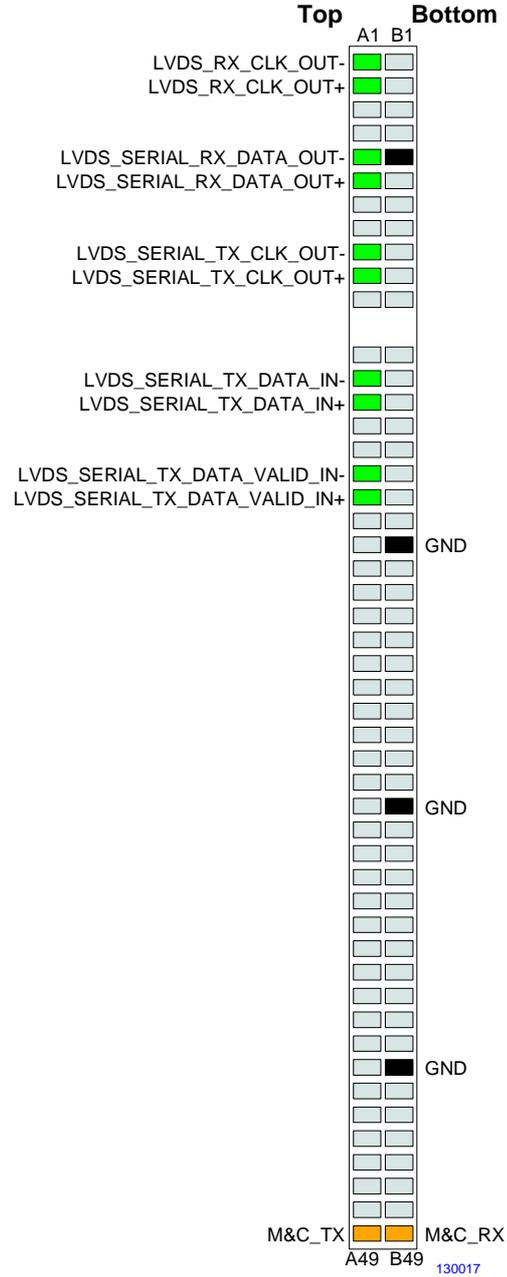
RJ-45 Jack



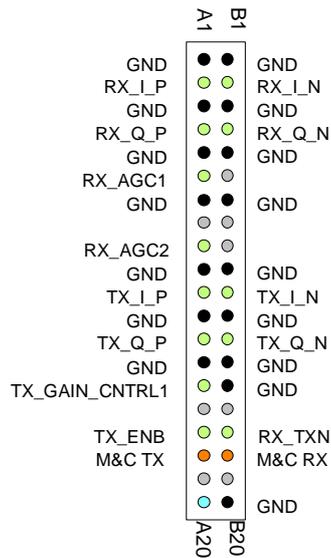
Right Connector J9

USB

Two USB ports labeled USB DATA and J7 are equipped with a mini type AB connectors. (G = GND). The COM-1705 acts as a USB device.



Analog I/O Connector J4

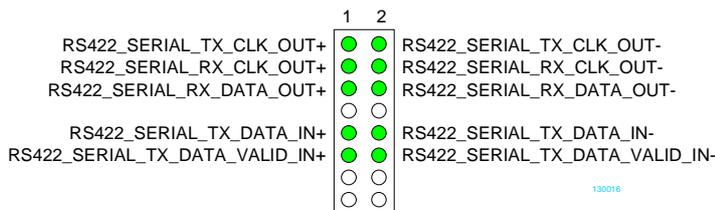


Configuration Management

This specification document is consistent with the following software versions:

- COM-1705 FPGA firmware: Version 0 and above.
- ComBlock Control Center graphical user interface: Revision 3.06i and above.

RS-422 Connector J1



I/O Compatibility List

(not an exhaustive list)

Digital Input
COM-30xx RF/IF/Baseband receivers.
Baseband Interface
COM-1500 Development platforms
Analog Interface
COM-3501 UHF transceiver
COM-3505 2.4/5 GHz transceiver
COM-4001/2/3/5/6 RF Quadrature Modulators (requires a simple harness: electrically compatible interface but not mechanically plug-in compatible)

ComBlock Ordering Information

COM-1705

**LOW-POWER PSK MODEM + VITERBI FEC +
IP ROUTER**

Options:

- A (baseband input, 26 MHz TCXO),
- B (70 MHz IF input, 26 MHz TCXO) or
- C (140 MHz IF input, 26 MHz TCXO)
- D (baseband input, 10 MHz external clock),
- E (70 MHz IF input, 10 MHz external clock),
- F (140 MHz IF input, 10 MHz external clock)

Please also specify +5V unregulated or +3.3V regulated supply voltage.

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