



**ARM - FPGA communication programming**

FPGA\_JTAG1 (TMS) → C21  
 FPGA\_JTAG2 (TCK) → C149  
 FPGA\_JTAG3 (TDI) → C152  
 FPGA\_JTAG4 (TDO) → C17  
 FPGA\_DONE (DONE) → C143  
 C15 → C163  
 C20 → D\_GND

ARM - FPGA communication

## ARM - FPGA communication

UC\_DATA[0-7] 

UC\_CTRL[1-4] 

UC\_CTRL1 {ALE}

UC\_CTRL2 {REB}

UC\_CTRL3 {WEB}

UC\_CTRL4 {FPGA CSB}

## Monitoring & Control

M&C\_[1-4]

M&C 1 (EDGE/LEFT\_RX)

M&C 2 (EDGE/LEFT\_TX)

M&C 3 (RIGHT\_RX)

M&C 4 (RIGHT\_TX)

### DDR3 SODIMM presence detect

DDR3\_I2C[0-1] SODIMM presence detect

DDR3\_I2C0 (SCL)  
DDR3\_I2C1 (SDA)

3 DDR3\_EVENT# require pull-up

## DISABLE FPGA CONFIGURATION

The diagram shows a 2-pin header labeled J3. Pin 1 is connected to a red wire that leads to a pin labeled D\_GND. Pin 2 is connected to a blue wire that leads to a pin labeled ARM. Below the header, the text 'HEADER-2PIN' is written. To the right of the diagram, there is a note: 'Place jumper on to prevent the ARM micro from configuring the FPGA at power up. Also place jumper when using a JTAG programming pod.'

Place jumper on to prevent the ARM micro from configuring the FPGA at power up. Also place jumper when using a JTAG programming pod.

The diagram shows a circuit with a red LED labeled D1. A resistor labeled R2 with a value of 100 Ohms and a tolerance of 1% is connected in series with the LED. The LED is connected to a point labeled D, and the resistor is connected to a point labeled D1. The ground connection is labeled D GND. The text "FAULT LED" is written in blue above the LED.

Temperature sensor

P4[29]/TX_MCLK/MAT2[1]/RXD3			
D5	P1[0]/ENET_TXD0		C2
B4	P1[1]/ENET_TXD1	TRST	C3
A4	P1[4]/ENET_TX_EN	TDI	B1
C5	P1[8]/ENET_CR5	TMS/SWDIO	C1
B5	P1[9]/ENET_RXD0	TC/SWDCLK	A1
A5	P1[10]/ENET_RXD1	TD0/SWO	F3
D6	P1[14]/ENET_RX_ER	RESET	B2
C6	P1[15]/ENET_REF_CLK	RTCK	
A6	P1[16]/ENET_MDC		
B6	P1[17]/ENET_MDIO		
H4	P1[18]/USB_UP_LED/PWM1[1]/CAP1[0]		H2
J4	P1[19]/MCO4/USB_PPWR/CAP1[1]	XTAL1	G3
K4	P1[20]/MCO1/PWM1[2]/SCK0	XTAL2	
F5	P1[21]/MCABORT/PWM1[3]/SSEL0		F2
J5	P1[22]/MCOB0/USB_PPWR/MAT1[0]	RTCX1	G1
K5	P1[23]/MCI1/PWM1[4]/MISO0	RTCX2	
H5	P1[24]/MC12/PWM1[5]/MOSI0		
G5	P1[25]/MCOA1/MAT1[1]		
K6	P1[26]/MCOB1/PWM1[6]/CAP0[0]	NC1	D4
K7	P1[27]/CLKOUT/USB_OVRCR/CAP0[1]	NC2	E4
J7	P1[28]/MCOA2/PCAP1[0]/MAT0[0]		
G6	P1[29]/MCOB2/PCAP1[1]/MAT0[1]		
F4	P1[31]/SCK1/AD0[5]		

[illegible]

Layout Note:  
Place 4.7uF cap close  
to USB connector

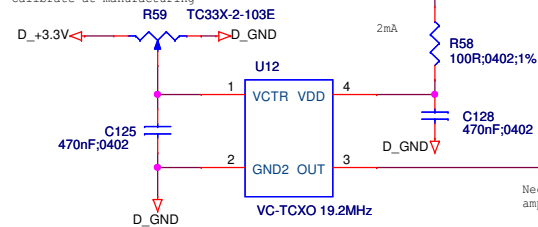
AZ  
Mobile Satellite Services  
18221A Flower Hill Way  
Gaithersburg, MD 20879  
USA

Title	COM-1800 / ARM MICRO
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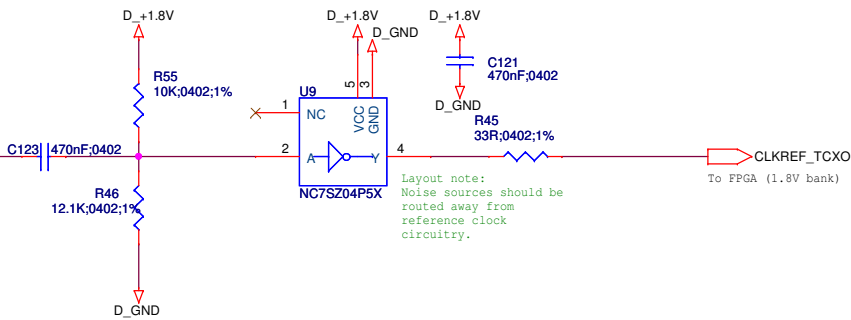
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### (19.2MHz) VC-TCXO

2.5ppm over -30/+75C, 1ppm/year aging  
3.2x2.5mm footprint  
Calibrate at manufacturing



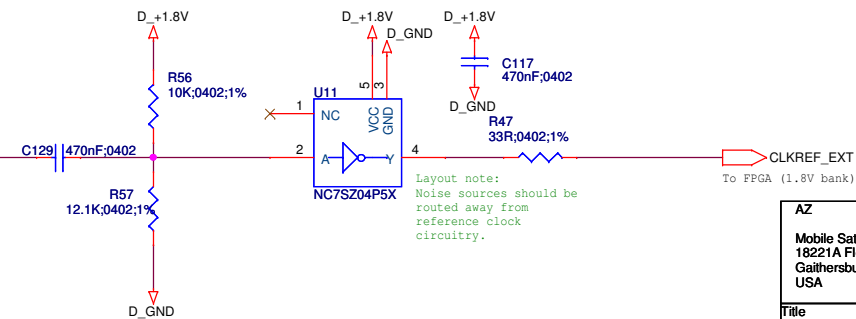
Design note1: use 1.8V drivers to minimize noise  
Design note2: place 33R at source to dampen waveform/reduce overshoot/clock harmonics  
Design note3: NC7SZ04 is 5.5V tolerant



### EXTERNAL FREQUENCY REFERENCE (INPUT) 10 MHz or 1PPS

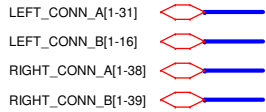


Ultra-miniature coaxial connector on PCB. Connected to IP67 SMA on front-panel through cabling.

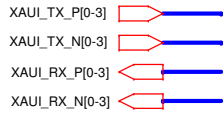


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Mobile Satellite Services 18221A Flower Hill Way Gaithersburg, MD 20879 USA		
Title		
COM-1800 CLOCKS		
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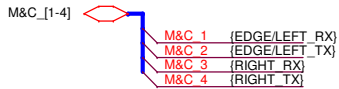
## I/Os (LVCMOS or LVDS)



## I/Os (XAUI)

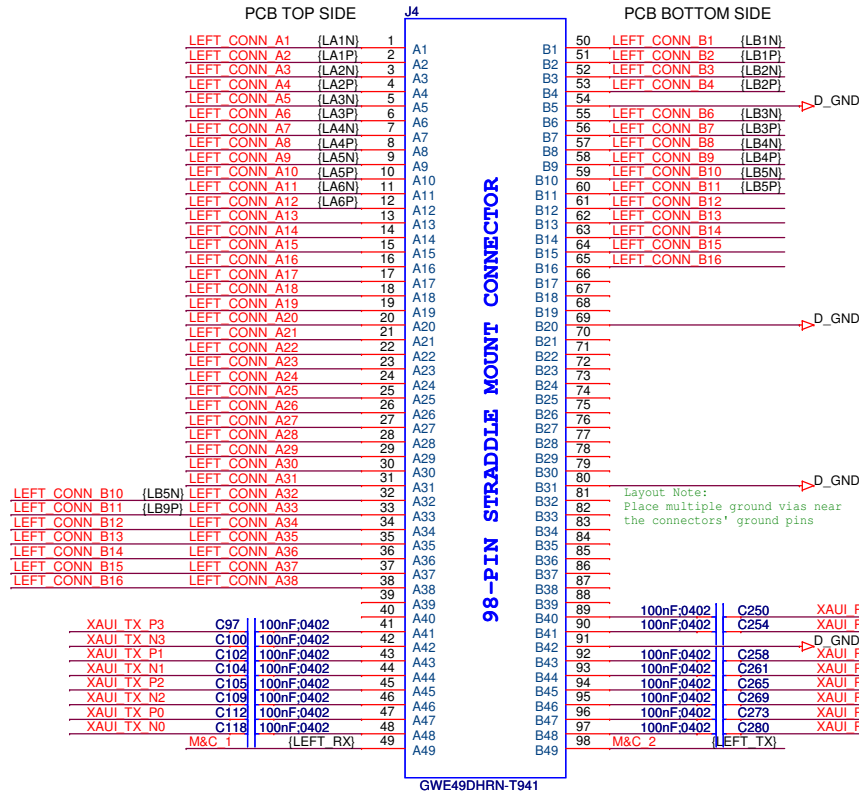


## Monitoring & Control

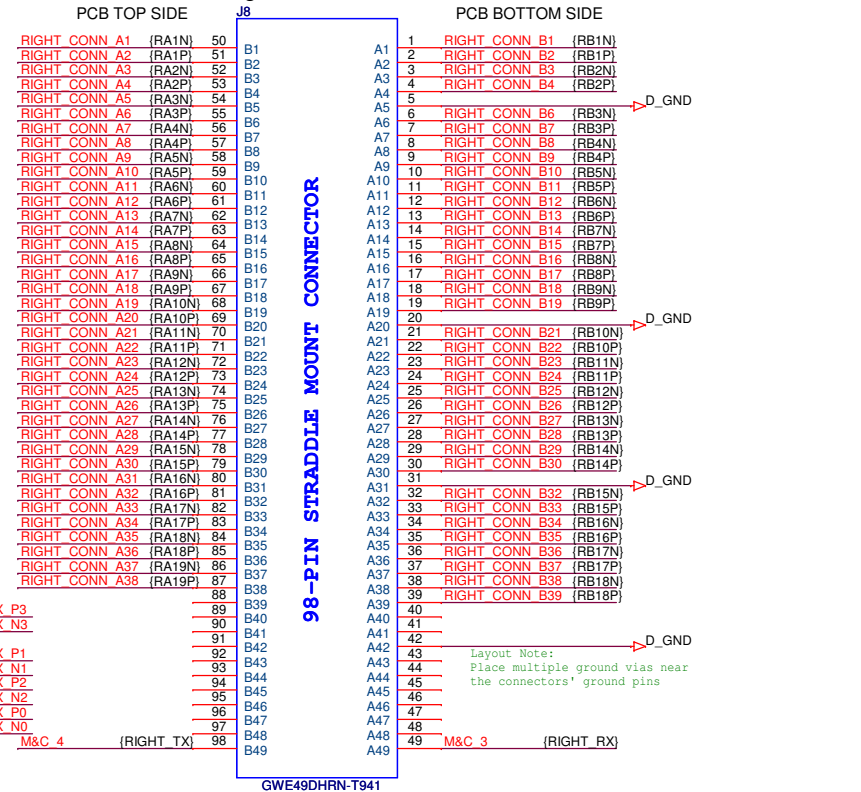


share pins A32-38 and B10-B16  
(for compatibility with COM-30xx,  
COM-5102, etc)

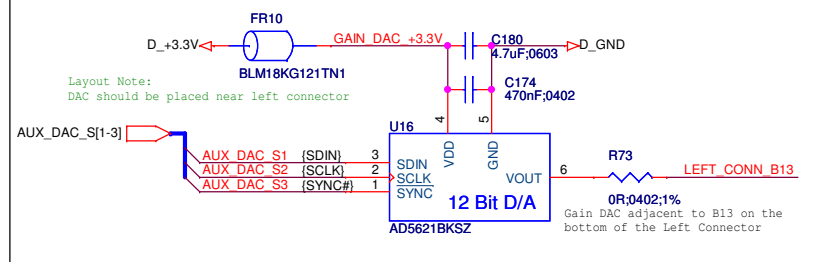
## Left Side Connector



## Right Side Connector



## Auxiliary DAC

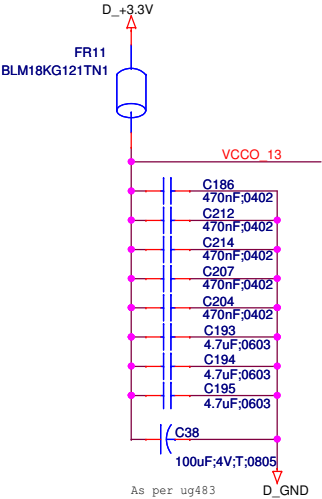


AK + AZ		
Mobile Satellite Services 18221A Flower Hill Way Gaithersburg, MD 20879 USA		
Title		
COM-1800 / CONNECTORS		
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B	Y14002	1
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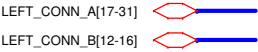




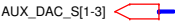
FPGA BANK 13, 3.3 I/O



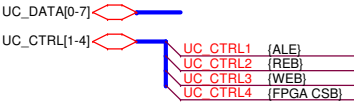
I/Os (LVCMOS33)



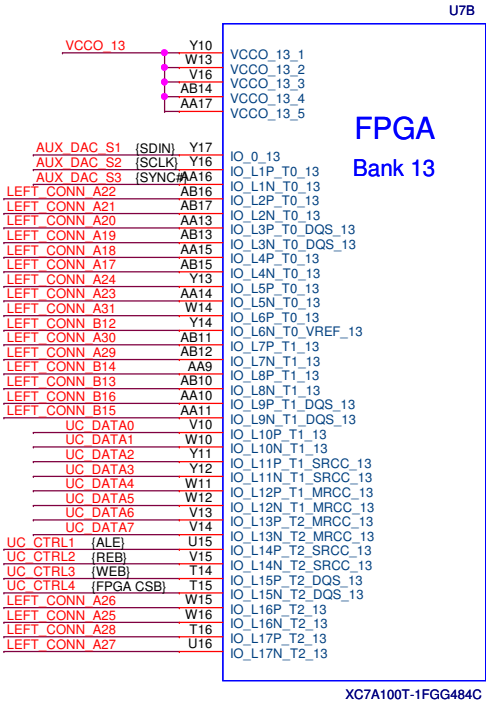
Auxiliary DAC



ARM - FPGA communication

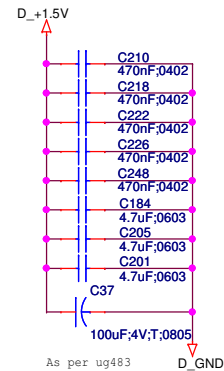


8-bit data bus shared by  
FPGA and NAND flash

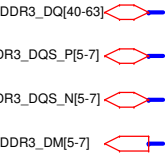


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Title		
COM-1800 / FPGA BANK13		
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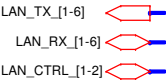
FPGA BANK 14, 1.5V I/O



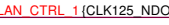
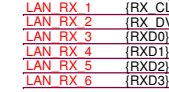
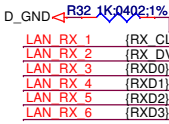
DDR3 SODIMM



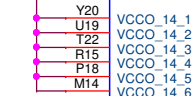
Ethernet LAN PHY



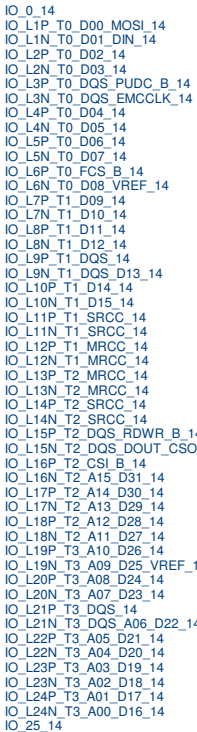
Pull-up during configuration#



D\_+1.5V



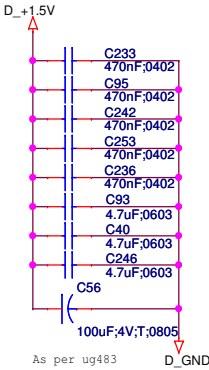
FPGA Bank 14



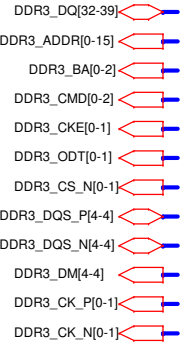
XC7A100T-1FGG484C

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COM-1800 /FPGA BANK14		
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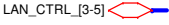
FPGA BANK 15, 1.5V I/O



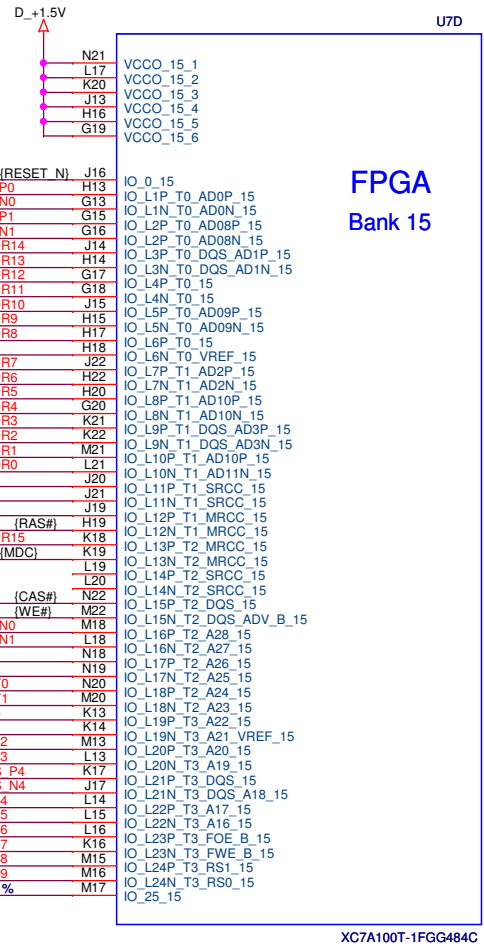
DDR3 SODIMM



Ethernet LAN PHY



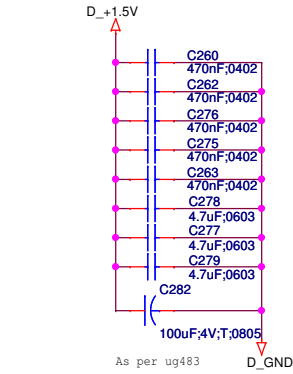
LAN_CTRL_3 (RESET_N)	J16	IO_0_15
DDR3_CK_P0	H13	IO_L1P_T0_AD0P_15
DDR3_CK_N0	G13	IO_L1N_T0_AD0N_15
DDR3_CK_P1	G15	IO_L2P_T0_AD08P_15
DDR3_CK_N1	G16	IO_L2P_T0_AD08N_15
DDR3_ADDR14	J14	IO_L3P_T0_DQS_AD1P_15
DDR3_ADDR13	H14	IO_L3N_T0_DQS_AD1N_15
DDR3_ADDR12	G17	IO_L4P_T0_15
DDR3_ADDR11	G18	IO_L4N_T0_15
DDR3_ADDR10	J15	IO_L5P_T0_AD09P_15
DDR3_ADDR9	H15	IO_L5N_T0_AD09N_15
DDR3_ADDR8	H17	IO_L6P_T0_15
	H18	IO_L6N_T0_VREF_15
DDR3_ADDR7	J22	IO_L7P_T1_AD2P_15
DDR3_ADDR6	H22	IO_L7N_T1_AD2N_15
DDR3_ADDR5	H20	IO_L8P_T1_AD10P_15
DDR3_ADDR4	G20	IO_L8N_T1_AD10N_15
DDR3_ADDR3	K21	IO_L9P_T1_DQS_AD3P_15
DDR3_ADDR2	K22	IO_L9N_T1_DQS_AD3N_15
DDR3_ADDR1	M21	IO_L10P_T1_AD10P_15
DDR3_ADDR0	L21	IO_L10N_T1_AD11N_15
DDR3_BA2	J20	IO_L11P_T1_SRCC_15
DDR3_BA1	J21	IO_L11N_T1_SRCC_15
DDR3_BA0	J19	IO_L12P_T1_MRCC_15
DDR3_CMD0 (RAS#)	H19	IO_L12N_T1_MRCC_15
DDR3_ADDR15	K18	IO_L13P_T2_MRCC_15
LAN_CTRL_4 (MDC)	K19	IO_L13N_T2_MRCC_15
	L19	IO_L14P_T2_SRCC_15
	L20	IO_L14N_T2_SRCC_15
DDR3_CMD1 (CAS#)	N22	IO_L15P_T2_DQS_15
DDR3_CMD2 (WE#)	M22	IO_L15N_T2_DQS_ADV_B_15
DDR3_CS_N0	M18	IO_L16P_T2_A28_15
DDR3_CS_N1	L18	IO_L16N_T2_A27_15
DDR3_CKE0	N18	IO_L17P_T2_A26_15
DDR3_CKE1	N19	IO_L17N_T2_A25_15
DDR3_ODT0	N20	IO_L18P_T2_A24_15
DDR3_ODT1	M20	IO_L18N_T2_A23_15
DDR3_DM4	K13	IO_L19P_T3_A22_15
	K14	IO_L19N_T3_A21_VREF_15
DDR3_DQ32	M13	IO_L20P_T3_A20_15
DDR3_DQ33	L13	IO_L20N_T3_A19_15
DDR3_DQS_P4	K17	IO_L21P_T3_DQS_15
DDR3_DQS_N4	J17	IO_L21N_T3_DQS_A18_15
DDR3_DQ34	L14	IO_L22P_T3_A17_15
DDR3_DQ35	L15	IO_L22N_T3_A16_15
DDR3_DQ36	L16	IO_L23P_T3_FOE_B_15
DDR3_DQ37	K16	IO_L23N_T3_FWE_B_15
DDR3_DQ38	M15	IO_L24P_T3_RS0_15
DDR3_DQ39	M16	IO_L24N_T3_RS0_15
LAN_CTRL_5 (MDIO)	R20	IO_25_15
	M17	



FPGA  
Bank 15

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Title		
COM-1800 / FPGA BANK15		
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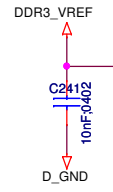
FPGA BANK 16, 1.5V I/O



DDR3 SODIMM



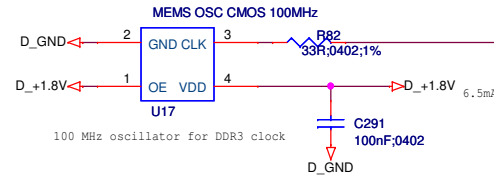
CLKREF\_TCXO  
19.2 MHz VC-TXCO for higher frequency stability



CLKREF\_EXT

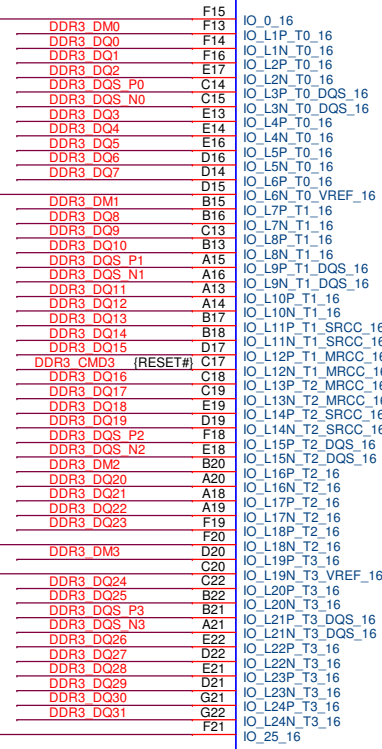
MEMS (silicon-only) oscillator

high gs, 20ppm over -40/+85C, 5ppm aging 1st year  
3.2x2.5mm footprint



VCCO\_16\_1  
VCCO\_16\_2  
VCCO\_16\_3  
VCCO\_16\_4  
VCCO\_16\_5  
VCCO\_16\_6

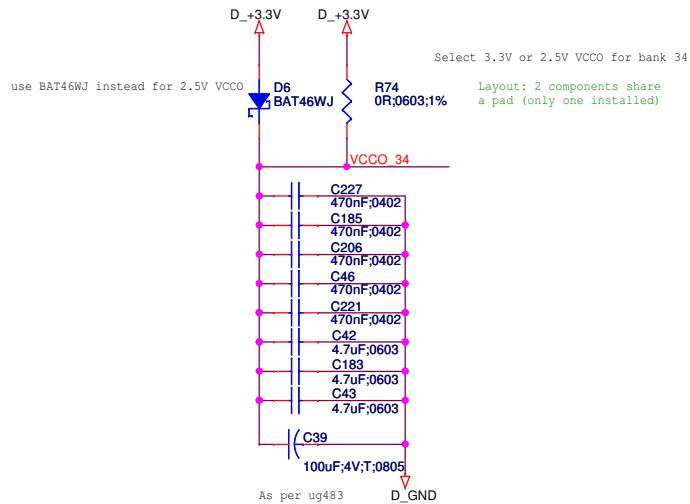
FPGA  
Bank 16



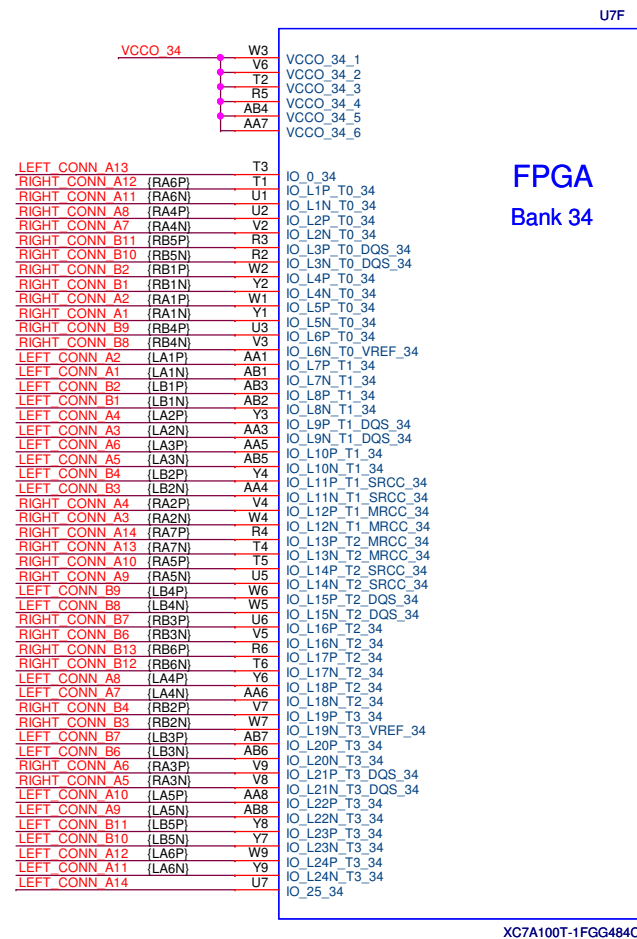
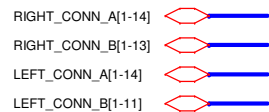
XC7A100T-1FGG484C

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COM-1800 / FPGA BANK16		
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# FPGA BANK 34, 2.5V or 3.3 I/O

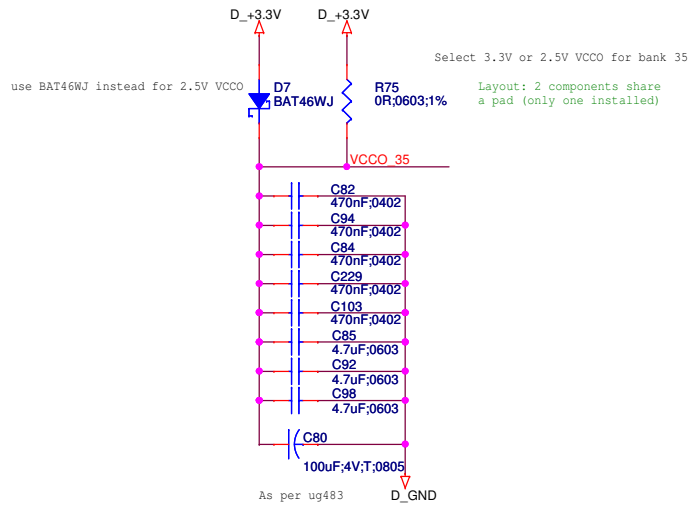


## I/Os (LVCMOS or LVDS)

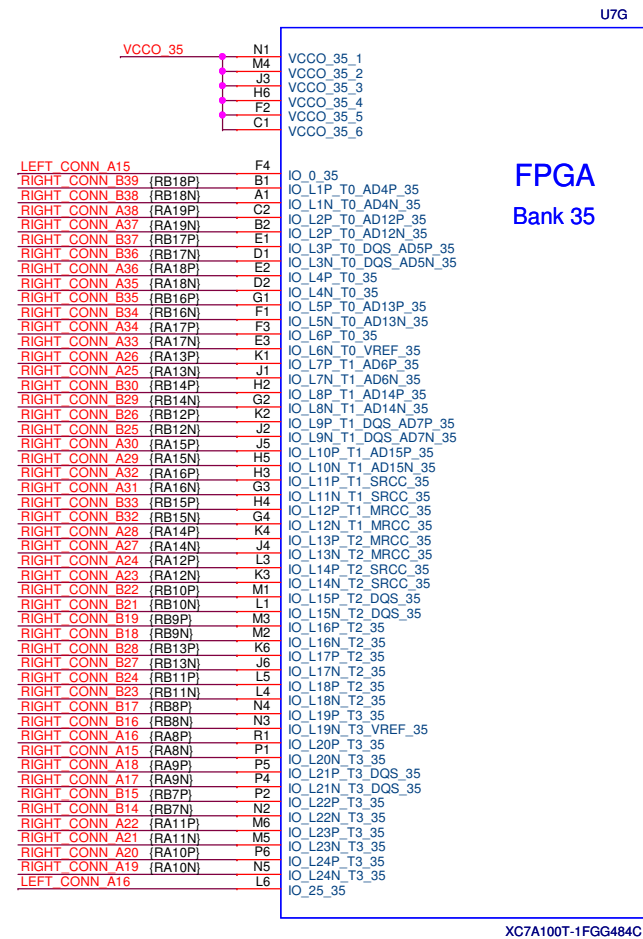
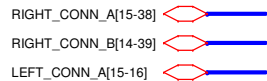


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COM-1800 / FPGA BANK34		
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FPGA BANK 35, 2.5V or 3.3 I/O



HIGH-SPEED LVCMOS or LVDS I/Os

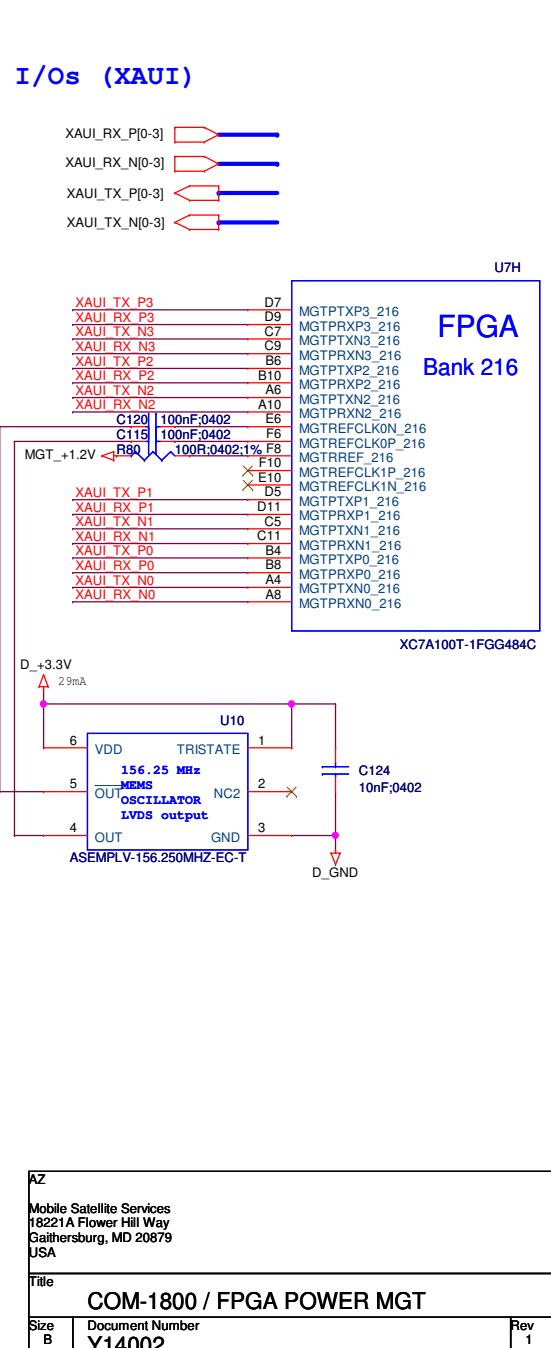
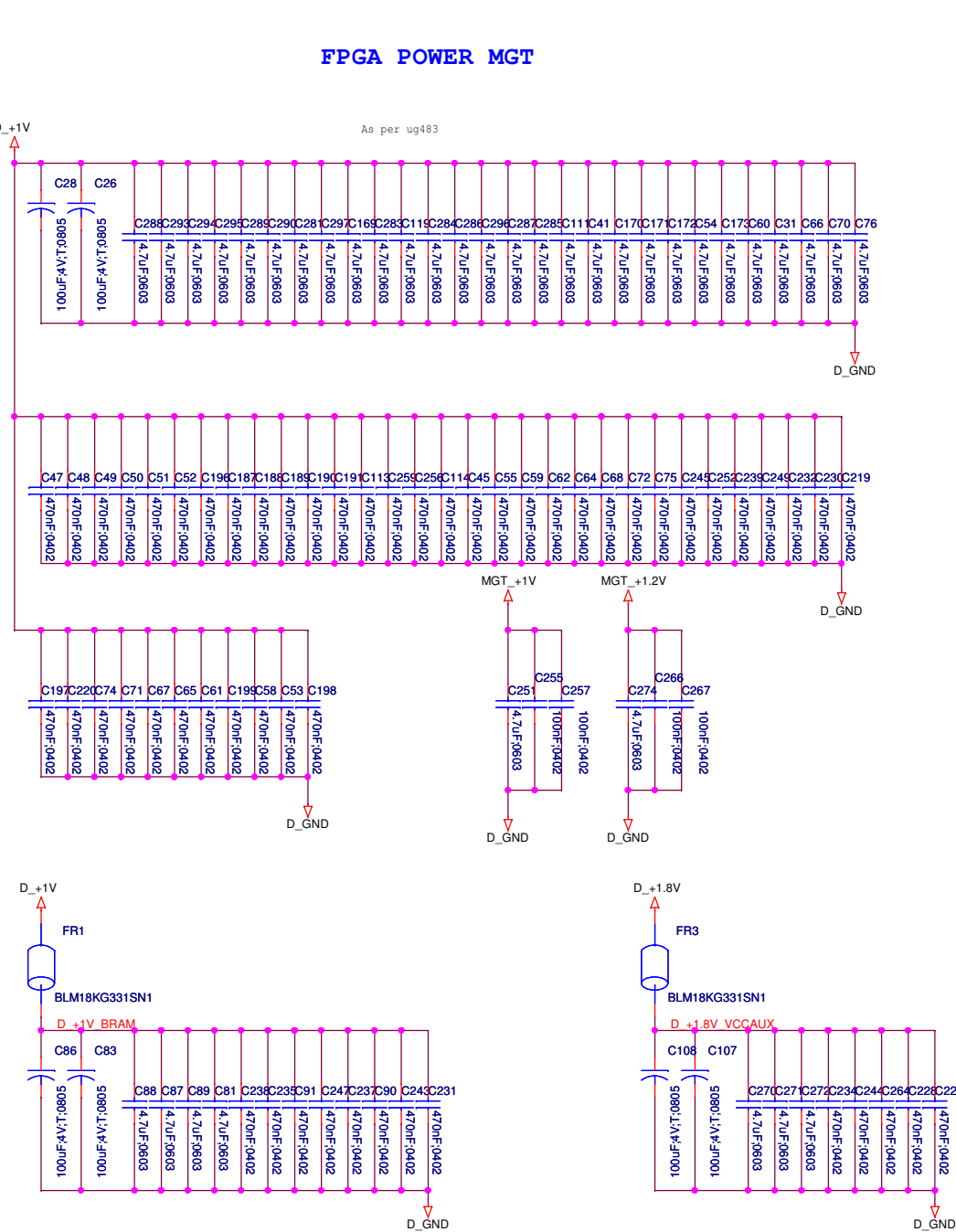
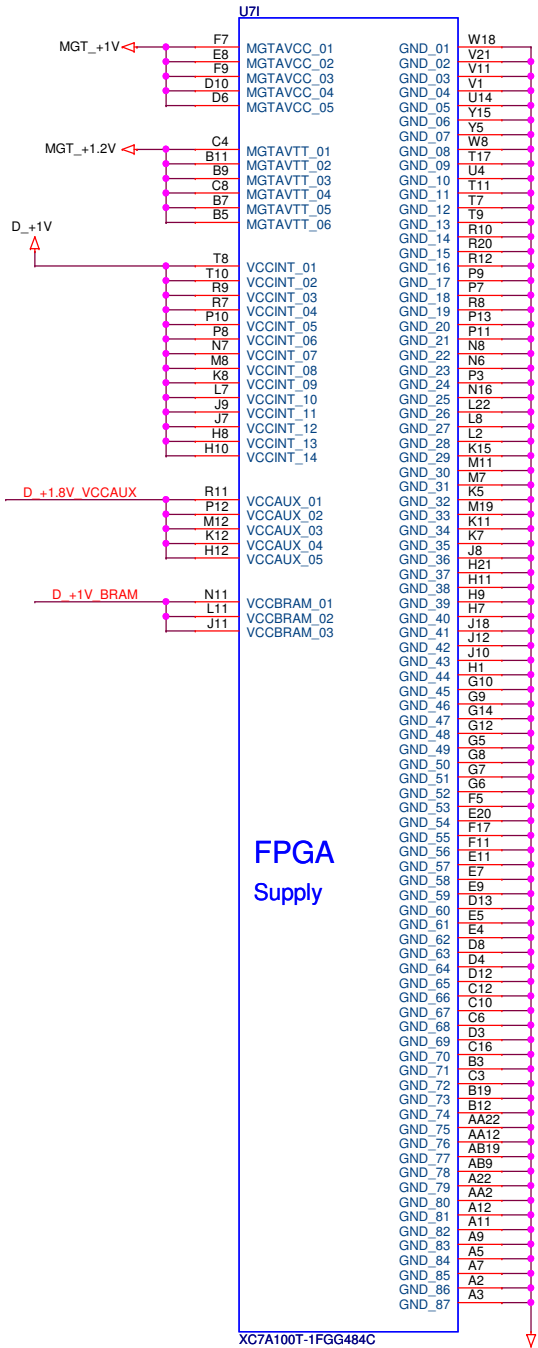


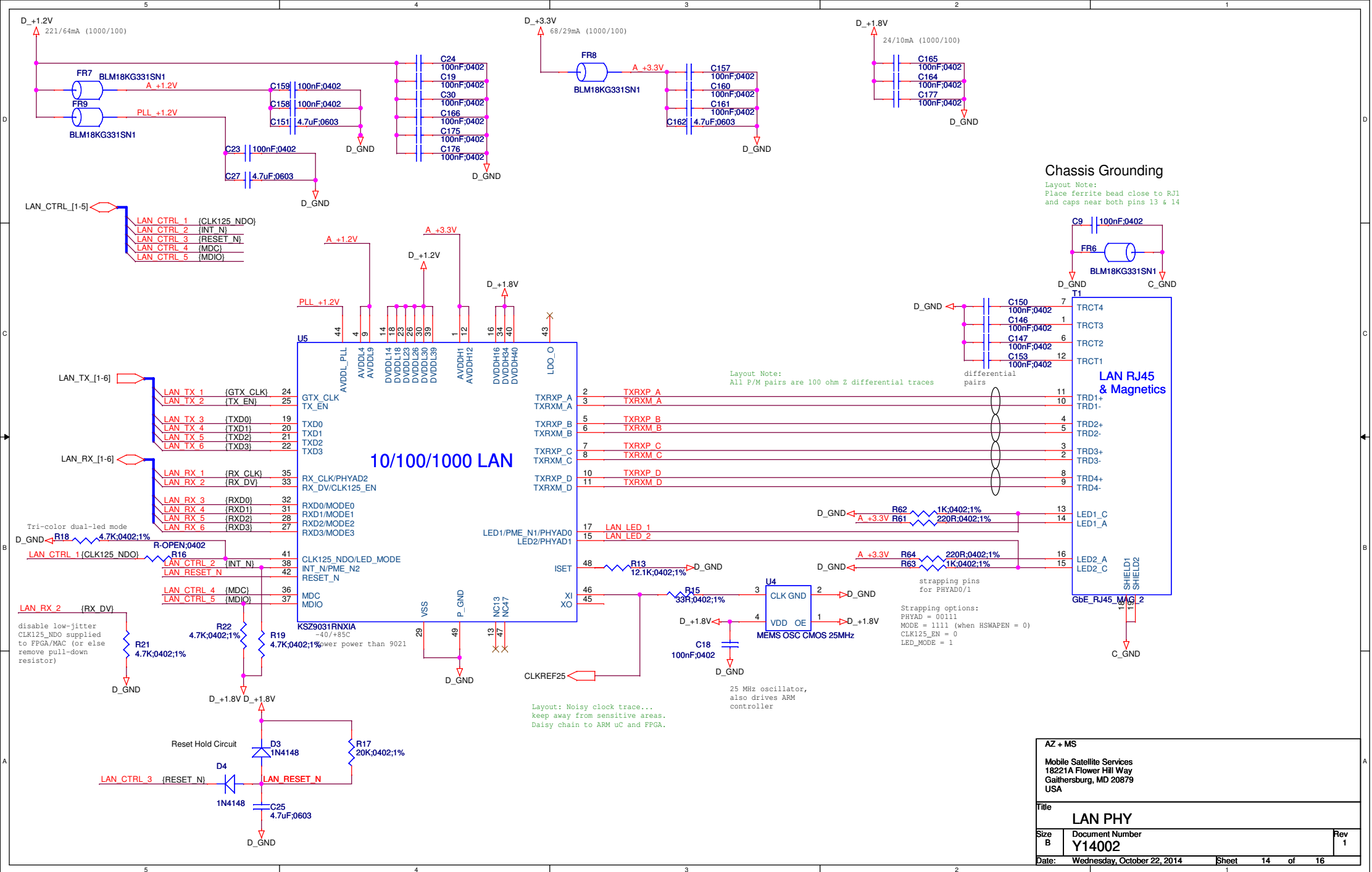
**AZ**  
**Mobile Satellite Services**  
**18221A Flower Hill Way**  
**Gaithersburg, MD 20879**  
**USA**

Title	COM-1800 / FPGA BANK35
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+5V DC Supply

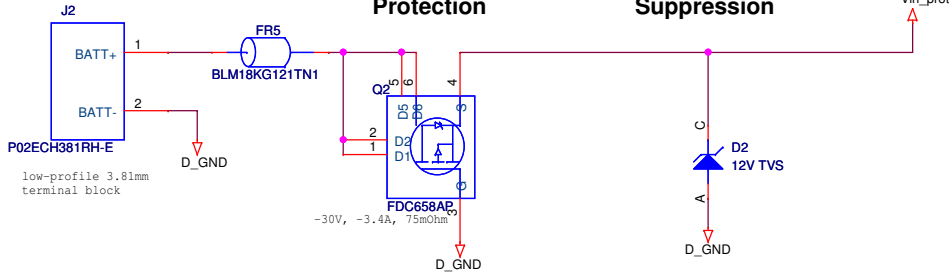
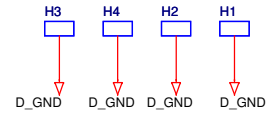
OPERATIONAL RANGE: 4.5 - 12V  
No damage: 20V max

### Filter

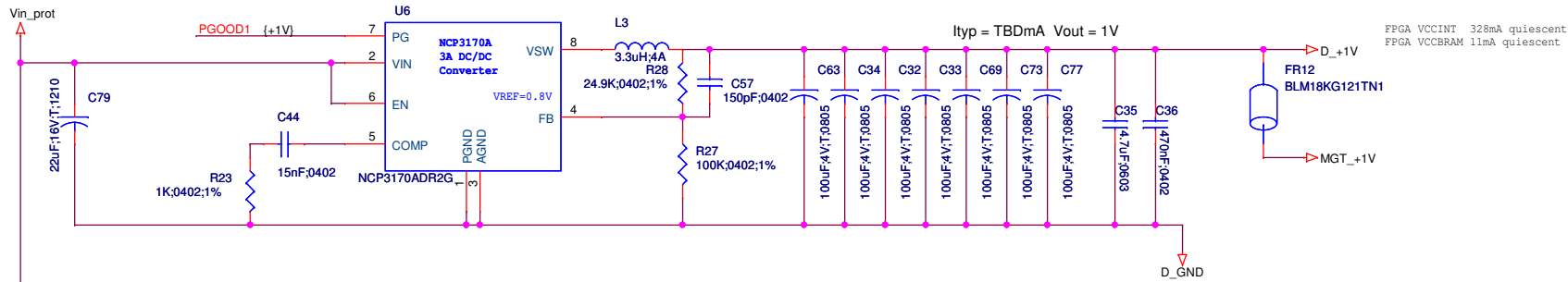
### Reverse Voltage Protection

### Transient Voltage Suppression

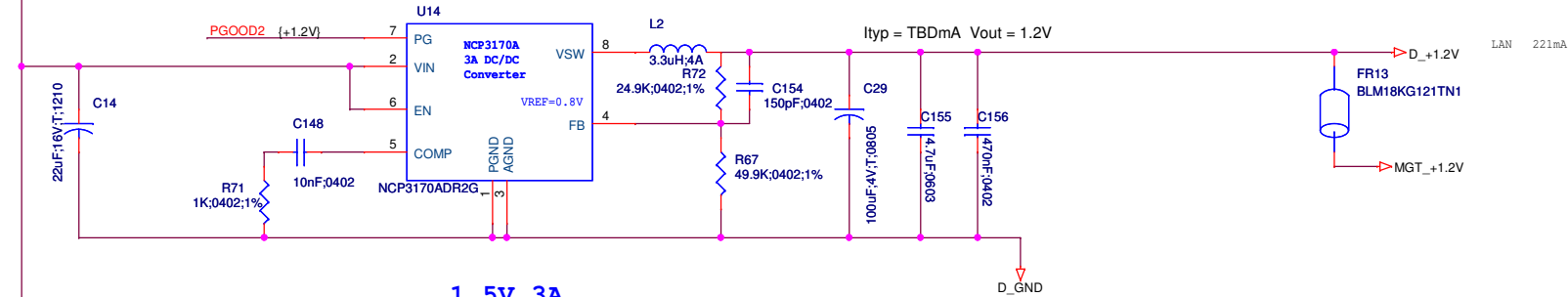
### PCB Mounting Holes



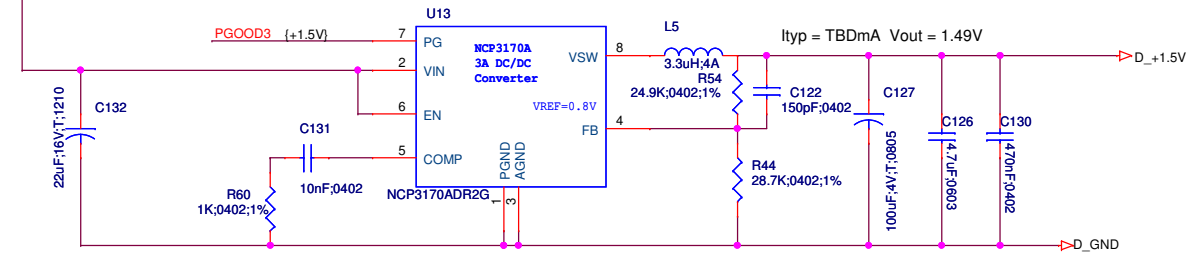
### 1V 3A



### 1.2V 3A



### 1.5V 3A



PGOOD[1-3] Power Good Indicators  
Must be pulled up by ARM processor

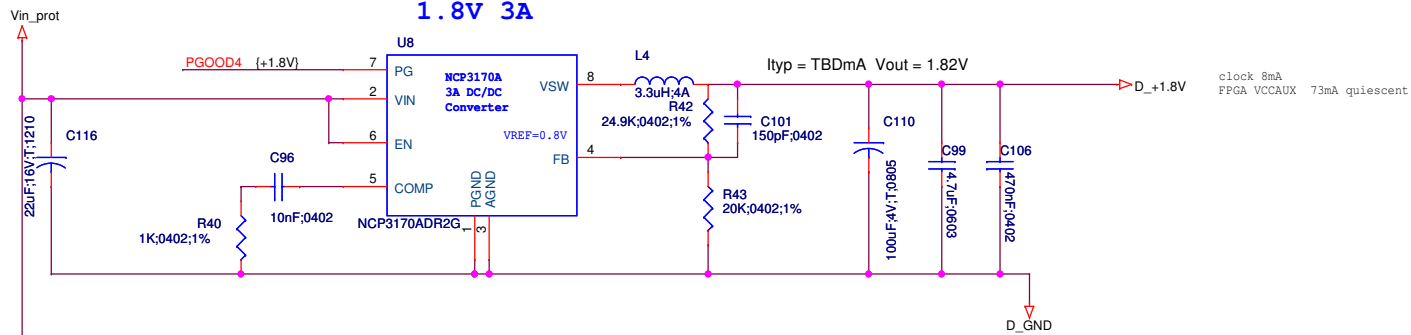
PGOOD1 (+1V)

PGOOD2 (+1.2V)

PGOOD3 (+1.5V)

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Mobile Satellite Services 18221A Flower Hill Way Gaithersburg, MD 20879 USA		
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COM-1800 / POWER1		
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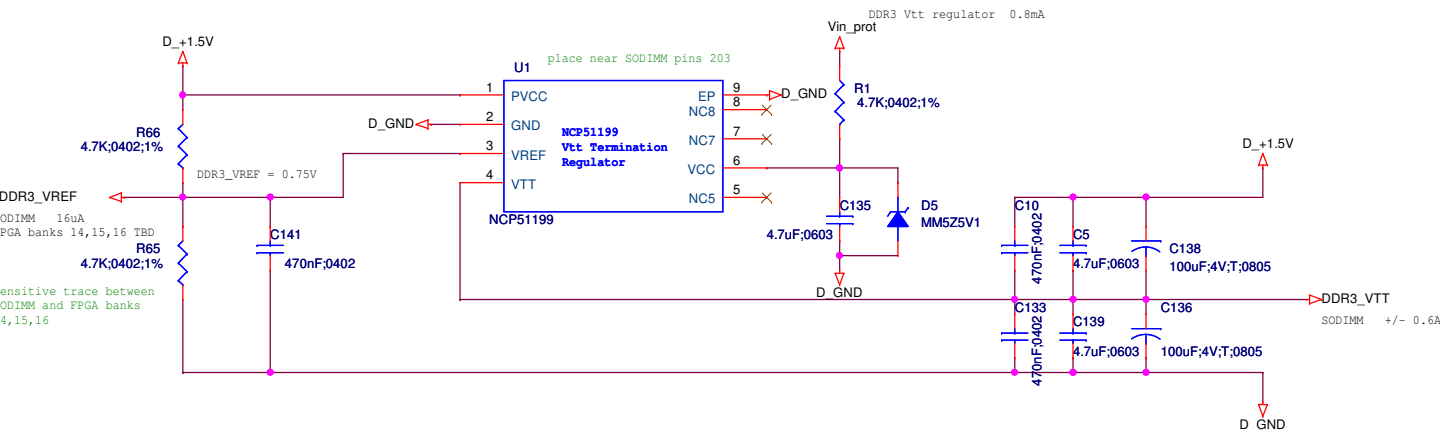
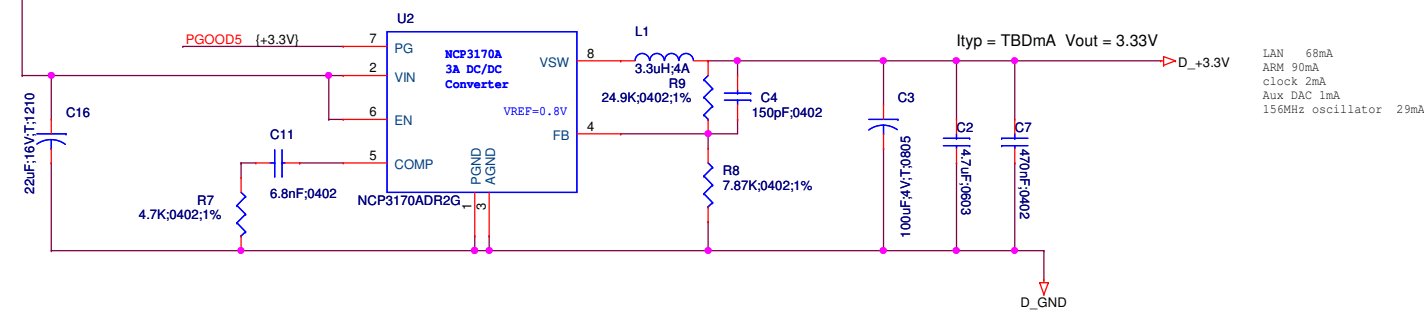
## 1.8V 3A



PGOOD[4-5] Power Good Indicators  
Must be pulled up by ARM processor

PGOOD4 (+1.8V)  
PGOOD5 (+3.3V)

## 3.3V 3A



Sensitive. 30mils trace between caps and pin.  
shield with gnd. other trace > 15mils away.

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