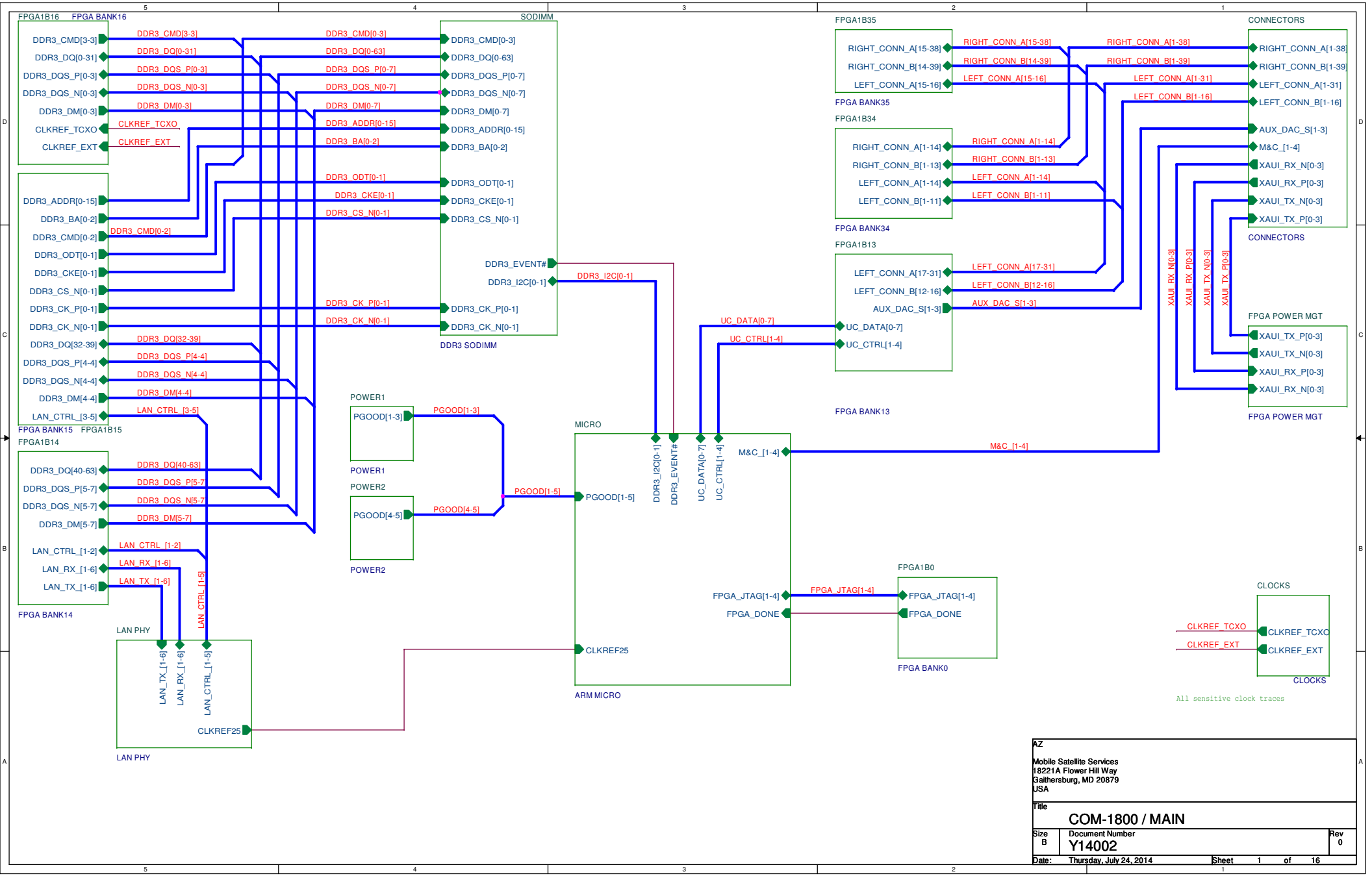

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Title: COM-1800 / MAIN

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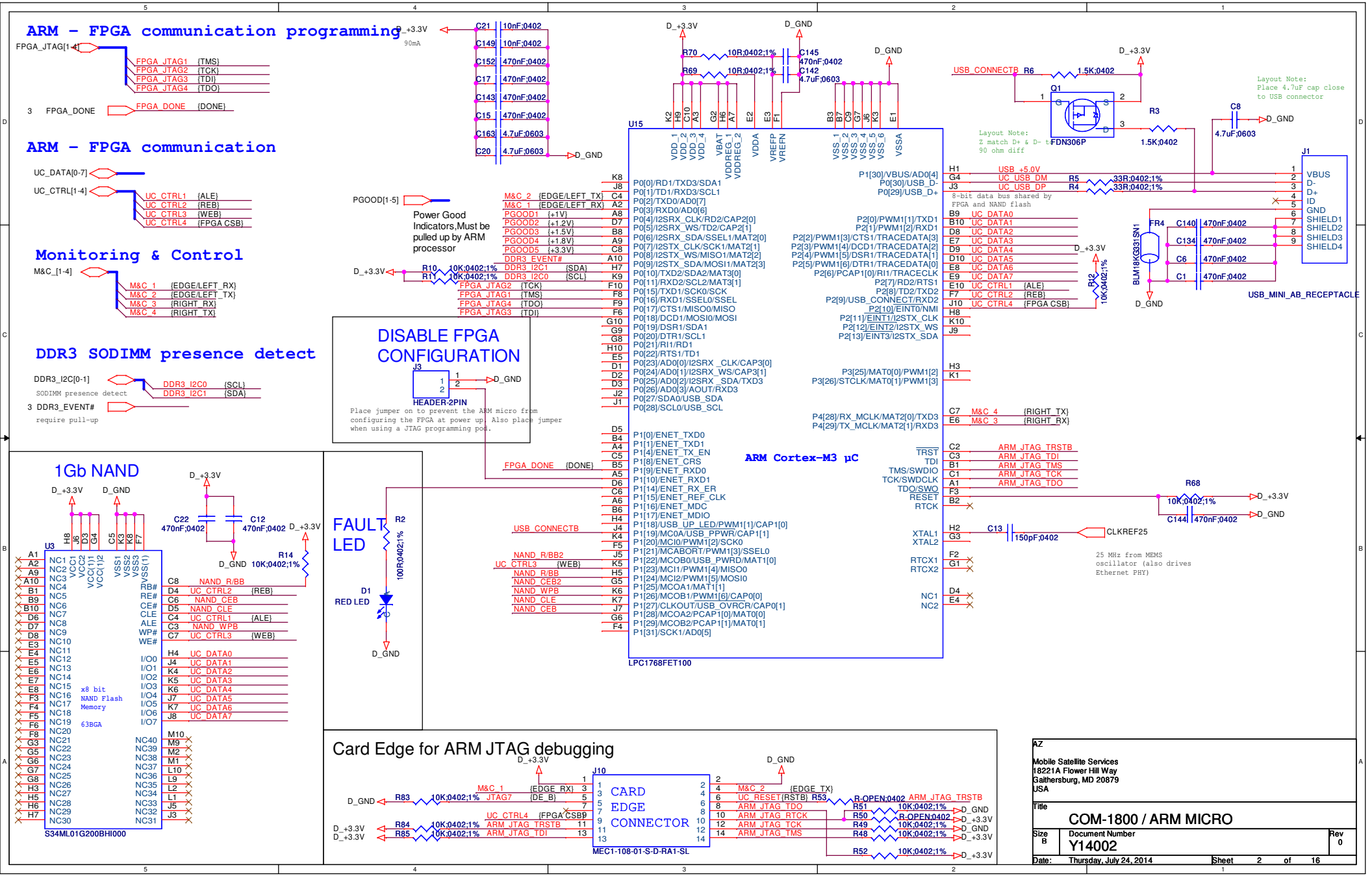
ARM – FPGA communication programming
FPGA_JTAG[1-4]
FPGA_JTAG1 {TMS}
FPGA_JTAG2 {TCK}
FPGA_JTAG3 {TDI}
FPGA_JTAG4 {TDO}
3 FPGA_DONE
FPGA_DONE {DONE}
ARM – FPGA communication
UC_DATA[0-7]
UC_CTRL[1-4]
UC_CTRL1 {ALE}
UC_CTRL2 {REB}
UC_CTRL3 {WEB}
UC_CTRL4 {FPGA CSB}
Monitoring & Control
M&C_[1-4]
M&C_1 {EDGE/LEFT_RX}
M&C_2 {EDGE/LEFT_TX}
M&C_3 {RIGHT_RX}
M&C_4 {RIGHT_TX}
DDR3 SODIMM presence detect
DDR3_I2C[0-1]
SODIMM presence detect
DDR3_I2C0 {SCL}
DDR3_I2C1 {SDA}
3 DDR3_EVENT#
require pull-up
1Gb NAND
U3
S34ML01G200BHI000
x8 bit NAND Flash Memory
63BGA
C22 470nF;0402
C12 470nF;0402
R14 10K;0402;1%
C8 NAND_R/BB
D4 UC_CTRL2 {REB}
C6 NAND_CEB
D5 NAND_CLE
C4 UC_CTRL1 {ALE}
C3 NAND_WPB
C7 UC_CTRL3 {WEB}
H4 UC_DATA0
J4 UC_DATA1
K4 UC_DATA2
K5 UC_DATA3
K6 UC_DATA4
J7 UC_DATA5
K7 UC_DATA6
J8 UC_DATA7
FAULT LED
R2 100R;0402;1%
D1 RED LED
C21 10nF;0402
C149 10nF;0402
C152 470nF;0402
C17 470nF;0402
C143 470nF;0402
C15 470nF;0402
C163 4.7uF;0603
C20 4.7uF;0603
90mA
PGOOD[1-5]
Power Good Indicators,Must be pulled up by ARM processor
M&C_2 {EDGE/LEFT_TX}
M&C_1 {EDGE/LEFT_RX}
PGOOD1 {+1V}
PGOOD2 {+1.2V}
PGOOD3 {+1.5V}
PGOOD4 {+1.8V}
PGOOD5 {+3.3V}
DDR3_EVENT#
R10 10K;0402;1%
R11 10K;0402;1%
DDR3_I2C1 {SDA}
DDR3_I2C0 {SCL}
FPGA_JTAG2 {TCK}
FPGA_JTAG1 {TMS}
FPGA_JTAG4 {TDO}
FPGA_JTAG3 {TDI}
DISABLE FPGA CONFIGURATION
J3
HEADER-2PIN
Place jumper on to prevent the ARM micro from configuring the FPGA at power up. Also place jumper when using a JTAG programming pod.
FPGA_DONE {DONE}
R70 10R;0402;1%
R69 10R;0402;1%
C145 470nF;0402
C142 4.7uF;0603
U15
ARM Cortex-M3 µC
LPC1768FET100
P0[0]/RD1/TXD3/SDA1
P0[1]/TD1/RXD3/SCL1
P0[2]/TXD0/AD0[7]
P0[3]/RXD0/AD0[6]
P0[4]/I2SRX_CLK/RD2/CAP2[0]
P0[5]/I2SRX_WS/TD2/CAP2[1]
P0[6]/I2SRX_SDA/SSEL1/MAT2[0]
P0[7]/I2STX_CLK/SCK1/MAT2[1]
P0[8]/I2STX_WS/MISO1/MAT2[2]
P0[9]/I2STX_SDA/MOSI1/MAT2[3]
P0[10]/TXD2/SDA2/MAT3[0]
P0[11]/RXD2/SCL2/MAT3[1]
P0[15]/TXD1/SCK0/SCK
P0[16]/RXD1/SSEL0/SSEL
P0[17]/CTS1/MISO0/MISO
P0[18]/DCD1/MOSI0/MOSI
P0[19]/DSR1/SDA1
P0[20]/DTR1/SCL1
P0[21]/RI1/RD1
P0[22]/RTS1/TD1
P0[23]/AD0[0]/I2SRX_CLK/CAP3[0]
P0[24]/AD0[1]/I2SRX_WS/CAP3[1]
P0[25]/AD0[2]/I2SRX_SDA/TXD3
P0[26]/AD0[3]/AOUT/RXD3
P0[27]/SDA0/USB_SDA
P0[28]/SCL0/USB_SCL
P1[0]/ENET_TXD0
P1[1]/ENET_TXD1
P1[4]/ENET_TX_EN
P1[8]/ENET_CRS
P1[9]/ENET_RXD0
P1[10]/ENET_RXD1
P1[14]/ENET_RX_ER
P1[15]/ENET_REF_CLK
P1[16]/ENET_MDC
P1[17]/ENET_MDIO
P1[18]/USB_UP_LED/PWM1[1]/CAP1[0]
P1[19]/MC0A/USB_PPWR/CAP1[1]
P1[20]/MCI0/PWM1[2]/SCK0
P1[21]/MCABORT/PWM1[3]/SSEL0
P1[22]/MCOB0/USB_PWRD/MAT1[0]
P1[23]/MCI1/PWM1[4]/MISO0
P1[24]/MCI2/PWM1[5]/MOSI0
P1[25]/MCOA1/MAT1[1]
P1[26]/MCOB1/PWM1[6]/CAP0[0]
P1[27]/CLKOUT/USB_OVRCR/CAP0[1]
P1[28]/MCOA2/PCAP1[0]/MAT0[0]
P1[29]/MCOB2/PCAP1[1]/MAT0[1]
P1[31]/SCK1/AD0[5]
P1[30]/VBUS/AD0[4]
P0[30]/USB_D-
P0[29]/USB_D+
P2[0]/PWM1[1]/TXD1
P2[1]/PWM1[2]/RXD1
P2[2]/PWM1[3]/CTS1/TRACEDATA[3]
P2[3]/PWM1[4]/DCD1/TRACEDATA[2]
P2[4]/PWM1[5]/DSR1/TRACEDATA[1]
P2[5]/PWM1[6]/DTR1/TRACEDATA[0]
P2[6]/PCAP1[0]/RI1/TRACECLK
P2[7]/RD2/RTS1
P2[8]/TD2/TXD2
P2[9]/USB_CONNECT/RXD2
P2[10]/EINT0/NMI
P2[11]/EINT1/I2STX_CLK
P2[12]/EINT2/I2STX_WS
P2[13]/EINT3/I2STX_SDA
P3[25]/MAT0[0]/PWM1[2]
P3[26]/STCLK/MAT0[1]/PWM1[3]
P4[28]/RX_MCLK/MAT2[0]/TXD3
P4[29]/TX_MCLK/MAT2[1]/RXD3
TRST
TDI
TMS/SWDIO
TCK/SWDCLK
TDO/SWO
RESET
RTCK
XTAL1
XTAL2
RTCX1
RTCX2
NC1
NC2
USB_CONNECTB
NAND_R/BB2
UC_CTRL3 {WEB}
NAND_R/BB
NAND_CEB2
NAND_WPB
NAND_CLE
NAND_CEB
USB_CONNECTB R6 1.5K;0402
Q1
FDN306P
R3 1.5K;0402
C8 4.7uF;0603
Layout Note: Place 4.7uF cap close to USB connector
Layout Note: Z match D+ & D- to 90 ohm diff
J1
USB_MINI_AB_RECEPTACLE
USB +5.0V
UC_USB_DM
UC_USB_DP
R5 33R;0402;1%
R4 33R;0402;1%
8-bit data bus shared by FPGA and NAND flash
UC_DATA0
UC_DATA1
UC_DATA2
UC_DATA3
UC_DATA4
UC_DATA5
UC_DATA6
UC_DATA7
UC_CTRL1 {ALE}
UC_CTRL2 {REB}
UC_CTRL4 {FPGA CSB}
R12 10K;0402;1%
FR4
BLM18KG331SN1
C140 470nF;0402
C134 470nF;0402
C6 470nF;0402
C1 470nF;0402
M&C_4 {RIGHT_TX}
M&C_3 {RIGHT_RX}
ARM_JTAG_TRSTB
ARM_JTAG_TDI
ARM_JTAG_TMS
ARM_JTAG_TCK
ARM_JTAG_TDO
R68 10K;0402;1%
C144 470nF;0402
C13 150pF;0402
CLKREF25
25 MHz from MEMS oscillator (also drives Ethernet PHY)
Card Edge for ARM JTAG debugging
J10
CARD EDGE CONNECTOR
MEC1-108-01-S-D-RA1-SL
R83 10K;0402;1%
R84 10K;0402;1%
R85 10K;0402;1%
JTAG7 {DE_B}
ARM_JTAG_TRSTB
ARM_JTAG_TDI
ARM_JTAG_TDO
ARM_JTAG_RTCK
ARM_JTAG_TCK
ARM_JTAG_TMS
R53 R-OPEN;0402
R51 10K;0402;1%
R50 R-OPEN;0402
R49 10K;0402;1%
R48 10K;0402;1%
R52 10K;0402;1%
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Title
COM-1800 / ARM MICRO
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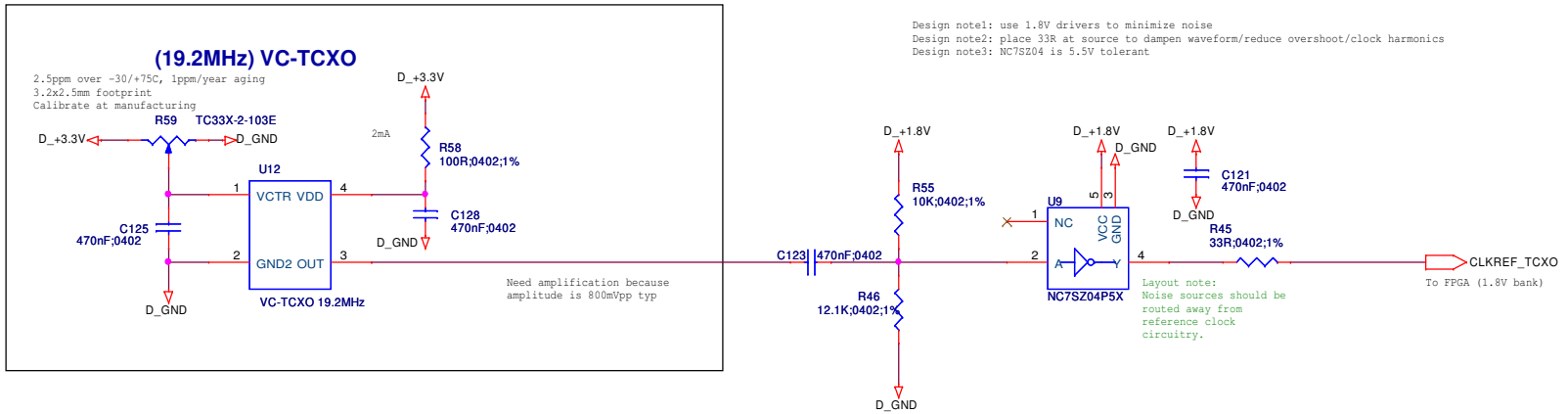
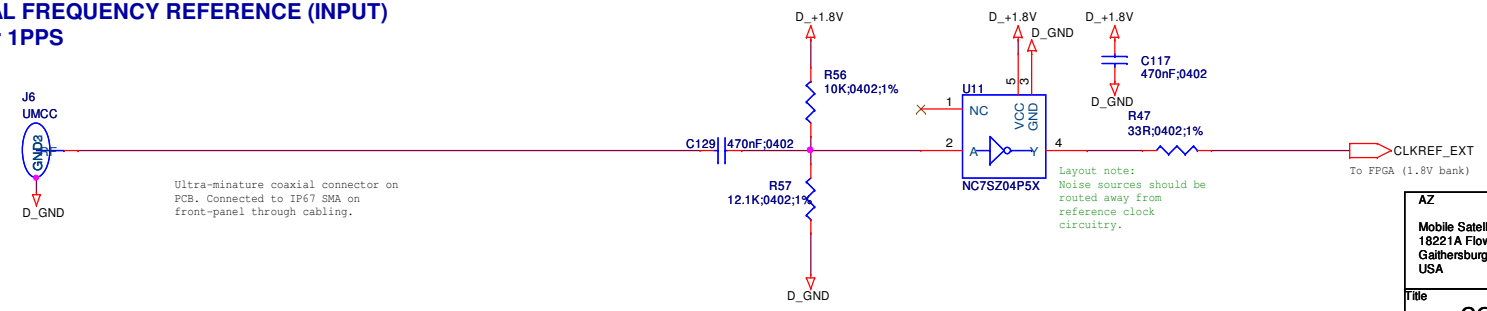


EXTERNAL FREQUENCY REFERENCE (INPUT)
10 MHz or 1PPS



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COM-1800 CLOCKS

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I/Os (LVCMOS or LVDS)

LEFT_CONN_A[1-31]
LEFT_CONN_B[1-16]
RIGHT_CONN_A[1-38]
RIGHT_CONN_B[1-39]

I/Os (XAUI)

XAUI_TX_P[0-3]
XAUI_TX_N[0-3]
XAUI_RX_P[0-3]
XAUI_RX_N[0-3]

Monitoring & Control

M&C_[1-4]

M&C_1 {EDGE/LEFT_RX}
M&C_2 {EDGE/LEFT_TX}
M&C_3 {RIGHT_RX}
M&C_4 {RIGHT_TX}

share pins A32-38 and B10-B16
(for compatibility with COM-30xx,
COM-5102, etc)

Left Side Connector

PCB TOP SIDE / PCB BOTTOM SIDE

J4 — 98-PIN STRADDLE MOUNT CONNECTOR — GWE49DHRN-T941

LEFT_CONN_A1	{LA1N}	1	50	LEFT_CONN_B1	{LB1N}
LEFT_CONN_A2	{LA1P}	2	51	LEFT_CONN_B2	{LB1P}
LEFT_CONN_A3	{LA2N}	3	52	LEFT_CONN_B3	{LB2N}
LEFT_CONN_A4	{LA2P}	4	53	LEFT_CONN_B4	{LB2P}
LEFT_CONN_A5	{LA3N}	5	54		
LEFT_CONN_A6	{LA3P}	6	55	LEFT_CONN_B6	{LB3N}
LEFT_CONN_A7	{LA4N}	7	56	LEFT_CONN_B7	{LB3P}
LEFT_CONN_A8	{LA4P}	8	57	LEFT_CONN_B8	{LB4N}
LEFT_CONN_A9	{LA5N}	9	58	LEFT_CONN_B9	{LB4P}
LEFT_CONN_A10	{LA5P}	10	59	LEFT_CONN_B10	{LB5N}
LEFT_CONN_A11	{LA6N}	11	60	LEFT_CONN_B11	{LB5P}
LEFT_CONN_A12	{LA6P}	12	61	LEFT_CONN_B12	
LEFT_CONN_A13		13	62	LEFT_CONN_B13	
LEFT_CONN_A14		14	63	LEFT_CONN_B14	
LEFT_CONN_A15		15	64	LEFT_CONN_B15	
LEFT_CONN_A16		16	65	LEFT_CONN_B16	
LEFT_CONN_A17		17	66		
LEFT_CONN_A18		18	67		
LEFT_CONN_A19		19	68		
LEFT_CONN_A20		20	69	D_GND	
LEFT_CONN_A21		21	70		
LEFT_CONN_A22		22	71		
LEFT_CONN_A23		23	72		
LEFT_CONN_A24		24	73		
LEFT_CONN_A25		25	74		
LEFT_CONN_A26		26	75		
LEFT_CONN_A27		27	76		
LEFT_CONN_A28		28	77		
LEFT_CONN_A29		29	78		
LEFT_CONN_A30		30	79		
LEFT_CONN_A31		31	80	D_GND	
LEFT_CONN_A32		32	81		
LEFT_CONN_A33		33	82		
LEFT_CONN_A34		34	83		
LEFT_CONN_A35		35	84		
LEFT_CONN_A36		36	85		
LEFT_CONN_A37		37	86		
LEFT_CONN_A38		38	87		
		39	88		
		40	89	100nF;0402 C250	XAUI_RX_P3
		41	90	100nF;0402 C254	XAUI_RX_N3
		42	91		D_GND
		43	92	100nF;0402 C258	XAUI_RX_P1
		44	93	100nF;0402 C261	XAUI_RX_N1
		45	94	100nF;0402 C265	XAUI_RX_P2
		46	95	100nF;0402 C269	XAUI_RX_N2
		47	96	100nF;0402 C273	XAUI_RX_P0
		48	97	100nF;0402 C280	XAUI_RX_N0
M&C_1	{LEFT_RX}	49	98	M&C_2	{LEFT_TX}

LEFT_CONN_B10 {LB5N}
LEFT_CONN_B11 {LB9P}

XAUI_TX_P3 C97 100nF;0402
XAUI_TX_N3 C100 100nF;0402
XAUI_TX_P1 C102 100nF;0402
XAUI_TX_N1 C104 100nF;0402
XAUI_TX_P2 C105 100nF;0402
XAUI_TX_N2 C109 100nF;0402
XAUI_TX_P0 C112 100nF;0402
XAUI_TX_N0 C118 100nF;0402

Layout Note:
Place multiple ground vias near
the connectors' ground pins

Right Side Connector

PCB TOP SIDE / PCB BOTTOM SIDE

J8 — 98-PIN STRADDLE MOUNT CONNECTOR — GWE49DHRN-T941

RIGHT_CONN_A1	{RA1N}	50	1	RIGHT_CONN_B1	{RB1N}
RIGHT_CONN_A2	{RA1P}	51	2	RIGHT_CONN_B2	{RB1P}
RIGHT_CONN_A3	{RA2N}	52	3	RIGHT_CONN_B3	{RB2N}
RIGHT_CONN_A4	{RA2P}	53	4	RIGHT_CONN_B4	{RB2P}
RIGHT_CONN_A5	{RA3N}	54	5		
RIGHT_CONN_A6	{RA3P}	55	6	RIGHT_CONN_B6	{RB3N}
RIGHT_CONN_A7	{RA4N}	56	7	RIGHT_CONN_B7	{RB3P}
RIGHT_CONN_A8	{RA4P}	57	8	RIGHT_CONN_B8	{RB4N}
RIGHT_CONN_A9	{RA5N}	58	9	RIGHT_CONN_B9	{RB4P}
RIGHT_CONN_A10	{RA5P}	59	10	RIGHT_CONN_B10	{RB5N}
RIGHT_CONN_A11	{RA6N}	60	11	RIGHT_CONN_B11	{RB5P}
RIGHT_CONN_A12	{RA6P}	61	12	RIGHT_CONN_B12	{RB6N}
RIGHT_CONN_A13	{RA7N}	62	13	RIGHT_CONN_B13	{RB6P}
RIGHT_CONN_A14	{RA7P}	63	14	RIGHT_CONN_B14	{RB7N}
RIGHT_CONN_A15	{RA8N}	64	15	RIGHT_CONN_B15	{RB7P}
RIGHT_CONN_A16	{RA8P}	65	16	RIGHT_CONN_B16	{RB8N}
RIGHT_CONN_A17	{RA9N}	66	17	RIGHT_CONN_B17	{RB8P}
RIGHT_CONN_A18	{RA9P}	67	18	RIGHT_CONN_B18	{RB9N}
RIGHT_CONN_A19	{RA10N}	68	19	RIGHT_CONN_B19	{RB9P}
RIGHT_CONN_A20	{RA10P}	69	20		D_GND
RIGHT_CONN_A21	{RA11N}	70	21	RIGHT_CONN_B21	{RB10N}
RIGHT_CONN_A22	{RA11P}	71	22	RIGHT_CONN_B22	{RB10P}
RIGHT_CONN_A23	{RA12N}	72	23	RIGHT_CONN_B23	{RB11N}
RIGHT_CONN_A24	{RA12P}	73	24	RIGHT_CONN_B24	{RB11P}
RIGHT_CONN_A25	{RA13N}	74	25	RIGHT_CONN_B25	{RB12N}
RIGHT_CONN_A26	{RA13P}	75	26	RIGHT_CONN_B26	{RB12P}
RIGHT_CONN_A27	{RA14N}	76	27	RIGHT_CONN_B27	{RB13N}
RIGHT_CONN_A28	{RA14P}	77	28	RIGHT_CONN_B28	{RB13P}
RIGHT_CONN_A29	{RA15N}	78	29	RIGHT_CONN_B29	{RB14N}
RIGHT_CONN_A30	{RA15P}	79	30	RIGHT_CONN_B30	{RB14P}
RIGHT_CONN_A31	{RA16N}	80	31		D_GND
RIGHT_CONN_A32	{RA16P}	81	32	RIGHT_CONN_B32	{RB15N}
RIGHT_CONN_A33	{RA17N}	82	33	RIGHT_CONN_B33	{RB15P}
RIGHT_CONN_A34	{RA17P}	83	34	RIGHT_CONN_B34	{RB16N}
RIGHT_CONN_A35	{RA18N}	84	35	RIGHT_CONN_B35	{RB16P}
RIGHT_CONN_A36	{RA18P}	85	36	RIGHT_CONN_B36	{RB17N}
RIGHT_CONN_A37	{RA19N}	86	37	RIGHT_CONN_B37	{RB17P}
RIGHT_CONN_A38	{RA19P}	87	38	RIGHT_CONN_B38	{RB18N}
		88	39	RIGHT_CONN_B39	{RB18P}
		89	40		
		90	41		
		91	42		D_GND
		92	43		
		93	44		
		94	45		
		95	46		
		96	47		
		97	48		
M&C_4	{RIGHT_TX}	98	49	M&C_3	{RIGHT_RX}

Layout Note:
Place multiple ground vias near
the connectors' ground pins

Auxiliary DAC

D_+3.3V — FR10 BLM18KG121TN1 — GAIN_DAC_+3.3V

C180 4.7uF;0603 D_GND
C174 470nF;0402

Layout Note:
DAC should be placed near left connector

AUX_DAC_S[1-3]

AUX_DAC_S1 {SDIN} 3
AUX_DAC_S2 {SCLK} 2
AUX_DAC_S3 {SYNC#} 1

U16 AD5621BKSZ — SDIN, SCLK, SYNC, VDD, GND, VOUT — 12 Bit D/A

R73 0R;0402;1% — LEFT_CONN_B13

Gain DAC adjacent to B13 on the
bottom of the Left Connector

AK + AZ

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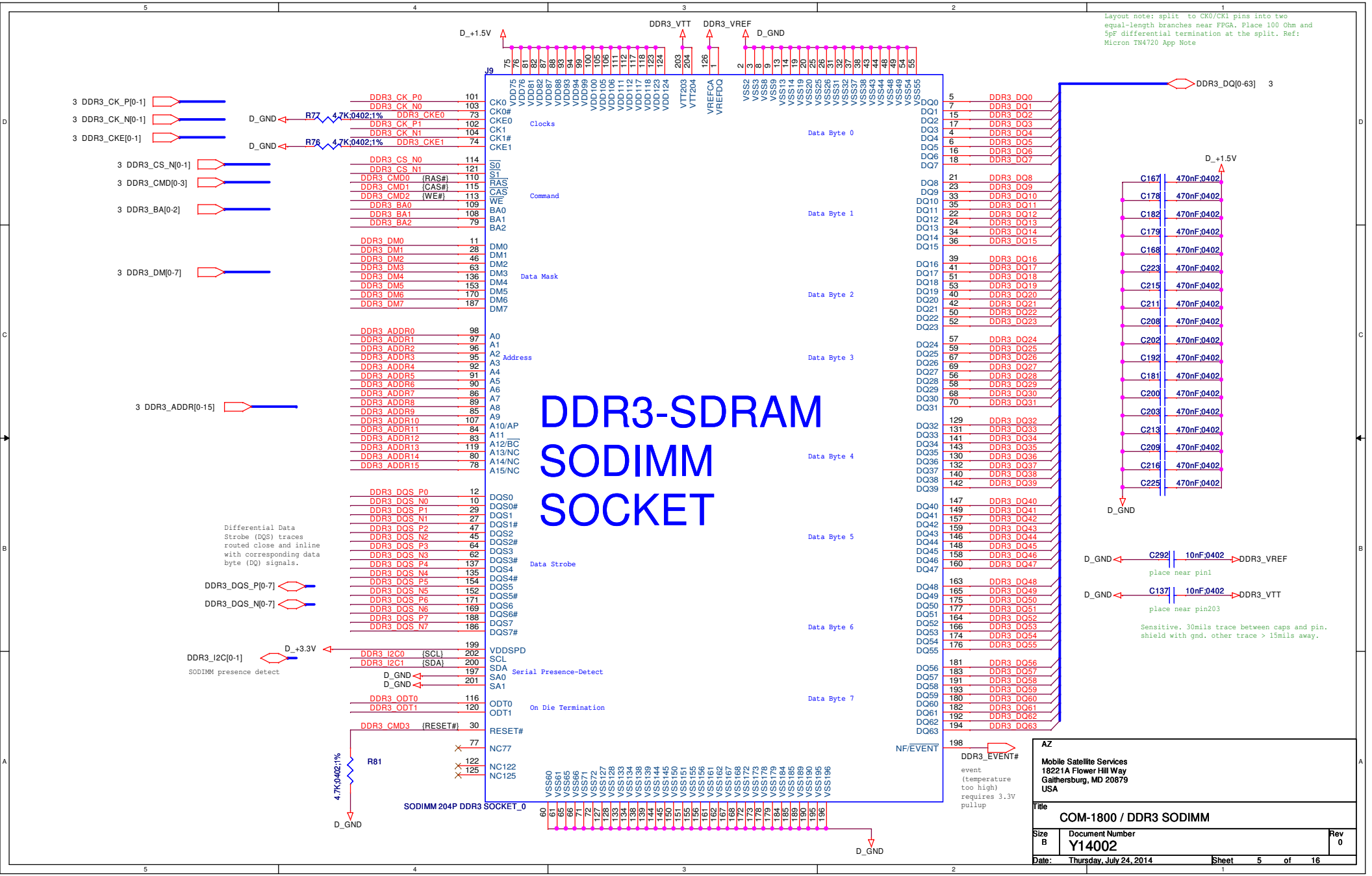

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Title: COM-1800 / DDR3 SODIMM

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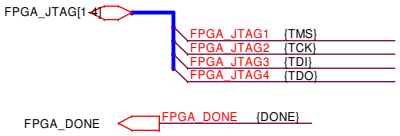
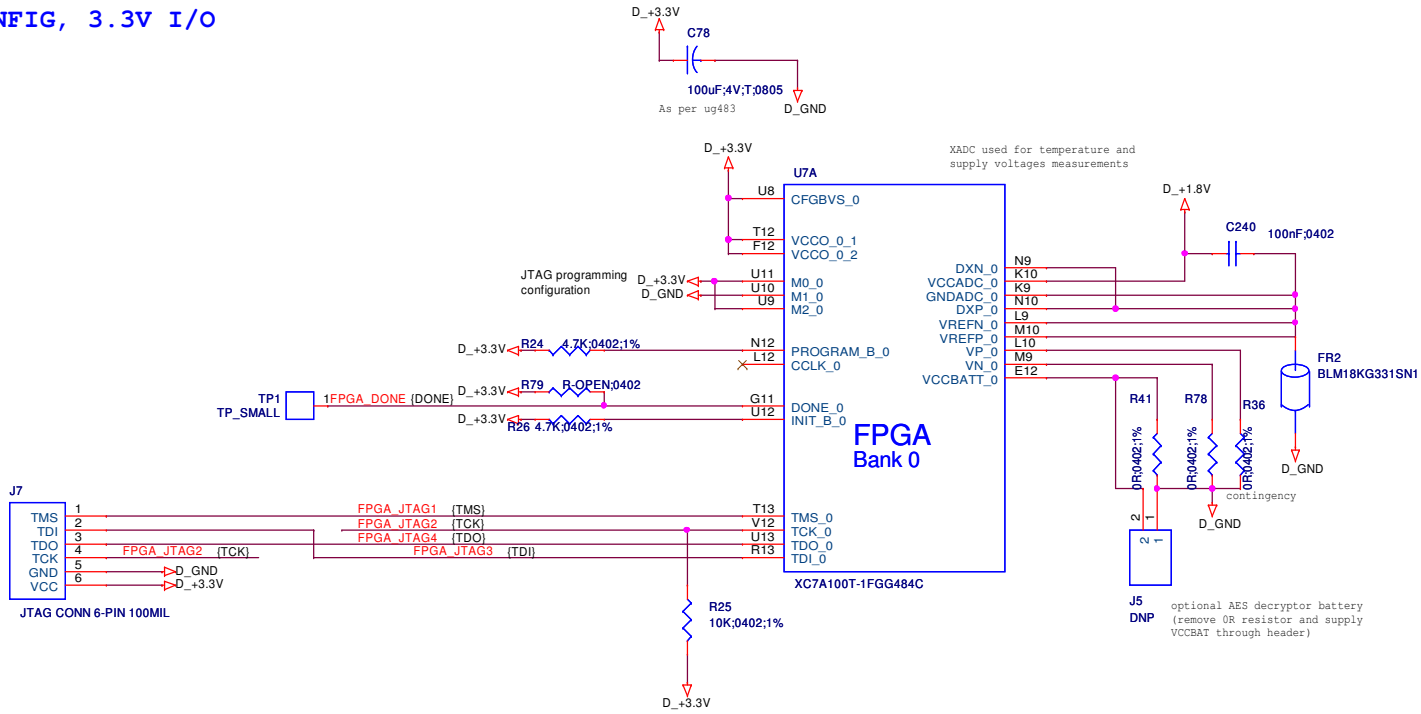
FPGA DEDICATED CONFIG, 3.3V I/O

ARM – FPGA communication programming





AZ		
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Title	COM-1800 / FPGA BANK0	
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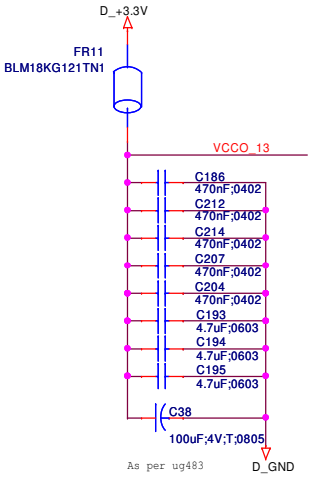
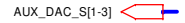
FPGA BANK 13, 3.3 I/O

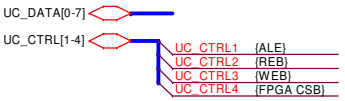


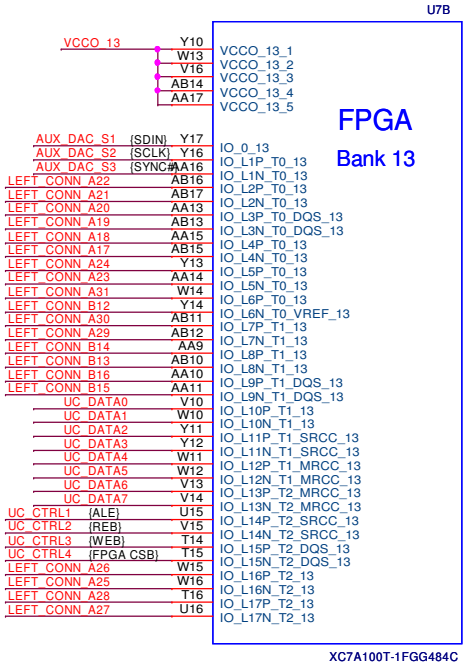
I/Os (LVCMOS33)

Auxiliary DAC



ARM - FPGA communication





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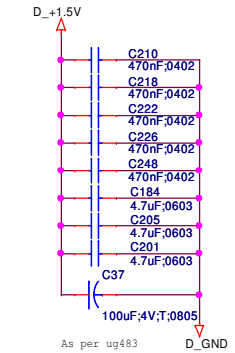
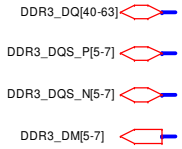
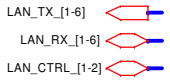
FPGA BANK 14, 1.5V I/O

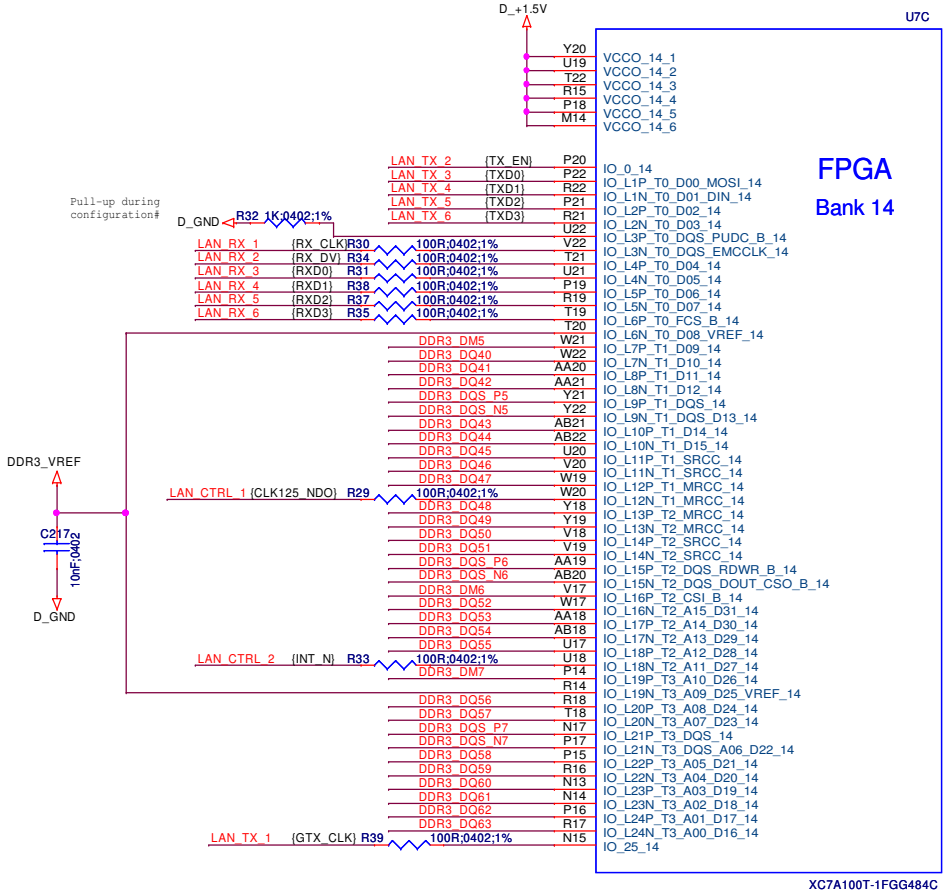


DDR3 SODIMM



Ethernet LAN PHY





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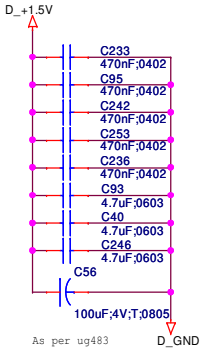
FPGA BANK 15, 1.5V I/O

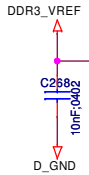


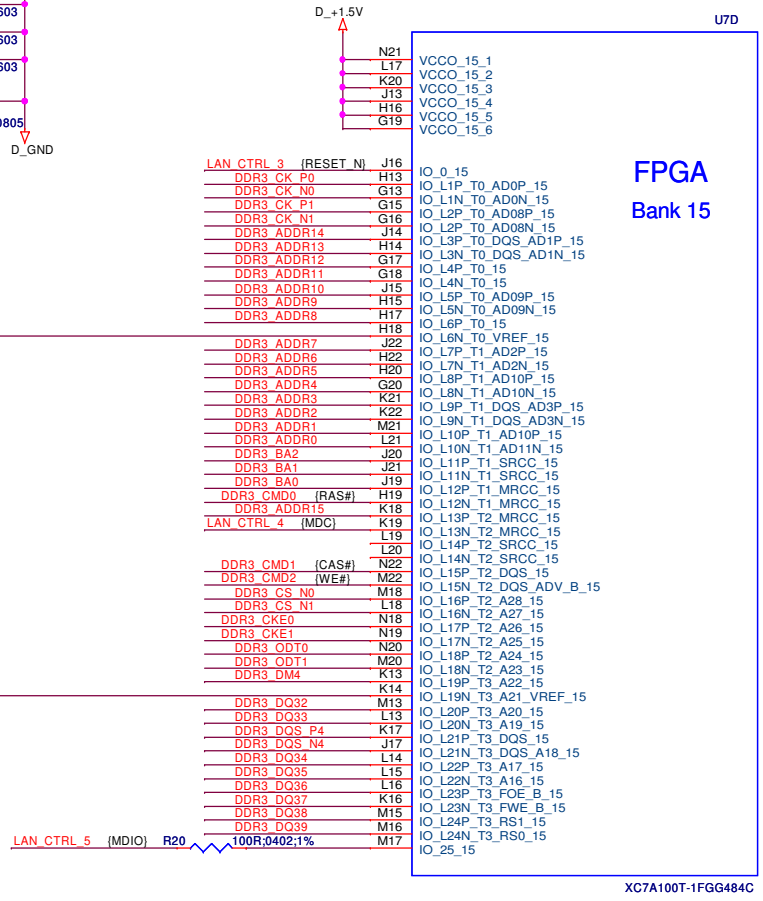
DDR3 SODIMM

DDR3_DQ[32-39]
DDR3_ADDR[0-15]
DDR3_BA[0-2]
DDR3_CMD[0-2]
DDR3_CKE[0-1]
DDR3_ODT[0-1]
DDR3_CS_N[0-1]
DDR3_DQS_P[4-4]
DDR3_DQS_N[4-4]
DDR3_DM[4-4]
DDR3_CK_P[0-1]
DDR3_CK_N[0-1]

Ethernet LAN PHY

LAN_CTRL_[3-5]





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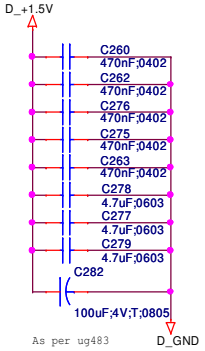
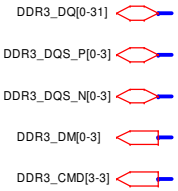
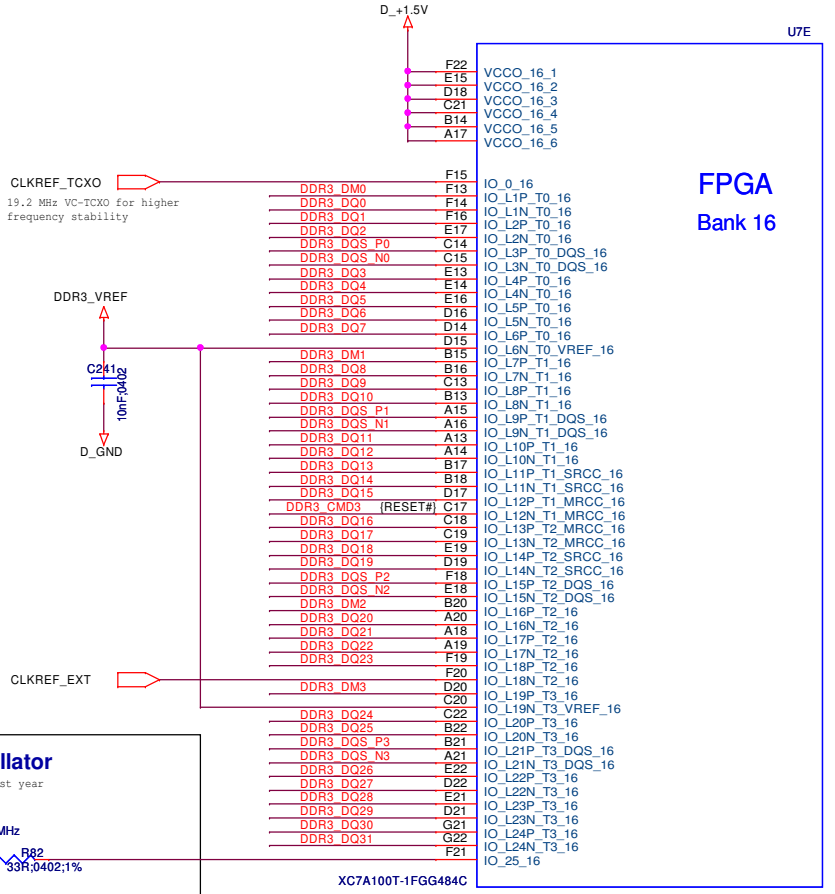
FPGA BANK 16, 1.5V I/O



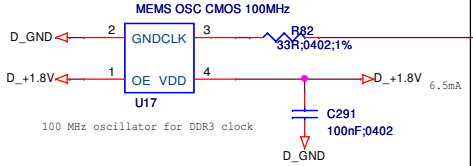
DDR3 SODIMM





MEMS (silicon-only) oscillator

high gs, 20ppm over -40/+85C, 5ppm aging 1st year
3.2x2.5mm footprint



100 MHz oscillator for DDR3 clock

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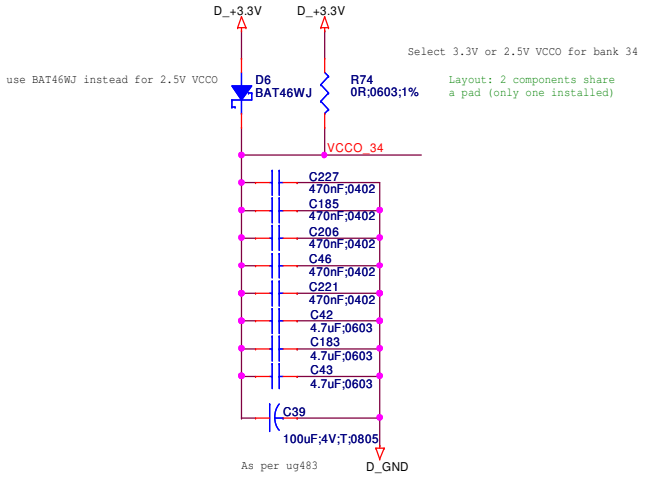
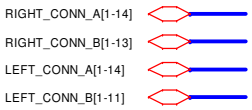
FPGA BANK 34, 2.5V or 3.3 I/O



I/Os (LVCMOS or LVDS)



U7F

VCCO_34		W3	VCCO_34_1
		V6	VCCO_34_2
		T2	VCCO_34_3
		R5	VCCO_34_4
		AB4	VCCO_34_5
		AA7	VCCO_34_6
LEFT_CONN_A13		T3	IO_0_34
RIGHT_CONN_A12	{RA6P}	T1	IO_L1P_T0_34
RIGHT_CONN_A11	{RA6N}	U1	IO_L1N_T0_34
RIGHT_CONN_A8	{RA4P}	U2	IO_L2P_T0_34
RIGHT_CONN_A7	{RA4N}	V2	IO_L2N_T0_34
RIGHT_CONN_B11	{RB5P}	R3	IO_L3P_T0_DQS_34
RIGHT_CONN_B10	{RB5N}	R2	IO_L3N_T0_DQS_34
RIGHT_CONN_B2	{RB1P}	W2	IO_L4P_T0_34
RIGHT_CONN_B1	{RB1N}	Y2	IO_L4N_T0_34
RIGHT_CONN_A2	{RA1P}	W1	IO_L5P_T0_34
RIGHT_CONN_A1	{RA1N}	Y1	IO_L5N_T0_34
RIGHT_CONN_B9	{RB4P}	U3	IO_L6P_T0_34
RIGHT_CONN_B8	{RB4N}	V3	IO_L6N_T0_VREF_34
LEFT_CONN_A2	{LA1P}	AA1	IO_L7P_T1_34
LEFT_CONN_A1	{LA1N}	AB1	IO_L7N_T1_34
LEFT_CONN_B2	{LB1P}	AB3	IO_L8P_T1_34
LEFT_CONN_B1	{LB1N}	AB2	IO_L8N_T1_34
LEFT_CONN_A4	{LA2P}	Y3	IO_L9P_T1_DQS_34
LEFT_CONN_A3	{LA2N}	AA3	IO_L9N_T1_DQS_34
LEFT_CONN_A6	{LA3P}	AA5	IO_L10P_T1_34
LEFT_CONN_A5	{LA3N}	AB5	IO_L10N_T1_34
LEFT_CONN_B4	{LB2P}	Y4	IO_L11P_T1_SRCC_34
LEFT_CONN_B3	{LB2N}	AA4	IO_L11N_T1_SRCC_34
RIGHT_CONN_A4	{RA2P}	V4	IO_L12P_T1_MRCC_34
RIGHT_CONN_A3	{RA2N}	W4	IO_L12N_T1_MRCC_34
RIGHT_CONN_A14	{RA7P}	R4	IO_L13P_T2_MRCC_34
RIGHT_CONN_A13	{RA7N}	T4	IO_L13N_T2_MRCC_34
RIGHT_CONN_A10	{RA5P}	T5	IO_L14P_T2_SRCC_34
RIGHT_CONN_A9	{RA5N}	U5	IO_L14N_T2_SRCC_34
LEFT_CONN_B9	{LB4P}	W6	IO_L15P_T2_DQS_34
LEFT_CONN_B8	{LB4N}	W5	IO_L15N_T2_DQS_34
RIGHT_CONN_B7	{RB3P}	U6	IO_L16P_T2_34
RIGHT_CONN_B6	{RB3N}	V5	IO_L16N_T2_34
RIGHT_CONN_B13	{RB6P}	R6	IO_L17P_T2_34
RIGHT_CONN_B12	{RB6N}	T6	IO_L17N_T2_34
LEFT_CONN_A8	{LA4P}	Y6	IO_L18P_T2_34
LEFT_CONN_A7	{LA4N}	AA6	IO_L18N_T2_34
RIGHT_CONN_B4	{RB2P}	V7	IO_L19P_T3_34
RIGHT_CONN_B3	{RB2N}	W7	IO_L19N_T3_VREF_34
LEFT_CONN_B7	{LB3P}	AB7	IO_L20P_T3_34
LEFT_CONN_B6	{LB3N}	AB6	IO_L20N_T3_34
RIGHT_CONN_A6	{RA3P}	V9	IO_L21P_T3_DQS_34
RIGHT_CONN_A5	{RA3N}	V8	IO_L21N_T3_DQS_34
LEFT_CONN_A10	{LA5P}	AA8	IO_L22P_T3_34
LEFT_CONN_A9	{LA5N}	AB8	IO_L22N_T3_34
LEFT_CONN_B11	{LB5P}	Y8	IO_L23P_T3_34
LEFT_CONN_B10	{LB5N}	Y7	IO_L23N_T3_34
LEFT_CONN_A12	{LA6P}	W9	IO_L24P_T3_34
LEFT_CONN_A11	{LA6N}	Y9	IO_L24N_T3_34
LEFT_CONN_A14		U7	IO_25_34

FPGA
Bank 34

XC7A100T-1FGG484C

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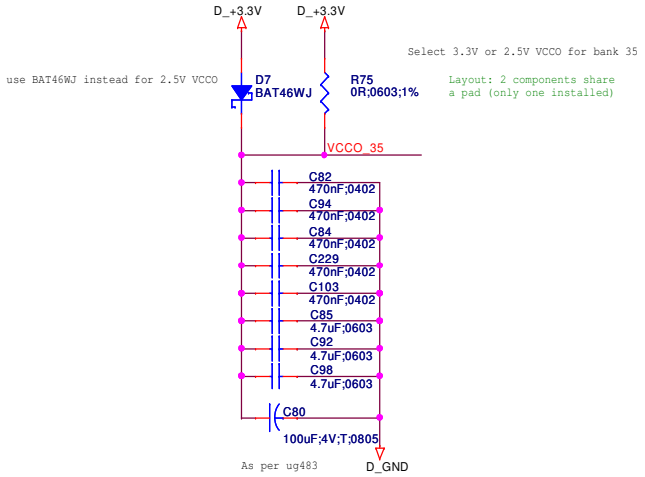
FPGA BANK 35, 2.5V or 3.3 I/O

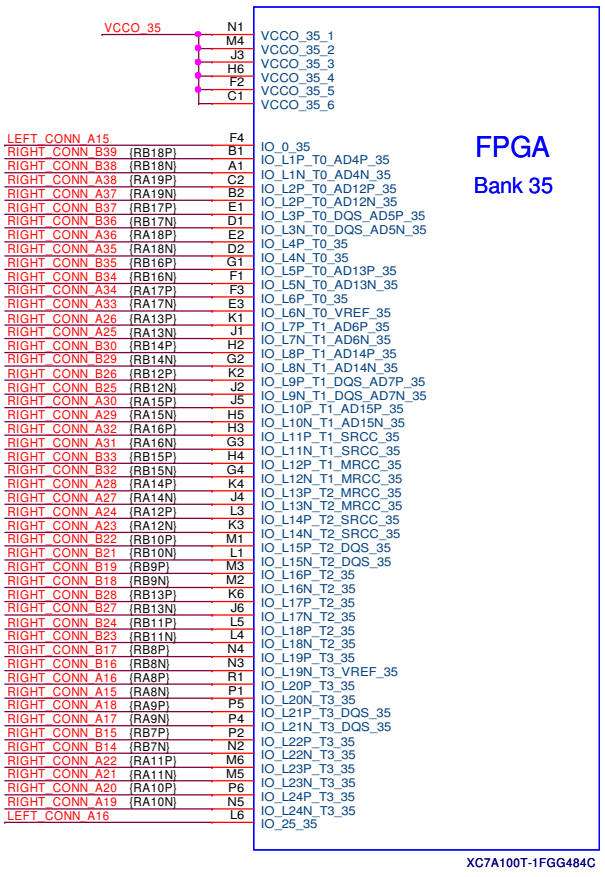


HIGH-SPEED LVCMOS or LVDS I/Os

RIGHT_CONN_A[15-38]

RIGHT_CONN_B[14-39]

LEFT_CONN_A[15-16]



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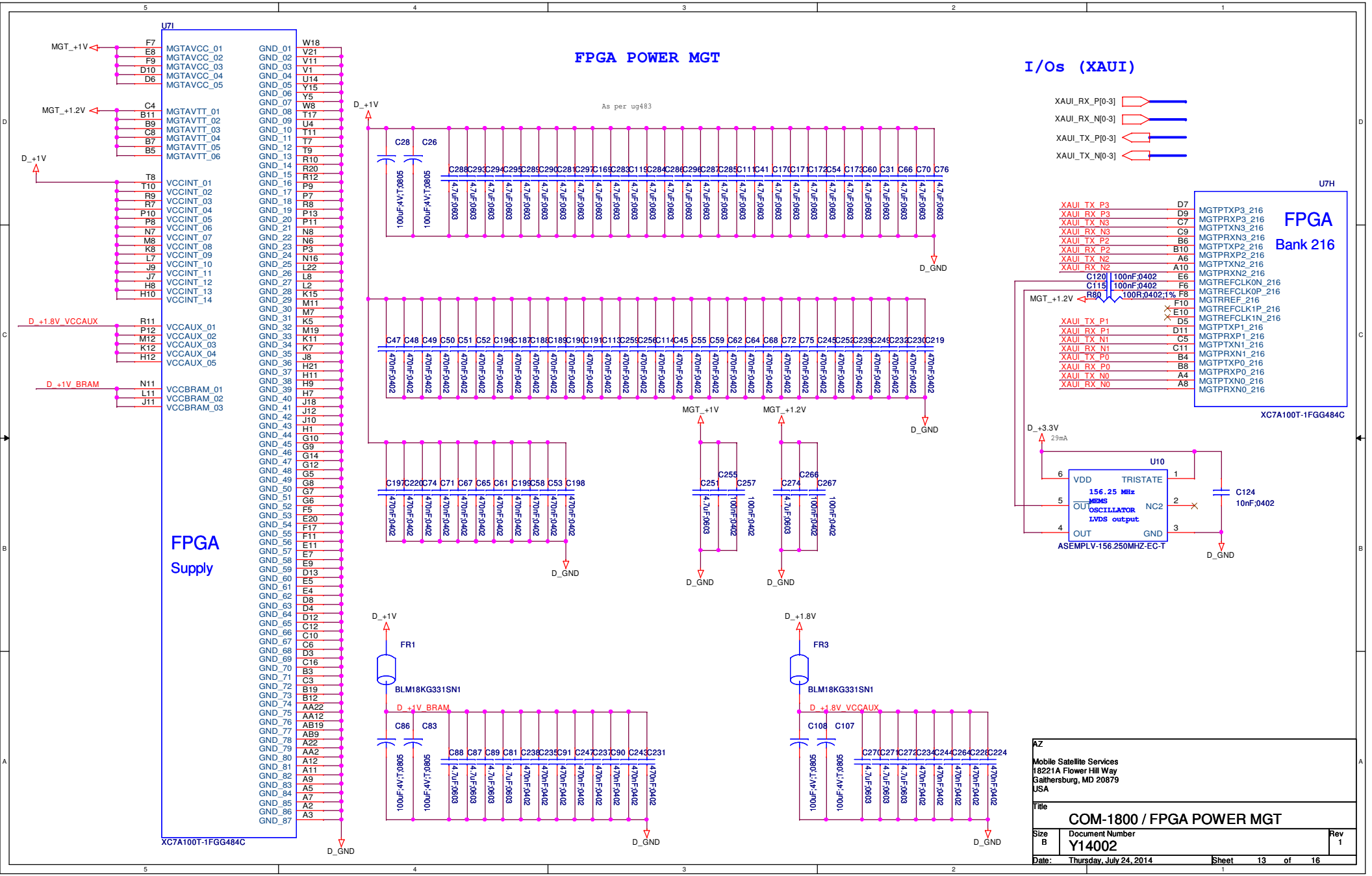
FPGA POWER MGT
I/Os (XAUI)
FPGA
Supply
FPGA
Bank 216
U7I
U7H
U10
XC7A100T-1FGG484C
ASEMPLV-156.250MHZ-EC-T
As per ug483
D_+1V
D_+1.8V_VCCAUX
D_+1V_BRAM
MGT_+1V
MGT_+1.2V
D_+3.3V
D_GND
FR1
FR3
BLM18KG331SN1
XAUI_RX_P[0-3]
XAUI_RX_N[0-3]
XAUI_TX_P[0-3]
XAUI_TX_N[0-3]
MGTAVCC_01
MGTAVCC_02
MGTAVCC_03
MGTAVCC_04
MGTAVCC_05
MGTAVTT_01
MGTAVTT_02
MGTAVTT_03
MGTAVTT_04
MGTAVTT_05
MGTAVTT_06
VCCINT_01
VCCINT_02
VCCINT_03
VCCINT_04
VCCINT_05
VCCINT_06
VCCINT_07
VCCINT_08
VCCINT_09
VCCINT_10
VCCINT_11
VCCINT_12
VCCINT_13
VCCINT_14
VCCAUX_01
VCCAUX_02
VCCAUX_03
VCCAUX_04
VCCAUX_05
VCCBRAM_01
VCCBRAM_02
VCCBRAM_03
GND_01
GND_02
GND_03
GND_04
GND_05
GND_06
GND_07
GND_08
GND_09
GND_10
GND_11
GND_12
GND_13
GND_14
GND_15
GND_16
GND_17
GND_18
GND_19
GND_20
GND_21
GND_22
GND_23
GND_24
GND_25
GND_26
GND_27
GND_28
GND_29
GND_30
GND_31
GND_32
GND_33
GND_34
GND_35
GND_36
GND_37
GND_38
GND_39
GND_40
GND_41
GND_42
GND_43
GND_44
GND_45
GND_46
GND_47
GND_48
GND_49
GND_50
GND_51
GND_52
GND_53
GND_54
GND_55
GND_56
GND_57
GND_58
GND_59
GND_60
GND_61
GND_62
GND_63
GND_64
GND_65
GND_66
GND_67
GND_68
GND_69
GND_70
GND_71
GND_72
GND_73
GND_74
GND_75
GND_76
GND_77
GND_78
GND_79
GND_80
GND_81
GND_82
GND_83
GND_84
GND_85
GND_86
GND_87
MGTPTXP3_216
MGTPRXP3_216
MGTPTXN3_216
MGTPRXN3_216
MGTPTXP2_216
MGTPRXP2_216
MGTPTXN2_216
MGTPRXN2_216
MGTREFCLK0N_216
MGTREFCLK0P_216
MGTRREF_216
MGTREFCLK1P_216
MGTREFCLK1N_216
MGTPTXP1_216
MGTPRXP1_216
MGTPTXN1_216
MGTPRXN1_216
MGTPTXP0_216
MGTPRXP0_216
MGTPTXN0_216
MGTPRXN0_216
XC7A100T-1FGG484C
C124
10nF;0402
C120
100nF;0402
C115
100nF;0402
R80
100R;0402;1%
156.25 MHz
MEMS
OSCILLATOR
LVDS output
VDD
TRISTATE
OUT
NC2
OUT
GND
29mA
AZ
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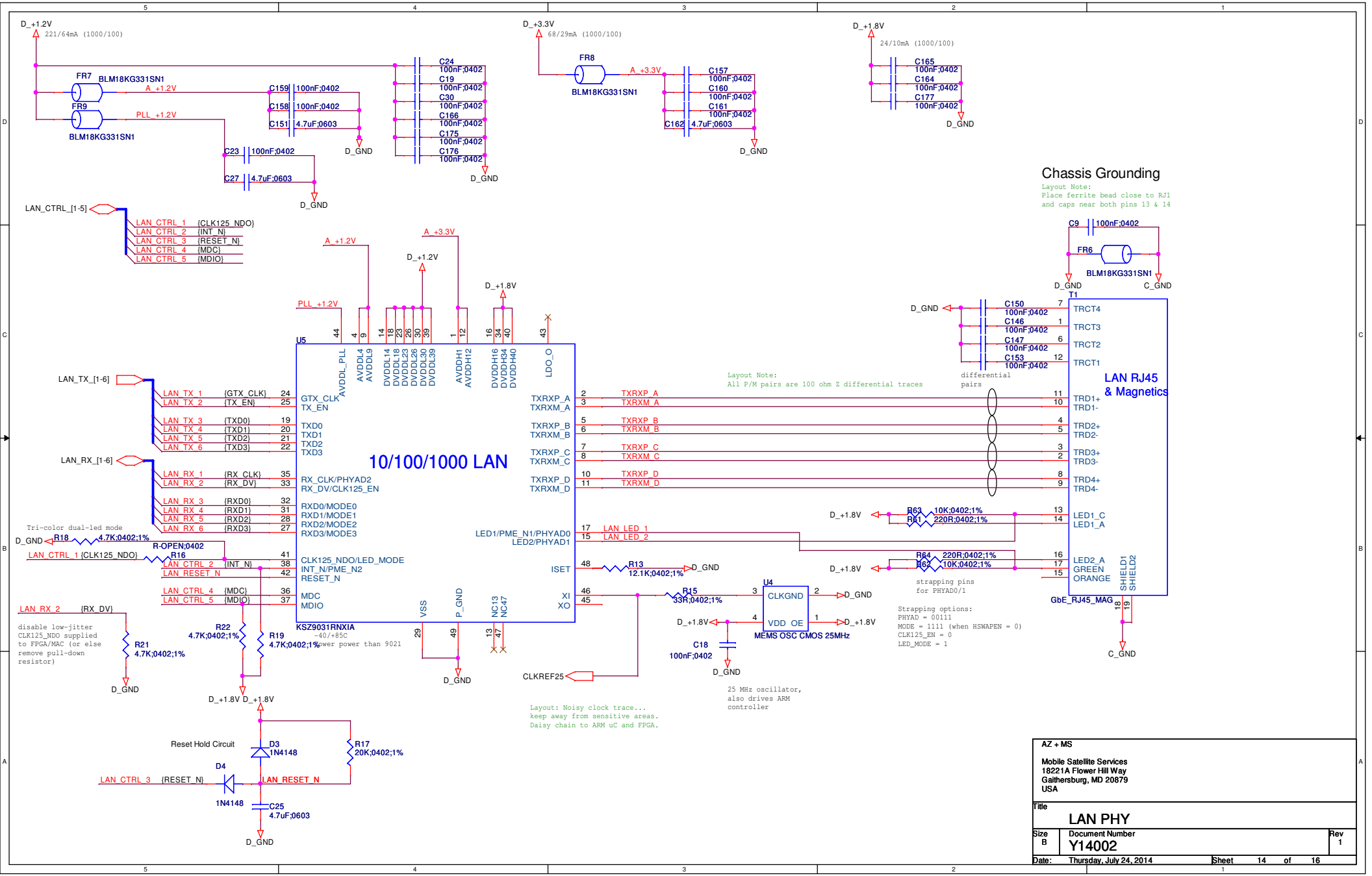
D_+1.2V
221/64mA (1000/100)
FR7
BLM18KG331SN1
A_+1.2V
FR9
BLM18KG331SN1
PLL_+1.2V
C159 100nF;0402
C158 100nF;0402
C151 4.7uF;0603
C23 100nF;0402
C27 4.7uF;0603
D_GND
C24 100nF;0402
C19 100nF;0402
C30 100nF;0402
C166 100nF;0402
C175 100nF;0402
C176 100nF;0402
D_+3.3V
68/29mA (1000/100)
FR8
BLM18KG331SN1
A_+3.3V
C157 100nF;0402
C160 100nF;0402
C161 100nF;0402
C162 4.7uF;0603
D_+1.8V
24/10mA (1000/100)
C165 100nF;0402
C164 100nF;0402
C177 100nF;0402
Chassis Grounding
Layout Note:
Place ferrite bead close to RJ1
and caps near both pins 13 & 14
C9 100nF;0402
FR6
BLM18KG331SN1
C_GND
T1
LAN RJ45
& Magnetics
GbE_RJ45_MAG
C150 100nF;0402
C146 100nF;0402
C147 100nF;0402
C153 100nF;0402
TRCT4
TRCT3
TRCT2
TRCT1
TRD1+
TRD1-
TRD2+
TRD2-
TRD3+
TRD3-
TRD4+
TRD4-
differential
pairs
LAN_CTRL_[1-5]
LAN_CTRL_1 {CLK125_NDO}
LAN_CTRL_2 {INT_N}
LAN_CTRL_3 {RESET_N}
LAN_CTRL_4 {MDC}
LAN_CTRL_5 {MDIO}
U5
10/100/1000 LAN
KSZ9031RNXIA
-40/+85C
Lower power than 9021
AVDDL_PLL
AVDDL4
AVDDL9
DVDDL14
DVDDL18
DVDDL23
DVDDL26
DVDDL30
DVDDL39
AVDDH1
AVDDH12
DVDDH16
DVDDH34
DVDDH40
LDO_O
LAN_TX_[1-6]
LAN_TX_1 {GTX_CLK}
LAN_TX_2 {TX_EN}
LAN_TX_3 {TXD0}
LAN_TX_4 {TXD1}
LAN_TX_5 {TXD2}
LAN_TX_6 {TXD3}
GTX_CLK
TX_EN
TXD0
TXD1
TXD2
TXD3
LAN_RX_[1-6]
LAN_RX_1 {RX_CLK}
LAN_RX_2 {RX_DV}
LAN_RX_3 {RXD0}
LAN_RX_4 {RXD1}
LAN_RX_5 {RXD2}
LAN_RX_6 {RXD3}
RX_CLK/PHYAD2
RX_DV/CLK125_EN
RXD0/MODE0
RXD1/MODE1
RXD2/MODE2
RXD3/MODE3
Tri-color dual-led mode
R18 4.7K;0402;1%
R-OPEN;0402
R16
LAN_CTRL_1 {CLK125_NDO}
LAN_CTRL_2 {INT_N}
LAN_RESET_N
CLK125_NDO/LED_MODE
INT_N/PME_N2
RESET_N
LAN_CTRL_4 {MDC}
LAN_CTRL_5 {MDIO}
MDC
MDIO
LAN_RX_2 {RX_DV}
disable low-jitter
CLK125_NDO supplied
to FPGA/MAC (or else
remove pull-down
resistor)
R21 4.7K;0402;1%
R22 4.7K;0402;1%
R19 4.7K;0402;1%
D_GND
D_+1.8V
VSS
P_GND
NC13
NC47
TXRXP_A
TXRXM_A
TXRXP_B
TXRXM_B
TXRXP_C
TXRXM_C
TXRXP_D
TXRXM_D
Layout Note:
All P/M pairs are 100 ohm Z differential traces
LED1/PME_N1/PHYAD0
LED2/PHYAD1
LAN_LED_1
LAN_LED_2
R63 10K;0402;1%
R61 220R;0402;1%
R64 220R;0402;1%
R62 10K;0402;1%
LED1_C
LED1_A
LED2_A
GREEN
ORANGE
SHIELD1
SHIELD2
strapping pins
for PHYAD0/1
Strapping options:
PHYAD = 00111
MODE = 1111 (when HSWAPEN = 0)
CLK125_EN = 0
LED_MODE = 1
ISET
R13 12.1K;0402;1%
XI
XO
CLKREF25
R15 33R;0402;1%
U4
CLKGND
VDD OE
MEMS OSC CMOS 25MHz
C18 100nF;0402
25 MHz oscillator,
also drives ARM
controller
Layout: Noisy clock trace...
keep away from sensitive areas.
Daisy chain to ARM uC and FPGA.
Reset Hold Circuit
D3 1N4148
D4 1N4148
R17 20K;0402;1%
LAN_CTRL_3 {RESET_N}
LAN_RESET_N
C25 4.7uF;0603
AZ + MS
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+5V DC Supply

OPERATIONAL RANGE: 4.9 - 12V
No damage: 13.2V max

Filter

J2
BATT+ 1
BATT- 2
P02ECH381RH-E
low-profile 3.81mm terminal block

FR5
BLM18KG121TN1

D_GND

Reverse Voltage Protection

Q2
D5 D6 S 4
2 D2
1 D1
G 3
FDC658AP
-30V, -3.4A, 75mOhm

D_GND

Transient Voltage Suppression

Vin_prot

D2
12V TVS
C
A

D_GND

PCB Mounting Holes

H3 H4 H2 H1
D_GND D_GND D_GND D_GND

1V 3A

Vin_prot

U6
NCP3170A 3A DC/DC Converter
PG 7
VIN 2
EN 6
COMP 5
VSW 8
FB 4
PGND 1
AGND 3
VREF=0.8V
NCP3170ADR2G

PGOOD1 {+1V}

C79 22uF;16V;T;1210
C44 15nF;0402
R23 1K;0402;1%

L3 3.3uH;4A
R28 24.9K;0402;1%
C57 150pF;0402
R27 100K;0402;1%

Ityp = TBDmA Vout = 1V

C63 C34 C32 C33 C69 C73 C77 100uF;4V;T;0805
C35 4.7uF;0603
C36 470nF;0402

D_+1V
FR12 BLM18KG121TN1
MGT_+1V

D_GND

FPGA VCCINT 328mA quiescent
FPGA VCCBRAM 11mA quiescent

1.2V 3A

U14
NCP3170A 3A DC/DC Converter
PG 7
VIN 2
EN 6
COMP 5
VSW 8
FB 4
PGND 1
AGND 3
VREF=0.8V
NCP3170ADR2G

PGOOD2 {+1.2V}

C14 22uF;16V;T;1210
C148 10nF;0402
R71 1K;0402;1%

L2 3.3uH;4A
R72 24.9K;0402;1%
C154 150pF;0402
R67 49.9K;0402;1%

Ityp = TBDmA Vout = 1.2V

C29 100uF;4V;T;0805
C155 4.7uF;0603
C156 470nF;0402

D_+1.2V
FR13 BLM18KG121TN1
MGT_+1.2V

D_GND

LAN 221mA

1.5V 3A

U13
NCP3170A 3A DC/DC Converter
PG 7
VIN 2
EN 6
COMP 5
VSW 8
FB 4
PGND 1
AGND 3
VREF=0.8V
NCP3170ADR2G

PGOOD3 {+1.5V}

C132 22uF;16V;T;1210
C131 10nF;0402
R60 1K;0402;1%

L5 3.3uH;4A
R54 24.9K;0402;1%
C122 150pF;0402
R44 28.7K;0402;1%

Ityp = TBDmA Vout = 1.49V

C127 100uF;4V;T;0805
C126 4.7uF;0603
C130 470nF;0402

D_+1.5V
D_GND

PGOOD[1-3]

Power Good Indicators
Must be pulled up by ARM processor

PGOOD1 {+1V}
PGOOD2 {+1.2V}
PGOOD3 {+1.5V}

AZ
Mobile Satellite Services
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Gaithersburg, MD 20879
USA

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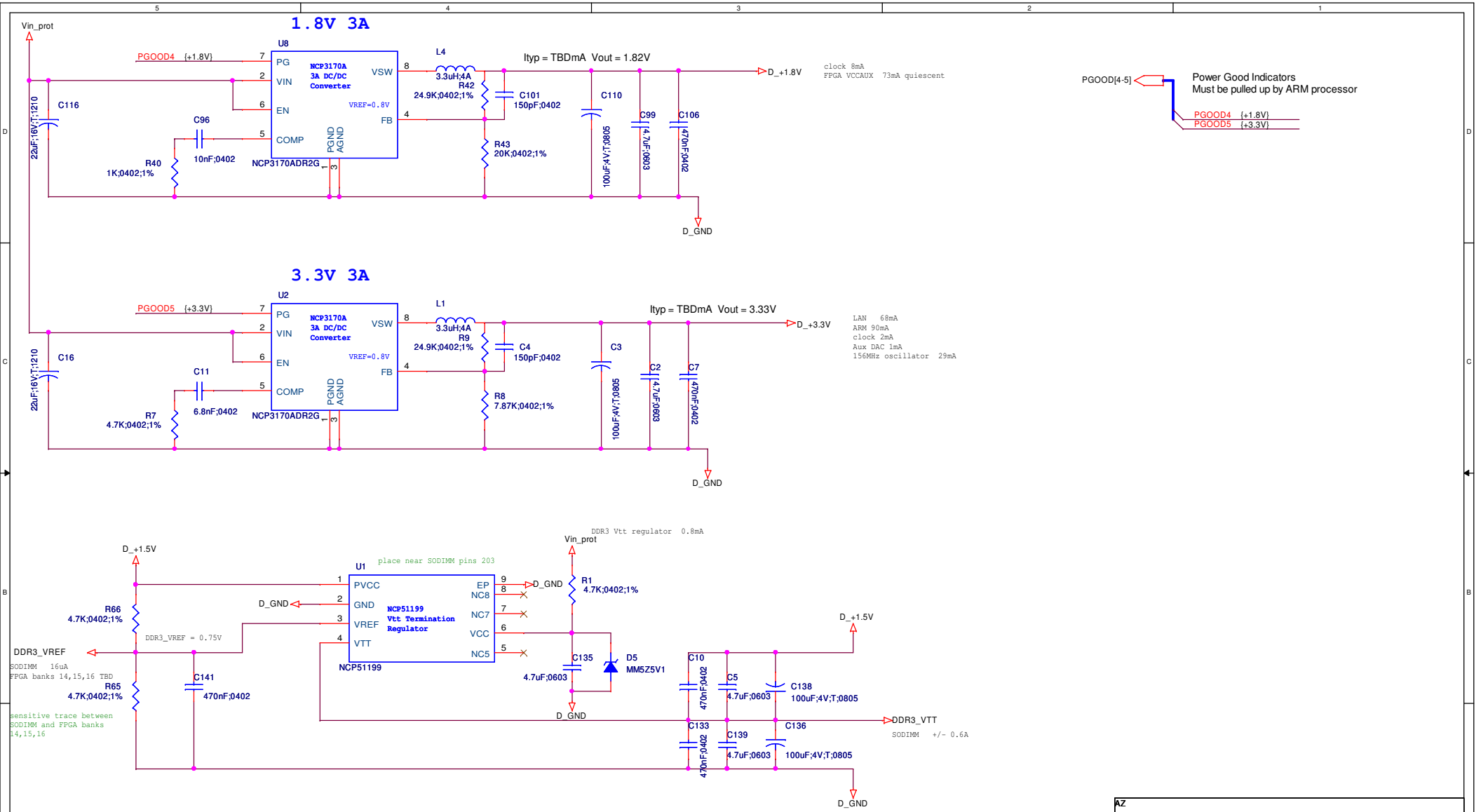

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Size	Document Number	Rev
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