COM-5401SOFT
Tri-Mode 10/100/1000 Ethernet MAC
VHDL SOURCE CODE OVERVIEW

Overview

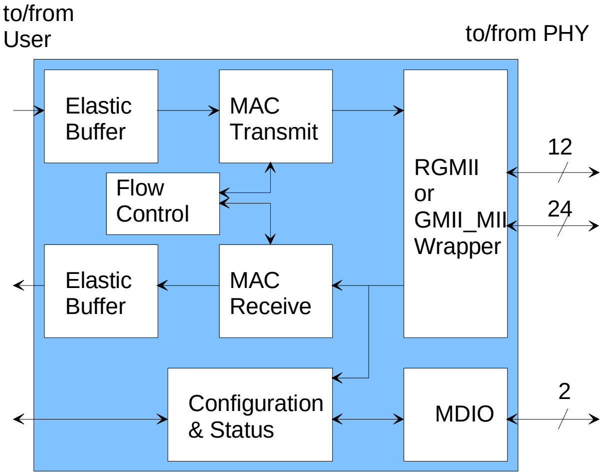
The COM-5401SOFT is a generic tri-mode Ethernet MAC core (including the **VHDL source code**) designed to support full- or half-duplex Gigabit throughput on low-cost FPGAs.

The component's very efficient implementation makes it suitable for multiple instantiations within a small FPGA. For example, it is instantiated four times (for a 4 Gbits/s combined throughput) in a small Spartan-6 XC6SLX16 [4][5].

Key features include:

- Compliance with the IEEE 802.3-2008 specification.
- Configurable half-duplex/full-duplex operation.
- Address filter to reject undesirable received packets.
- Automatic
    - Preamble generation and removal
    - 32-bit CRC generation and checking.
    - Packet retransmission in case of collision (when half-duplex).
    - Payload padding and pad removal for very short frames.

Block Diagram



Target Hardware

The code is written in generic VHDL so that it can be ported to a variety of FPGAs. The code was developed and tested on a Xilinx Spartan-6 XC6SLX16 FPGA.

It can be easily ported to any Xilinx Kintex7, Virtex-6, Virtex-5, Spartan-6 FPGAs and other FPGAs capable of running at 125 MHz.

Please note that the target FPGA must be capable of creating a 2ns delay on the RGMII transmit and receive clocks.

Keywords

Tri-mode, Ethernet MAC, 10/100/1000, MAC core, RGMII, GMII, VHDL, FPGA, GbE, Micrel KSZ9021, Ethernet PHY, Ethernet transceiver.

Device Utilization Summary

Device: Xilinx Spartan-6 –2 speed

	RGMII	GMII/MII
Slice Registers	726	738
LUTs	1023	1077
Block RAM/FIFO	3	3
DSP48A1s	0	0
GCLKs	2	3
DCMs/PLLs	0	0

Maximum user clk frequency: 153 MHz

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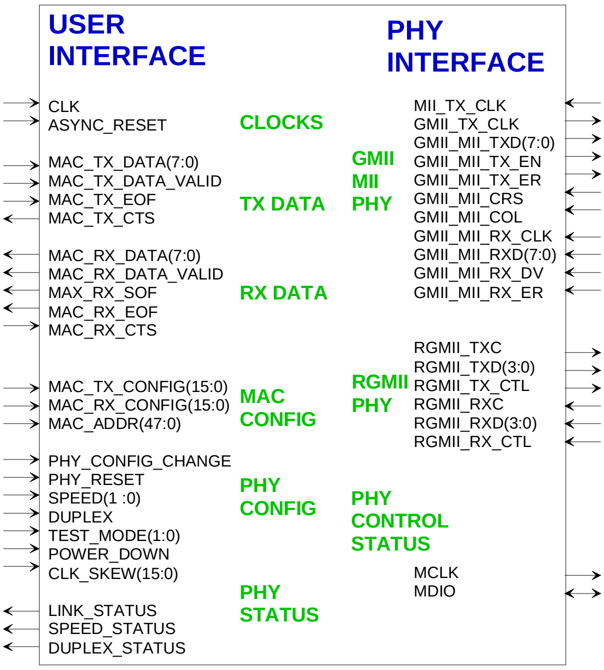
Device: Xilinx Kintex7 –3 speed

	RGMII	GMII/MII
Slice Registers	714	731
LUTs	1003	1000
Block RAM/FIFO	2	2
DSP48A1s	0	0
GCLKs	2	3
DCMs/PLLs	0	0

Maximum user clk frequency: 315 MHz

Interfaces



User Interface

This interface comprises three primary signal groups: transmit data, receive data and monitoring & control. All signals are clock synchronous with a user-selected clock CLK (it does not have to be the same as the 125/25/2.5 MHz PHY clocks).

For maximum throughput, 16Kb elastic buffers are included in both tx/rx directions at the user interface. This allows the MAC engine to multi-task, sending a complete packet to the PHY while accepting subsequent packet data from the user.

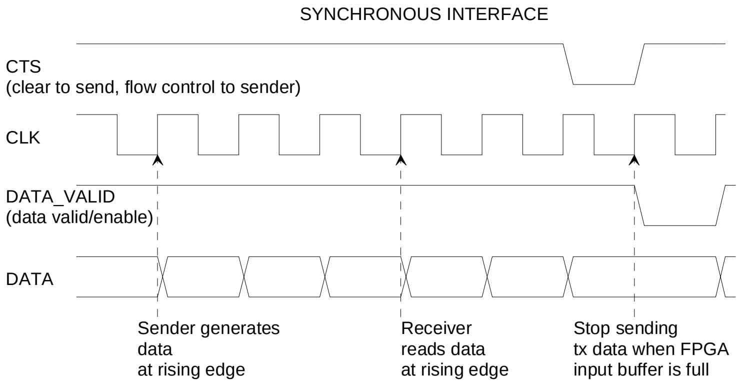
When space is available in the tx elastic buffer, the user can send an Ethernet frame as illustrated below:

Destination Address	6Bytes
Source Address	6Bytes
Length / Type	2Bytes
MAC Client Data	46-1500Bytes (pad is added to reach minimum size)
Pad	
Frame Check Sequence (CRC)	4Bytes

The software inserts the pad and frame check sequence (CRC) fields automatically unless disabled by the user.

The software then encapsulates the tx frame into an Ethernet Packet by adding a preamble, start of frame delimiter and extension as needed.

User Interface timing



PHY Interface

The COM-5401SOFT interfaces with an external 10/100/1000 Ethernet PHY through one of several standard Media Independent Interfaces. The interface type is user-selected with the MII_SEL generic signal prior to VHDL synthesis.

MII_SEL = ‘0’

- RGMII for 10/100/1000 Mbps

MII_SEL = ‘1’

- MII for 10/100 Mbps as per 802.3 clause 22
- GMII for 1000 Mbps as per 802.3 clause 35

In parallel, the external PHY is managed via a two-wire standard MDIO interface.

The GMII/MII interface is fairly generic. It should work with most PHYs with only very minor code changes. In particular, the delay between clock and data may need to be adjusted for the target hardware through the constants RXC_DELAY and TXC_DELAY in the *GMII_MII_WRAPPER.vhd* component, in order to avoid glitches.

The RGMII interface is written for the Micrel KSZ9021 PHY. Changes in the extended control registers to adjust the clock skew are expected when using a PHY from another vendor (see *PHY_CONFIG.vhd*).

Additional PHY-specific configuration options are also defined at the time of power-up/reset. See the "Strapping options" section.

Configuration

Pre-synthesis configuration parameters

The following configuration parameters are set prior to synthesis in the generic section of the *COM5401.vhd* component declaration.

Generic	*Description*
MII interface type	MII_SEL. Select the MII interface type: 0 = RGMII 1 = GMII/MII
PHY IC address	5-bit PHY IC address PHY_ADDR
User clock frequency	The user-supplied CLK serves as time reference for internal timers/delays. Declare the frequency in MHz (120 for 120 MHz, etc) CLK_FREQUENCY

Run-time configuration parameters

The user can set and modify the following controls at run-time. All controls are synchronous with the user-supplied global CLK.

MAC transmit configuration	*Description*
Auto-padding	1 = Automatic padding of short frames. Requires that auto-CRC insertion be enabled too. 0 = Skip padding. User is responsible for adding padding to meet the minimum 60 byte frame size.
	MAC_TX_ CONFIG (0)
Auto-CRC	1 = Automatic appending of 32-bit CRC at the end of the frame 0 = Skip CRC insertion. User is responsible for including the frame check sequence. MAC_TX_CONFIG(1)
MAC receive configuration	*Description*
MAC address	This network node 48-bit MAC address. The receiver checks incoming packets for a match between the destination address field and this MAC address. The user is responsible for selecting a unique 'hardware' address for each instantiation. Natural bit order: enter x0123456789ab for the MAC address 01:23:45:67:89:ab
Promiscuous mode	1 = all valid frames are accepted, regardless of their destination address. 0 = destination addresses are checked. MAC_RX_CONFIG(0)
Allow rx broadcast packets	0 = filter out packets with the broadcast destination address FF:FF:FF:FF:FF:FF. 1 = accepts broadcast packets. MAC_RX_CONFIG(1)
Allow rx multi-cast packets	0 = filter out packets with the multicast bit set in the destination address. 1 = accepts multicast packets. MAC_RX_CONFIG(2)
Filter out padding and CRC fields	1 = filter out the pad and CRC fields. 0 = pass along the entire Ethernet frame including pad and CRC fields. MAC_RX_CONFIG(1)
PHY configuration	*Description*
Speed	Select autonegotiation or force the PHY to operate at a specific speed. 00 = force 10 Mbps 01 = force 100 Mbps 10 = force 1000 Mbps 11 = auto-negotiation (default)
Half/Full duplex	Half-duplex is a safe configuration which can be used

	with older networking equipment. Full duplex results in higher throughput but may be incompatible with unswitched hubs. 0 = half-duplex 1 = full duplex.
PHY test mode	00 = normal mode (default) 01 = loopback mode (at the phy) 10 = remote loopback 11 = led test mode
PHY reset	1 = PHY software reset, 0 = no reset
PHY power down	1 = power down enabled 0 = disabled

To enact any PHY configuration, a pulse must be sent to PHY_CONFIG_CHANGE.

MAC Receive Packets Check

The MAC receive section performs the following checks on the incoming packets:

- frame size >= 64 bytes
- frame size <= 1518 bytes
- frame length field is consistent with actual received frame size
- destination address matches the user-specified MAC address, or
- destination address is a broadcast or multicast address
- Frame check sequence (CRC) is verified.

When an incoming packet passes all above checks, it is forwarded to the user via a 16Kb rx elastic buffer.

Exclusions

This software does not support the following 802.3-2008 options:

- Packet bursting (half duplex mode 1000Mbps only) Section 4.2.3.2.7

Software Licensing

The COM-5401SOFT is supplied under the following key licensing terms:

1. A nonexclusive, nontransferable license to use the VHDL source code internally, and
2. An unlimited, royalty-free, nonexclusive transferable license to make and use products incorporating the licensed materials, solely in bitstream format, on a worldwide basis.

The complete VHDL/IP Software License Agreement can be downloaded from
http://www.comblock.com/download/softwarelicense.pdf

Reference documents

[1] IEEE Std. 802.3™-2008
Relevant clauses:

- Clause 3: MAC frame and packet specifications
- Clause 4: Media Access Control
- Clause 22: Reconcilliation Sublayer and Media Independent Interface (MII)
- Clause 35: Reconcilliation Sublayer and Gigabit Media Independent Interface (GMII)

[2] Reduced Gigabit Media Independent Interface (RGMII) 4/1/2002 Version 2.0

[3] Micrel KSZ9021 specifications, "Gigabit Ethernet Transceiver with RGMII Support", 10/2009

[4] ComBlock COM-1600 FPGA + ARM + USB2.0+ DDR2 + NAND development platform
www.comblock.com/com1600.html

[5] ComBlock COM-5401 4-Port 10/100/1000 Mbps Ethernet Transceivers
www.comblock.com/com5401.html

[6] COM-1600 development platform schematics

Configuration Management

The current software revision is 8.

Directory	Contents
/	Project files for various Xilinx ISE versions.
/doc	Specifications, user manual, implementation documents
/src	.vhd source code, .ucf constraint files, .pkg packages. One component per file.
/sim	Test benches
/bin	.ngc, .bit, .mcs configuration files
/use_example	use example, .ngc for Spartan-6 and instantiation template

VHDL development environment

The VHDL software was developed using the following development environment:

(a) Xilinx ISE 14.1 with XST as VHDL synthesis tool

(b) Xilinx ISE Isim as VHDL simulation tool

Ready-to-use Hardware

The binary component (.ngc) is freely available for use on the following Comblock hardware modules:

- COM-1600 FPGA + ARM + DDR2 + NAND + USB2 development platform
- COM-5401 4-Port 10/100/1000 Mbps Ethernet Transceivers

See the following code templates:
comblock.com/download.html#COM1600template

All hardware schematics are available in this CD.

Xilinx-specific code

The VHDL source code is written in generic VHDL with few Xilinx primitives. No Xilinx CORE is used. The Xilinx primitives are:

- IBUF
- IBUFG
- BUFG (global clocks)
- IDDR2 (RGMII DDR input)
- ODDR2 (RGMII DDR output)
- IODELAY2 to delay the RGMII clocks
- RAM block: RAMB16_S9_S9

XST synthesis

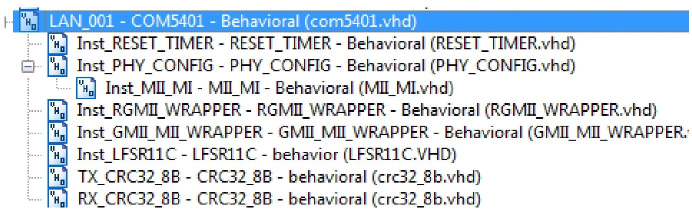
The *com5401.vhd* MAC can be synthesized as a black box to be included in large projects. To generate this "black box" .ngc file, the Xilinx ISE XST synthesis properties must first be configured as follows:

- Xilinx Specific Options
  - Add I/O buffers: disabled
  - Pack I/O registers in IOBs: No

The synthesis process then generates a .ngc output file.

When synthesizing the final project, XST synthesis should be configured with "Pack I/O registers in IOBs: yes" as it results in better timing.

Top-Level VHDL hierarchy



The code is stored with one, and only one, component per file.

The root entity (highlighted above) is *COM5401.vhd*. It comprises the tx and rx elastic buffers, tx state machine and tx packet construction.

The root also includes the following components:

- The *PHY_CONFIG.vhd* component to configure the PHY.

- The *RGMII_WRAPPER.vhd* converts the natural PHY interface to the lower pin-count RGMII.
- The *GMII_MII_WRAPPER.vhd* converts the natural PHY interface to the standard GMII (1000 Mbps) or MII (10/100 Mbps) interface.
- The *CRC32_8B.vhd*, instantiated twice, computes the CRC32 to be appended to tx packets and to check rx. The CRC32 computation is performed 8 data bits at a time.

Clock / Timing

The software uses the following main clocks:

- A 125/25/2.5 MHz receive clock generated by the PHY. The speed depends on the recovered LAN signal. In the RGMII and GMII cases, the receive clock is looped back and used as transmit clock.
- In the MII case, the transmit clock is supplied by the PHY.
- A user-supplied interface clock (CLK) to read and write packets from/to the MAC. CLK frequency is independent of the PHY clock but should be high enough to support the expected data throughput.

Quick Start

This section describes a few tips to quickly establish a working, albeit simple, baseline.

Quick start using ComBlock modules

The purpose is to load the ready-to-use FPGA configuration for Ethernet MAC with RGMII interface into off-the-shelf hardware consisting of a COM-1600 FPGA development platform and a COM-5102 or 5401 plug-in Ethernet adapter.

FPGA programming:
Connect a USB cable between a PC and the COM-1600 DEV port. Power up the assembly. From the ComBlock Control Center software, detect the modules. Click on the swiss army knife button and program the ready-to-use FPGA firmware com1600_use_example_rgmii.mcs located in use_example/bin/

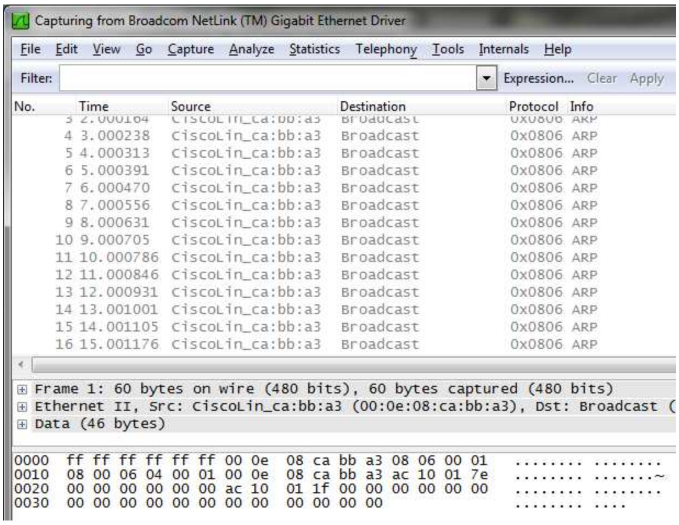
FPGA configuration:
From the ComBlock Control Center, click on the settings button and enter a 48-bit MAC address in control registers REG0 through REG5 such as 000102030405. Set REG6 as 0F.

Connect a LAN cable between the ComBlock RG45 connector and a PC. Any Cat5 cable will work (no need for a special cross-over cable).

LINK check: a green LED will turn on the ComBlock RJ45 connector (other colors if the PC is not 1000Mbps capable). Likewise, the PC LAN port will also turn on its LINK LED.

Start a LAN analyzer like Wireshark on the PC.

Transmit check: the LAN analyzer will detect short broadcast messages sent by the ComBlock once every second. This frame is defined in the *LAN_TX_TEST.vhd* component.



Receive check:
From the ComBlock Control Center, click on the status button.
Verify that the number of received frames (SREG11 & SREG10) increases while all error counters (SREG12 through SREG21) remain at zero.
SREG11/10: number of received frames
SREG13/12: number of frames with bad CRC
SREG15/14: number of frames too short (<64B)
SREG17/16: number of frames too long (>1518B)
SREG19/18: number of frames where address does not match (and promiscuous mode is off)

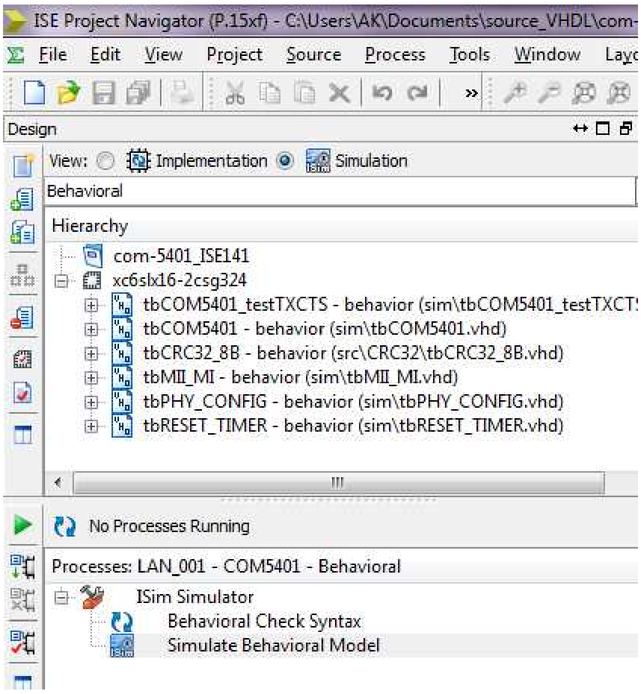
SREG21/20: number of frames with length field inconsistent with actual received frame length.

Real-time tx/rx check:
To gain a better understanding of the *COM5401.vhd* code, it may be helpful to probe the following test points with an oscilloscope probe.
J6/A1: tx data from user
J6/A2: tx flow control to the user
J6/A3: start tx to PHY
J6/A4: collision
J6/A5: done sending frame to PHY
J6/A6: new rx frame
J6/A7: rx frame delimiter
J6/A8: rx frame valid byte
J6/A9: rx frame complete
J6/A10: rx frame, invalid CRC

Quick start with VHDL simulation

Several testbenches located in the /sim directory can be used to validate the VHDL code. Some focus on detailed areas (CRC32, MDIO timing, PHY configuration), while others create stimulus to exercise the entire Ethernet MAC.

The easiest way to start is to use the Xilinx ISE tools which include the ISIM VHDL simulator.



Click on View Simulation.
Highlight one of the testbenches, and click on "Simulate behavioral model" to start the ISIM VHDL simulator.

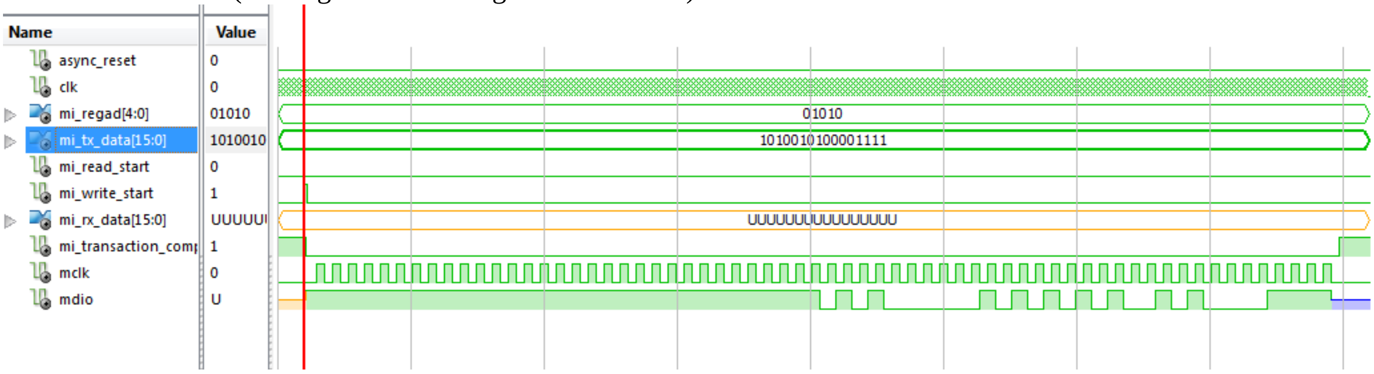
For example, the tbCOM5401.vhd testbench sends a 42-byte Ethernet frame to the RGMII PHY where it is looped back. This allows one to visualize the PHY interface signals, padding and CRC insertion by the MAC layer and the frame verification upon reception.

The SIMULATION constant (typically at the tope level) should be set to '1' to enable configurations specific to the VHDL simulation, shorten long timers for example. These constants should revert to '0' prior to synthesis.

MII Management Interface

The PHY is managed through a two-wire Management Data Input/Output (MDIO) interface. The MDIO is a synchronous serial link comprising two signals: a clock MCLK and a bi-directional data line MDIO. The MDIO timing diagram is specified by the IEEE 802.3 standard.
The component *MII_MI.vhd* implements a read or write transaction, converting a 16-bit parallel register value and 5-bit register address to a serial stream and vice-versa.

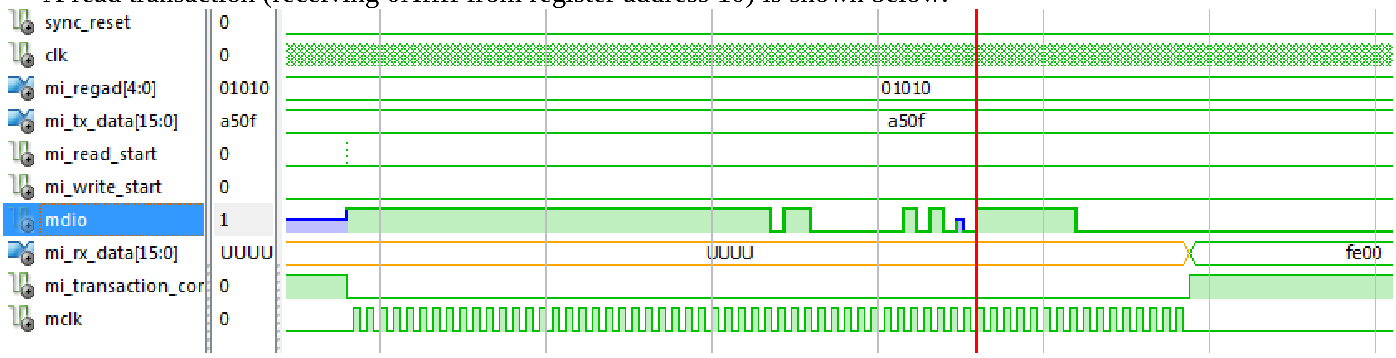
A write transaction (sending 0xA50F to register address 10) is illustrated below:



The write sequence consists of

(a) 32-bit preamble field (all ones)
(b) "0101"
(c) 5-bit PHY address, here fixed at 0
(d) REG address MI_REGAD[4:0]
(e) "10"
(f) 16-bit data field MI_TX_DATA[15:0]

A read transaction (receiving 0Xffff from register address 10) is shown below:



The read sequence consists of

(g) a 32-bit preamble field (all ones) to the PHY
(h) "0110" to the PHY
(i) 5-bit PHY address, here fixed at 0 to the PHY
(j) REG address MI_REGAD[4:0] to the PHY
(k) "Z"
(l) "0" from the PHY
(m) 16-bit data field MI_RX_DATA[15:0] from the PHY

The PHY generally sets a speed limit for the MDIO interface. For example, the Micrel KSZ9021 PHY defines the typical MCLK frequency as 2.5 MHz. The *MII_MI.vhd* component includes a constant (MCLK_COUNTER_DIV) to adjust the MCLK frequency by dividing the processing clock CLK. The designer should adjust this constant prior to synthesis, depending on the specific MDIO timing requirements of the PHY IC.

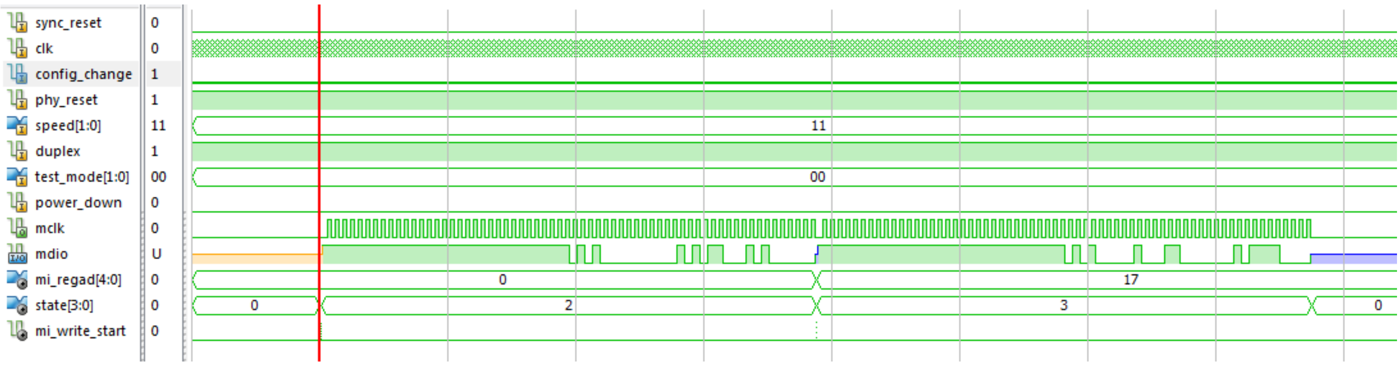
PHY configuration

The *PHY_CONFIG.vhd* component encapsulates the PHY configuration as specified by the user. The configuration is triggered by a single pulse on the CONFIG_CHANGE input.

The key configuration parameters are brought to the interface so that the user can change them dynamically at run time. Other, more arcane, parameters are fixed at the time of VHDL synthesis.

Dynamic configuration parameter	Definition
PHY_RESET	1 = PHY software reset, 0 = no reset
SPEED	00 = force 10 Mbps 01 = force 100 Mbps 10 = force 1000 Mbps 11 = auto-negotiation
DUPLEX	1 = full-duplex, 0 = half-duplex
TEST_MODE	00 = normal mode 01 = loopback mode 10 = remote loopback 11 = led test mode
POWER_DOWN	software power down mode. 1 = enabled, 0 = disabled.

A CONFIG_CHANGE pulse will trigger the state machine as shown below. The *PHY_CONFIG.vhd* component subsequently writes to two PHY control registers at register addresses 0 and 17 respectively.



PHY strapping options configuration

Depending on the PHY integrated circuit, a few configuration options are set at the time of power-up or reset. For example, the Micrel KSZ9021RN PHY uses general output pins (RX_D, RX_DV, etc) as temporary inputs during power-up or reset. These temporary inputs allow the FPGA to configure a few PHY options. The designer should therefore define pull-ups or pull-downs for these dual-function signals in the .ucf constraint file.

Example:

```
# strap-in configuration. Micrel KSZ9021RN
# advertise all capabilities: 10/100/1000
NET "RXD<3>" PULLUP ;
NET "RXD<2>" PULLUP ;
NET "RXD<1>" PULLUP ;
NET "RXD<0>" PULLUP ;
# enable 125 MHz clock reference to FPGA (at least for one PHY, not needed for all PHYs)
NET "RX_CTL" PULLUP;
# dual LED mode
NET "CLK125_NDO" PULLDOWN;
# PHYAD2   This PHY address is 4
NET "RXC" PULLUP;
# repeat the code above for each PHY
```

The PHY may also impose a minimum reset duration at power up. For example, the Micrel KSZ9021RN PHY requires a minimum 10ms reset duration at power up. The *RESET_TIMER.vhd* component generates such a reset. Upon de-assertion of the RESET_N signal, the PHY reads the strapping options as defined in the .ucf file. Following the reset, the PHY needs another 40ms to start. The *RESET_TIMER.vhd* delays the PHY configuration until the PHY is up and running (as visible from the 125 MHz clock output from the PHY).

RGMII Interface

The *RGMII_WRAPPER.vhd* component translates the 6-pin receive PHY interface (DDR, 4-bit niblets) into a simpler (single clock edge, data-byte) interface. A symmetrical translation is performed on the transmit side, as illustrated below:

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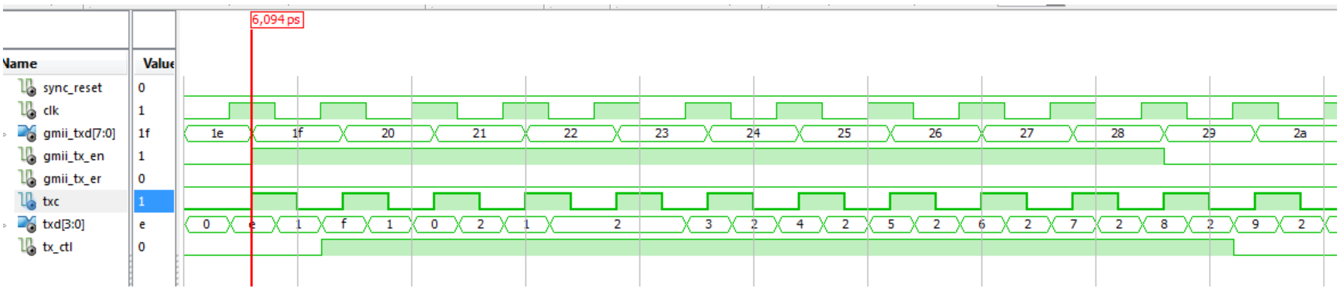
RGMII Transmit Side :



The *RGMII_WRAPPER.vhd* component includes two delays to be configured prior to synthesis:
constant RXC_DELAY: integer range 0 to 255 := 32; -- adjust as needed. Here: 2ns
constant TXC_DELAY: integer range 0 to 255 := 32; -- adjust as needed. Here: 2ns

These delays offset the RXC and TXC synchronous clocks so as to avoid a race condition (and the possible resulting glitches) when reclocking the data with the associated clock at the receiving end. The recommended delay is between 1.5 and 2.0 ns [2]. When the clocks operate at 125 MHz, the IODELAY2 Xilinx primitive implements a delay by increments of 16ns/256 = 62.5ps. Thus, a configuration value of 32 results in a 2ns delay.

The *RGMII_WRAPPER.vhd* component includes two methods for creating a 2ns offset between the receive clock RXC and the receive data. The baseline method is to set the delay in the extended control register 260 of the PHY. This method works well with Micrel KSZ9021 PHY but may not be supported by other Manufacturers' PHYs. An alternative method using IODELAY2 in the FPGA is also coded but currently commented out.

GMII/MII Interface

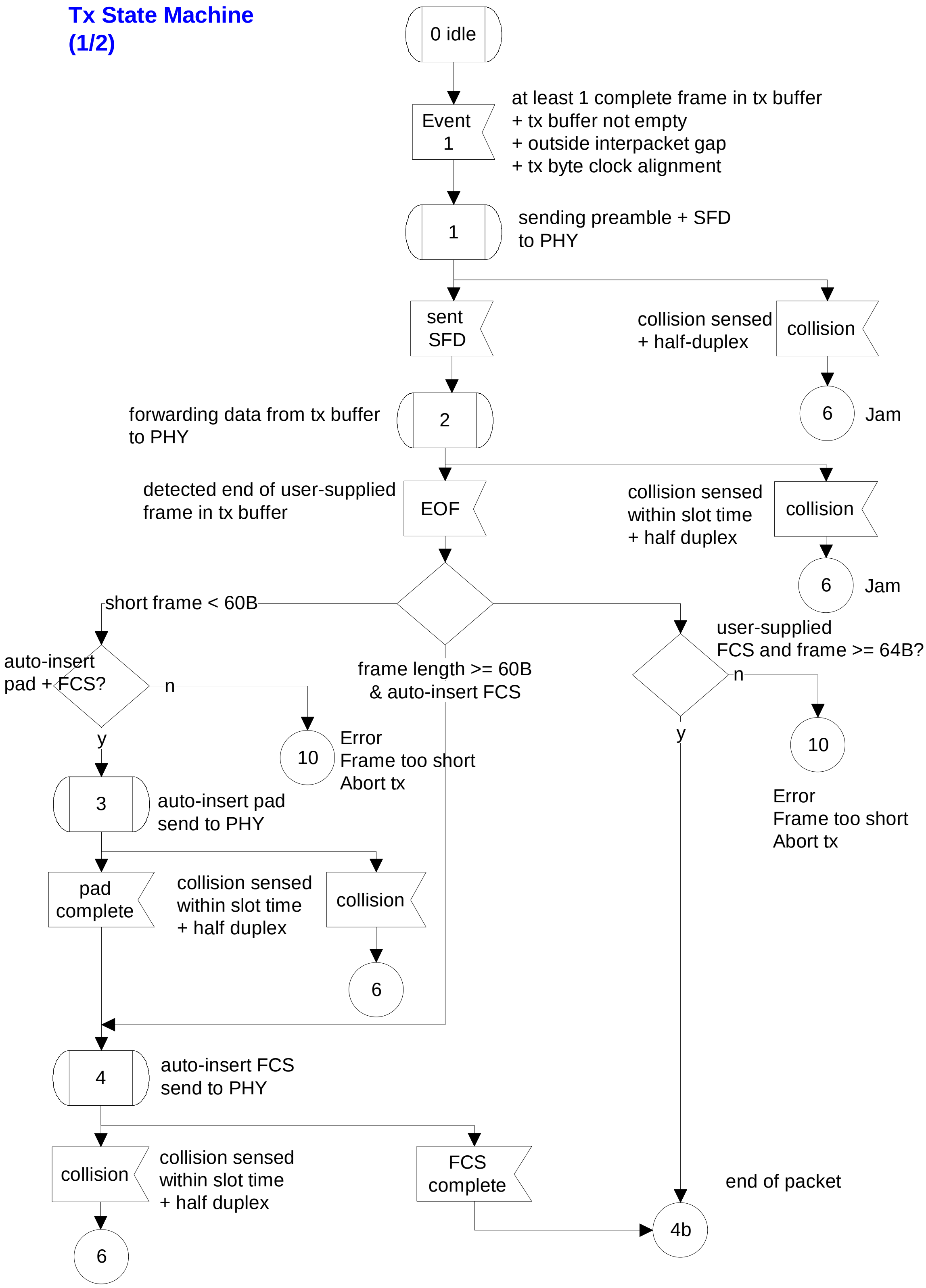
The *GMII_MII_WRAPPER.vhd* component reformat signals exchanged between the FPGA and an external GMII/MII PHY.

The receive clock RX_CLK is always supplied by the PHY to the FPGA. Its frequency (2.5,25 or 125 MHz) depends on the 10/100/1000 Mbps link speed negotiated by the PHY.

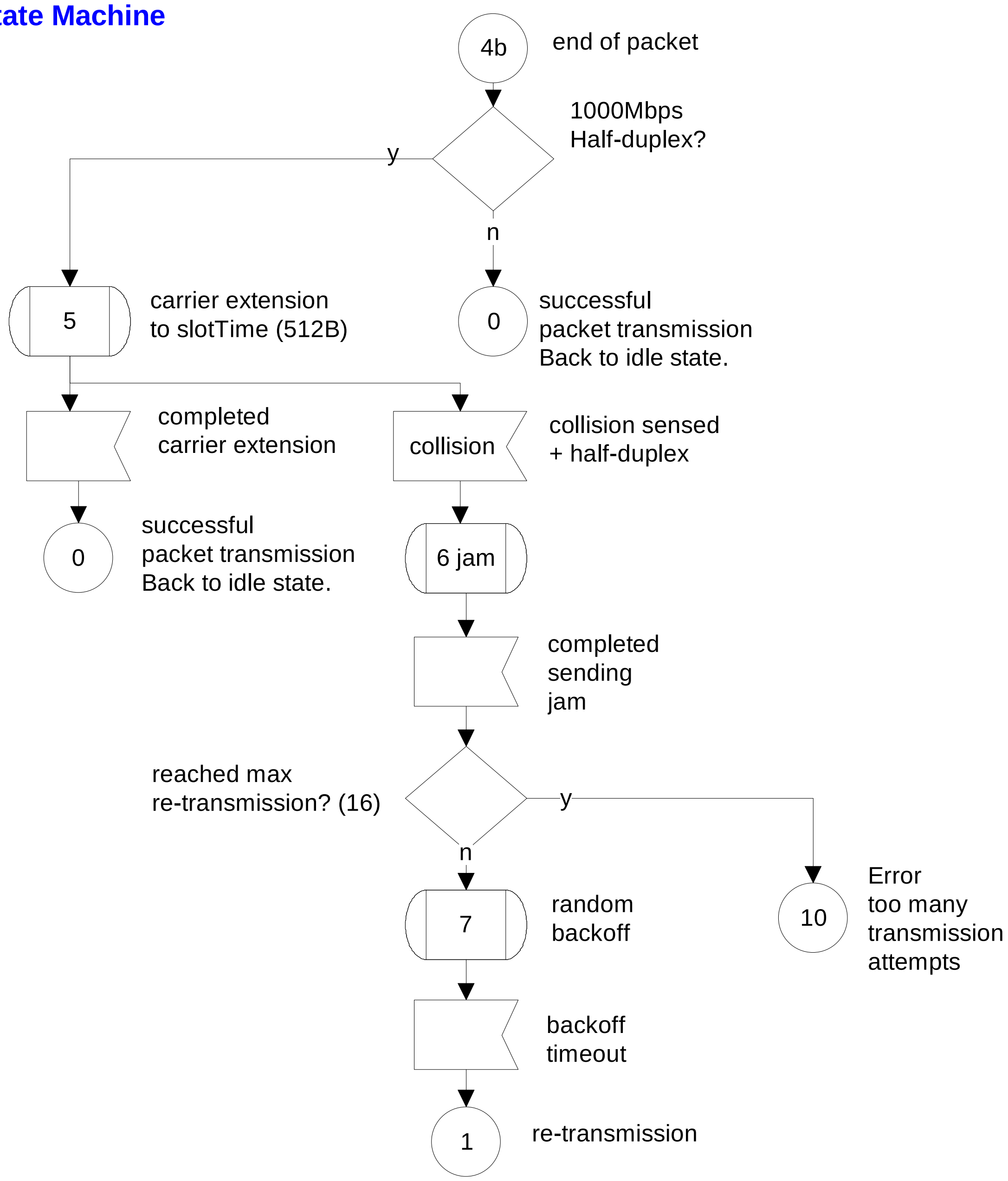
The transmit clock direction depends on the selected speed:
The MII TX_CLK is from the PHY to the FPGA, at speeds of 2.5 or 25 MHz (10/100 Mbps link)
The GMII GTX_CLK is a 125 MHz from the FPGA to the PHY (1000 Mbps link)

MAC Tx State Machine

The tx state machine is described by the SDL flowchart below:



Tx State Machine (2/2)



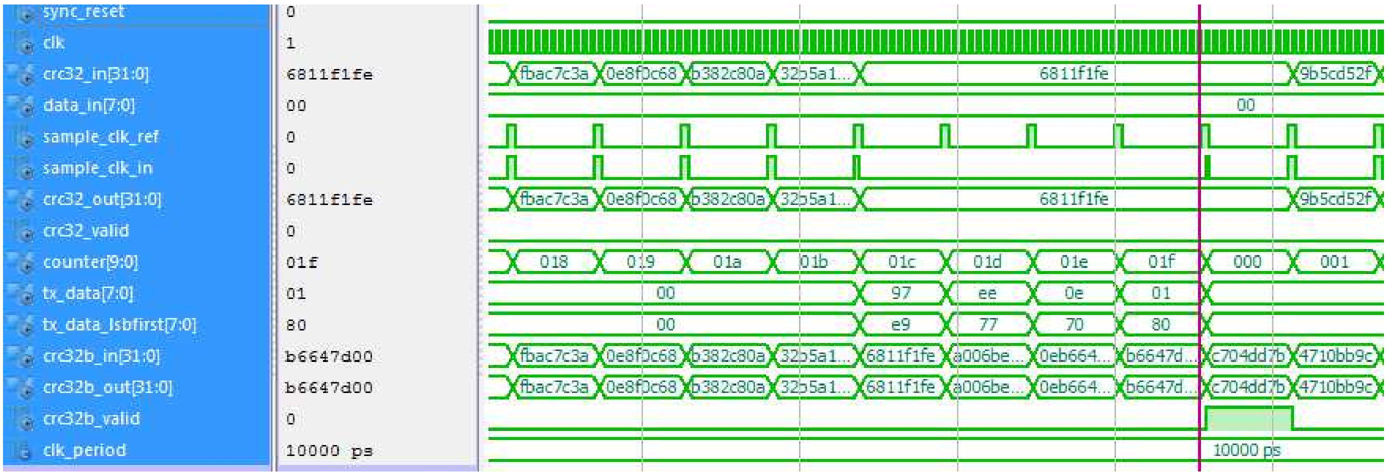
MAC CRC32

All 802.11 frame include a 32-bit CRC (frame check sequence FCS). As part of the MAC layer processing, this software automatically appends the 32-bit CRC at transmission and verifies the CRC validity upon receiving a frame from the PHY. A single VHDL component *crc32_8b.vhd* is used for both CRC32 generation and CRC check.

The algorithm is as follows:

(a) The CRC32 field is set to x"FFFFFFFF" at the start of frame.
(b) Parallel implementation of the CRC32 takes one clock for each input byte.
(c) The generator polynomial is
$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{8} + x^{7} + x^{5} + x^{4} + x^{2} + x + 1.$
(d) The CRC is inverted prior to transmission. The transmission is least significant bit first.
(e) Verification is done by feeding an entire frame (including the 32-bit CRC at the end) into the *crc32_8b.vhd* component. When the frame is error free, the resulting CRC is the residual value 0xC704DD7B. This causes the CRC32_VALID flag to go high.

The tb*crc32_8b.vhd* testbench was created to verify proper operation. A null frame with 28 "00" bytes result in a 32-bit CRC x"6811f1fe". The CRC is inverted and flipped LSb first. Upon receiving this CRC at the end of a frame, the CRC check indicates a valid frame by raising the CRC32_VALID flag.



An alternate test bench tb*crc32_8b_alt.vhd* verifies the32-bit CRC for a packet collected over the LAN (assumed valid).

ComBlock Compatibility List

FPGA development platform	
COM-1600	FPGA + ARM + DDR2 + USB2 + NAND development platform
COM-1500	FPGA + DDR2 SODIMM socket + ARM development platform
Network adapter	
COM-5102	1-port 10/100/1000 Mbps Ethernet Transceiver + HDMI
COM-5401	4-port 10/100/1000 Mbps Ethernet Transceivers
Software	
COM-5402SOFT	IP/TCP/UDP for Gigabit Ethernet, VHDL Source / IP Core

ComBlock Ordering Information

COM-5401SOFT Tri-Mode 10/100/1000 Ethernet MAC, VHDL SOURCE CODE

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