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COM-1801SOFT PSK/QAM/APSK Modem VHDL source code overview / IP core

.Overview

The COM-1801SOFT PSK/QAM/APSK modem is a digital modulator and demodulator- written in generic VHDL.

The entire **VHDL source code** is deliverable. It is portable to a variety of FPGA targets.

Key features and performance:

- Flexible programmable features:
  - Multiple modulation types with 1 to 5 bits per symbol: BPSK, QPSK, 8-PSK, 16-QAM, 16-APSK, 32-APSK.
  - Symbol rate up to $f_{clk}/2$ -1%, where f_{clk} is the processing clock frequency. 32-bit precision.
- 4-bit soft-decision demodulator output for interface to FEC decoders.
- Framing structure for demodulator frequency acquisition and phase ambiguity removal.
- Performance:
  - Near theoretical BER vs Eb/No: demod implementation loss < 0.5dB (QPSK)
  - ±50ppm symbol timing tracking
  - Carrier frequency acquisition: ±10% of symbol rate at the threshold
  - Acquisition threshold < -1dB Eb/No
- Provided with IP core:
  - VHDL source code
  - Matlab .m file for generating stimulus files for VHDL simulation of the demodulator and for end-to-end BER performance analysis at various signal to noise ratios
  - VHDL testbenches (back-to-back modem or stimulus file input)
  - PRBS11 test sequence generator, AWGN noise generator, BER tester

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.Configuration

Pre-Synthesis configuration parameters

The following constants are user-defined in the components generic section prior to synthesis. These parameters generally affect the size of the embodiment.

Synthesis-time configuration parameters	
Modulator Parameters	
SYNC_LENGTH	Periodic sync marker length, in number of symbols. Typically 32 or 64
Demodulator Parameters	
SYNC_LENGTH	Periodic sync marker length, in number of symbols. Typically 32 or 64
BER_INST	'1' to instantiate a Bit Error Rate Tester.

Run-time configuration parameters

The user can set and modify the following controls at run-time through the top level component interface:

Modulator Parameters	Configuration
SYMBOL_RATE(31:0)	symbol rate expressed as fsymbol_rate/f_{clk} * 2^32
GAIN(16:0)	output amplitude scaling factor. 16-bit unsigned
CENTER_FREQ(31:0)	modulated signal center frequency. Expressed as fc/ f_{clk} * 2^32
BURST_LENGTH(15:0)	Payload field length, in number of symbols. Excludes the sync marker length Constraints: Total number of bits per frame must be a multiple of 8.
CONTROL(15:0)	bits 5:0 modulation type 0: BPSK 1: QPSK 8: 8PSK 16: 16QAM 24: 16APSK 32: 32APSK bit 6: spectrum inversion bit 7: spectrum shaping
	filter enable bits 9:8 test mode: 00 no test, 01 = PRBS11, 11 = unmodulated carrier bits 10-12: SRRC rolloff factor
SYNC_WORD(63/31:0)	Sync marker, inserted periodically once per frame. Current code supports 32-bit and 64-bit length sync markers.
SYNC_EN	Enable periodic sync marker insertion. Generally enabled as the sync marker is essential in recovering any phase ambiguity at the receiving end.

Receiver Parameters	Configuration
AGC_RESPONSE(4:0)	Adjust the AGC response time. approximately log2(NSymbols).
RECEIVER_CENTER_FREQ(31:0)	nominal (i.e. expected) center frequency. 32-bit signed (2's complement) Expressed as f_c/ f_{clk} * 2^32
CIC_R(15:0)	CIC Decimation ratio. The output sampling rate is thus f_{clk}/R -- 1 to bypass. 0 is illegal, otherwise, nominal range is 1 to 16384. -- Usage: be careful not to decimate too much as the CIC decimation filter is not very sharp and thus can distort the modulated signal. -- Rule of thumb: the CIC filter output sampling rate should be >= 4 samples per symbol.
NOMINAL_SYMBOL_RATE(31:0)	$f_{symbol\ rate}$ / f_{clk} * 2^32 = nominal symbol rate
FRAME_LENGTH(15:0)	Frame length, in symbols, including payload + sync marker.

DEMOD_CONTROL	bits 5:0 modulation type 0: BPSK 1: QPSK 8: 8PSK 16: 16QAM 24: 16APSK 32: 32APSK bit 6: spectrum inversion bit 7: enable(1)/disable(0) sync marker detection and removal at output. Generally enabled. bits 10-12: SRRC rolloff factor
SYNC_WORD(63/31:0)	Sync marker, inserted periodically once per frame. Current code detects 32-bit and 64-bit length sync markers.

.I/Os

.General

CLK: input
Synchronous clock. The modulator and demodulator components typically use distinct synchronous clocks: DAC sampling clock for the modulator and ADC sampling clock for the demodulator.

The synchronous clocks must be global clocks (use BUFG). The timing periods must be constrained in the .xdc constraint file associated with the project.

SYNC_RESET: input
Synchronous reset. The reset MUST be exercised at least once to initialize the internal variables. It must be exercised whenever a control parameter is changed.

When the modulator and demodulator use different synchronous clocks, they must use different synchronous resets.

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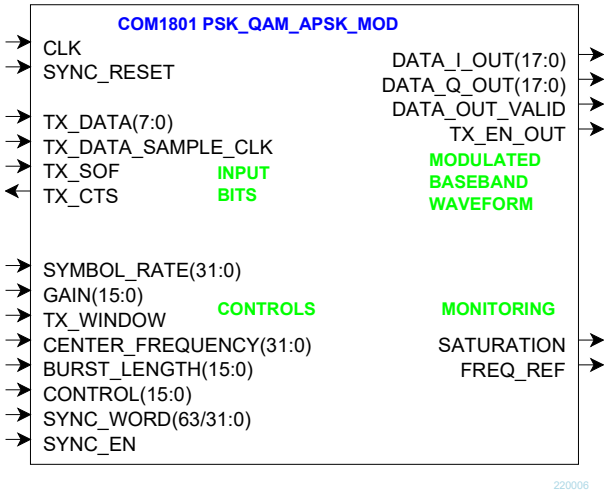
.Modulator

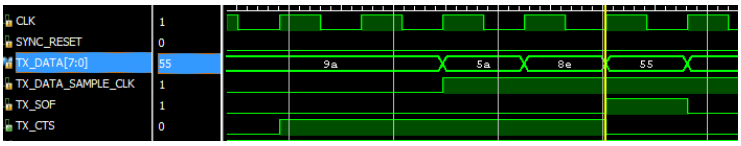


TX_DATA(7:0): Input data byte. The MSb is sent first.

TX_DATA_SAMPLE_CLK: input.
1 CLK-wide pulse indicating that TX_DATA is valid.

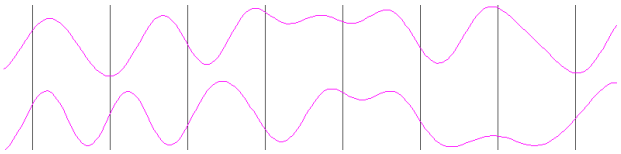
TX_SOF: input Start Of Frame. 1 CLK-wide pulse. The SOF is aligned with **TX_DATA_SAMPLE_CLK**.

TX_CTS: output.
Clear-To-Send flow control. '1' indicates that the modulator is ready to accept another input byte. Thanks to an input elastic buffer, the data source is allowed to send a few more bytes after TX_CTS goes low.



Modulator input flow control example

DATA_I/Q_OUT(17:0): Modulated baseband output samples (I = in-phase, Q = quadrature). Read when **DATA_OUT_VALID** = '1'. Format: 2's complement (signed)

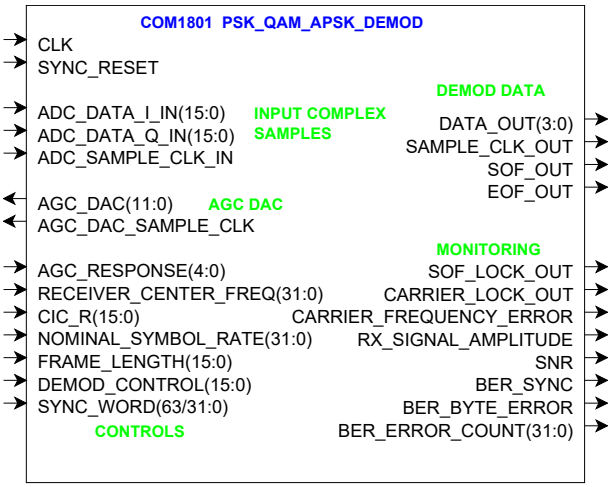


DATA_OUT_VALID: generally all 1s.

TX_EN_OUT: goes low to turn off an external power amplifier when the modulator is not receiving any input data.

For more information about the input/output signals, please refer to the PSK_QAM_APSK_MOD.vhd component declaration.

.Receiver



ADC_DATA_I/Q_IN(15:0): input samples from one or two external ADCs. (one in the case of IF undersampling, two for near-zero frequency complex inputs). If the ADCs have fewer than 16-bit precision, align the most significant bit with ADC_DATA_IN(15). Format: 2's complement (signed).

ADC_SAMPLE_CLK_IN: valid signal for the **ADC_DATA_I/Q_IN** input samples. Generally a solid '1'.

AGC_DAC(11:0): output to an external DAC to control an external AGC. Read when **AGC_DAC_SAMPLE_CLK** is '1'

DATA_OUT(3:0): soft-decision output. The demodulated bit is bit 3. The three lower bits indicate the level of confidence: "0000" for a solid '0', "1111" for a solid '1', "1000" for a '1' barely above the thresold.

SAMPLE_CLK_OUT: valid signal for the **DATA_OUT** output.

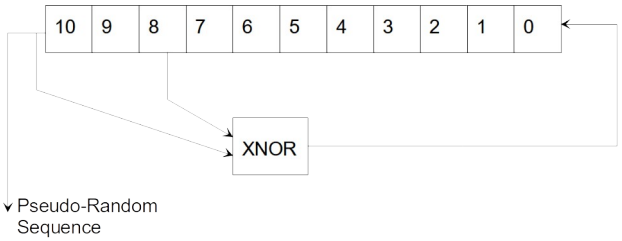
SOF_OUT/EOF_OUT: 1 clock-wide pulses marking the Start/End Of Frames. Aligned with the first/last **SAMPLE_CLK_OUT** in a frame.

For more information about the input/output signals, please refer to the PSK_QAM_APSK_DEMOD.vhd component declaration.

.Operation

.PRBS-11 Pseudo-Random Bit Stream

In order to perform bit error rate measurements at the receiver, a pseudo-random binary sequence can be inserted at the transmitter input (thus replacing any user data). BER measurement is made by counting actual errors in the received bit stream. The received bit stream is compared with a locally generated replica of the reference PRBS-11 sequence.
The reference sequence is a periodic 2047-bit long maximum length sequence generated by a 11-tap linear feedback shift register:



The first 100 bits of the PN sequence are as follows:
0000000000 0111111111 0011111110 0001111100 1100111000 0000010011 1111010001 1110110100 1101001100 0011000001

.Format Conversion

Serial to parallel conversion occurs at the interface between the modem and the application. The general rule is that the first received bit is placed at the MSb position in the byte.

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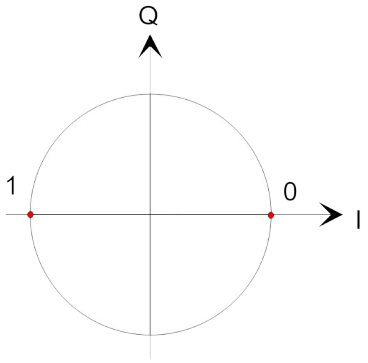
.Constellation: Symbol Mapping

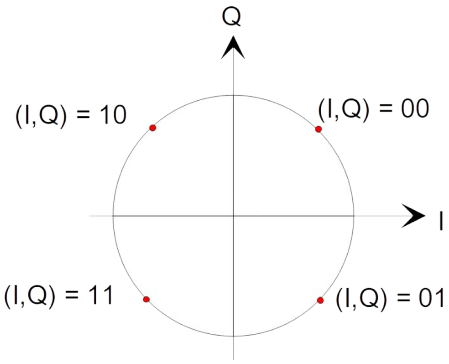
The packing of serial data stream into symbols is done with the Most Significant bit first.

.BPSK

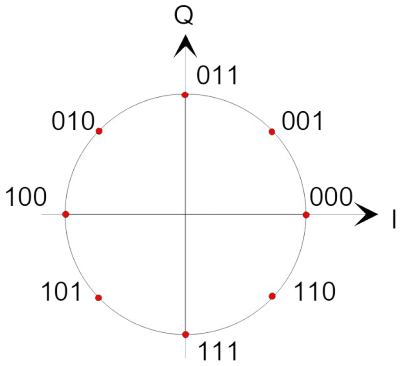


.QPSK

Gray encoding.



.8PSK (1)



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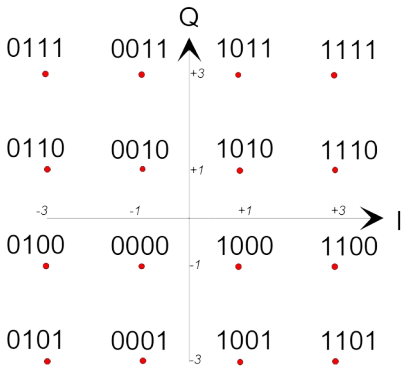
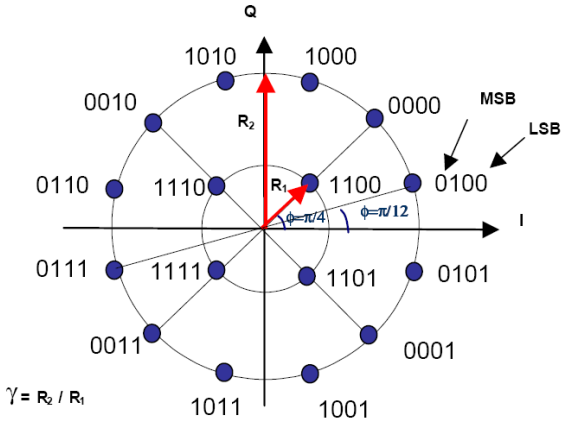
.16QAM



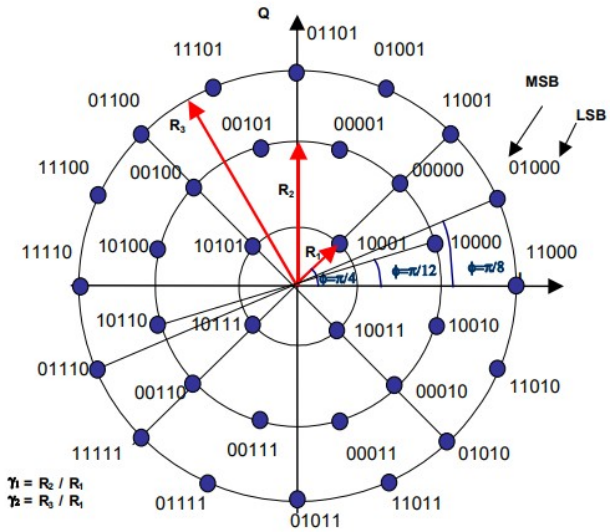
.16APSK

γ = R2 / R1 = 2.85, best for code rate 3/4



.32APSK

γ1 = 2.84, γ2 = 5.27, best for code rate 3/4



.Channel Filter Response

The same square-root raised cosine (SRRC) filter type is used at the modulator for spectral shaping and at the receiver for noise rejection. This filter is used for all modulations types. It is applied to both In-phase and Quadrature signals at baseband. The filters vary slightly by their 'rolloff factor'. In order to minimize intersymbol interferences, the same rolloff factor should be used at both the modulator and demodulator. To this effect, users can select one of several rolloff factors: 20%, 25%, 35%.

.Framing

32 or 64-bit sync markers can be inserted periodically at the modulator. The purpose is three-fold:

- delineate frames and convey frame boundary information from modulator input to demodulator output.
- estimate input signal frequency error at the demodulator
- remove inherent phase ambiguities at the demodulator.

Enabling sync markers is required for all higher order modulations

Example of sync markers:

32-bit: 0x5A0FBE66, 0x1ACFFC1D
64-bit: 0x034776C7272895B0

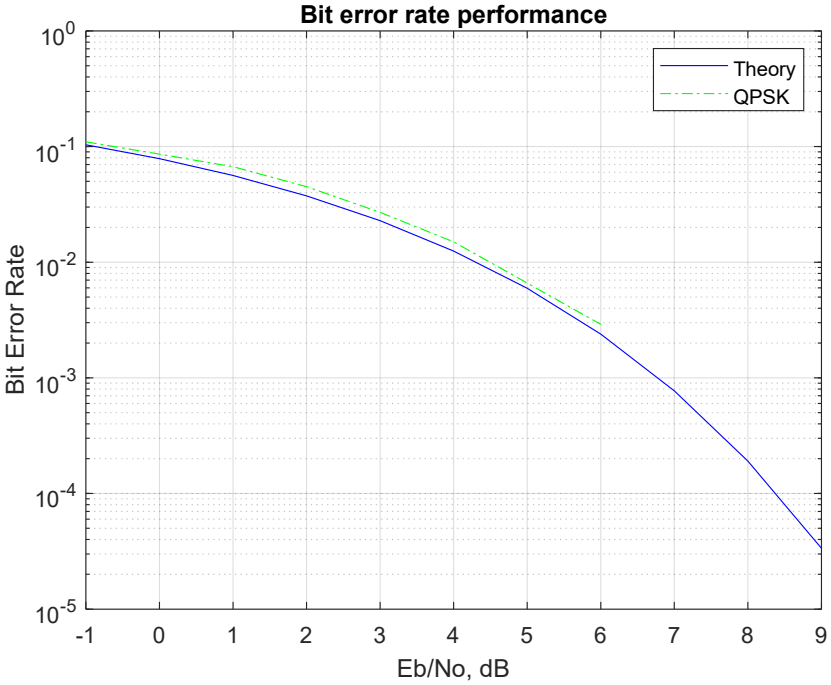
The sync marker is user-programmable.

Sync markers are modulated as BPSK, irrespective of the selected modulation scheme for the payload field.

.Performance

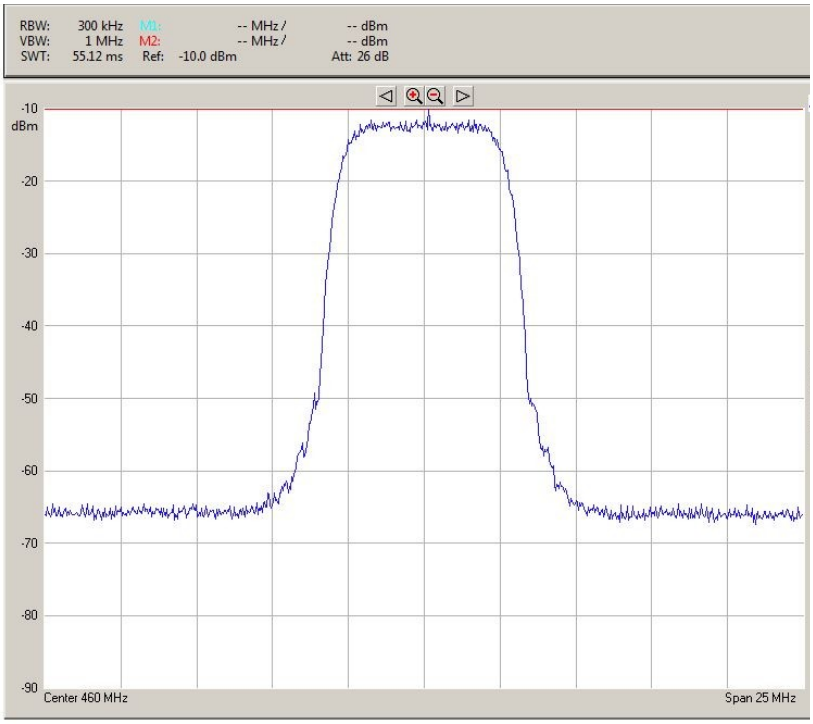
.BER vs Eb/No

The plot below shows near-theoretical performance for the demodulator without error correction.



Test condition: +0ppm symbol timing error, 0 Hz frequency error

.Transmitted spectrum



QPSK 10MSymbols/s, root raised cosine filter 20% rolloff

.Latency

The latency between received signal and demodulated bit output is approximately 20 bits.

.Software Licensing

This software is supplied under the following key licensing terms:

1. A nonexclusive, nontransferable license to use the VHDL source code internally, and
2. An unlimited, royalty-free, nonexclusive transferable license to make and use products incorporating the licensed materials, solely in bit stream format, on a worldwide basis.

The complete VHDL/IP Software License Agreement can be downloaded from
http://www.comblock.com/download/softwarelicense.pdf

.Portability

The VHDL source code is written in generic VHDL and thus can be ported FPGAs from various vendors.

.Configuration Management

The current software revision is 041022.

Directory	Contents
/doc	Specifications, user manual, implementation documents
/src	.vhd source code,.pkg packages, .xdc constraint files (Xilinx) One component per file.
/sim	VHDL test benches
/matlab	Matlab .m file for generating stimulus files for VHDL simulation and for end-to-end BER performance analysis at various signal to noise ratios
/bin	.bit configuration files (for use with ComBlock COM-1800 FPGA development platform)

Project files:

Xilinx Vivado v2020.2 project file:
project_1V2020 modem only.xpr

.VHDL development environment

The VHDL software was developed using the following development environment:
Xilinx Vivado 2020.2 for synthesis, place and route and VHDL simulation

The entire project fits within a Xilinx Artix7-100T. Therefore, the ISE project can be processed using the free Xilinx WebPack tools.

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.Device Utilization Summary

The modulator size is fixed (not parameterized).

Device: Xilinx Artix7-100T

Resource	Estimation	Available	Utilization...
LUT	3481	63400	5.49
LUTRAM	76	19000	0.40
FF	4978	126800	3.93
BRAM	15.50	135	11.48
DSP	32	240	13.33
IO	185	285	64.91
BUFG	1	32	3.13

The receiver size is fixed (not parameterized).

Resource	Estimation	Available	Utilization...
LUT	9606	63400	15.15
LUTRAM	81	19000	0.43
FF	9070	126800	7.15
BRAM	1.50	135	1.11
DSP	51	240	21.25

.Clock frequency

The modulator and demodulator components each use a single global clock CLK.
Typical maximum clock frequencies for various FPGA families are listed below:

Device family	Modulator	Demodulator
Xilinx Artix 7 -1 speed grade	160 MHz	160 MHz
Xilinx Kintex ultrascale plus, -1 speed grade	288 MHz	280 MHz

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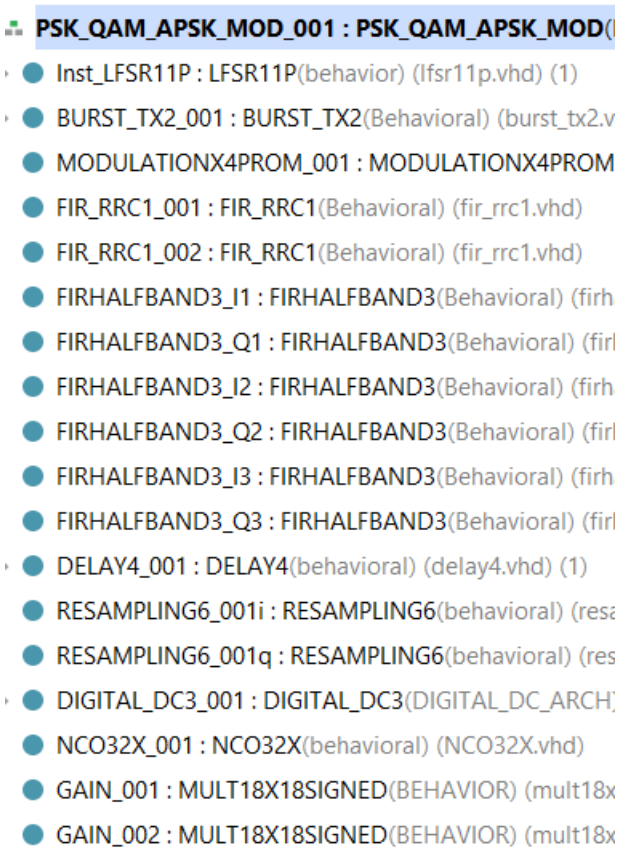
.Ready-to-use Hardware

The COM-1801SOFT was developed on, and therefore ready to use on the following commercial off-the-shelf hardware platform:

FPGA development platform
COM-1800 FPGA (XC7A100T) + ARM + DDR3 SODIMM socket + GbE LAN development platform

.VHDL components overview

.Modulator top level



PSK_QAM_APSK.vhd generates complex baseband (I/Q) sampled waveform from byte-size input data.

BURST_TX2.vhd stores input data in an elastic input buffer, then packs input bits into symbols (1,2,3,4,5 bits/symbol) at the specified symbol rate. Ia also inserts periodic sync markers when enabled. It also stops the transmitter when the input elastic buffer is empty.

MODULATIONX4PROM.vhd is a ROM storing the complex constellation points for each modulation type.

FIRRRC1.vhd implements a square root raised cosine FIR filter using classic multipliers and stored FIR filter coefficients. Currently supporting three sets of coefficients for 20%, 25% and 35% rollof factor. Implemented as a 21-tap FIR filter.

FIRHALFBAND3.vhd are half-band interpolation filters used to double the sampling rate. Implemented as a 20-tap FIR filter.

RESAMPLING6.vhd interpolates the modulated signal up to the DAC sampling rate. Implemented as a Farrow structure for parabolic interpolation (alpha = 0.5)

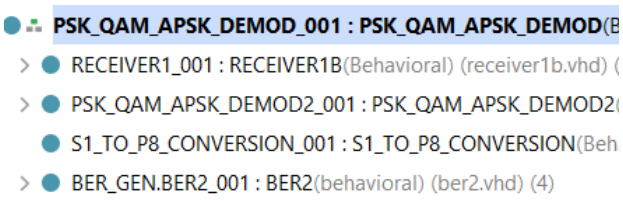
DIGITAL_DC3.vhd translates the modulated signal to a non-zero frequency. The 32-bit precision of the NCO frequency setting provides the user with a fine control over the output signal center frequency.

SIGNED_SIN_COS_TBL3.vhd stores sine and cosine functions in ROM. It is used to convert phase to complex I/Q baseband output samples.

COM1801_TOP.vhd: is mostly a use example when the modem is implemented on a ComBlock COM-1800 FPGA development platform. Please note that this top component can't be simulated as it makes many references to other components outside the scope of the modem proper (TCP stack, turbo codec, etc)

.Receiver top level

The receiver is comprised of two high-level components:



RECEIVER1B.vhd performs non modulation-specific tasks such as AGC, DC bias removal, frequency translation to baseband, anti-aliasing filtering and decimation.

PSK_QAM_APSK_DEMOD2.vhd performs the demodulation, including carrier tracking (for coherent demodulation), symbol timing tracking, AGC, channel filtering and sync marker detection.

Note: several components are included for special custom applications but not used in the baseline code:
FREQUENCY_SCAN.vhd,
FAST_FREQUENCY_DETECTION.vhd,

FRAME_SYNC.vhd performs the initial frame synchronization detection: it detects the periodic sync marker and estimates the frequency error. Designed to acquire a maximum center frequency error of +/- 10% of the symbol rate at the worst case Eb/No of -1 dB when configured for a 64-bit sync marker.

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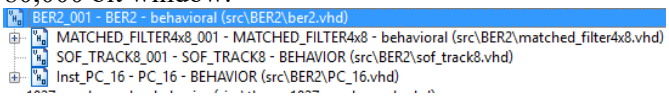
.Ancillary components

LFSR11P.vhd is a pseudo-random sequence generator used for test purposes. It generates a PRBS11 test sequence commonly used for bit error rate testing at the receiving end of a transmission channel.

BER2.vhd is a bit error rate tester expecting to receive a PRBS11 test sequence. It synchronizes with the received bit stream and count errors over a 80,000 bit window.



AWGN.vhd generates a precise Additive White Gaussian Noise. The noise bandwidth is 2*symbol rate.

INFILE2SIM.vhd reads an input file. This component is used by the testbench to read a modulated samples file generated by the `siggen_psk_qam_apsk.m` Matlab program for various Eb/No and frequency offset cases.

SIM2OUTFILE.vhd writes three 12-bit data variables to a tab delimited file which can be subsequently read by Matlab (load command) for plotting or analysis.

BRAM_DP2.vhd is a generic dual-port memory, used as input and output elastic buffers. Memory is inferred (no Xilinx primitive is used).

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.VHDL simulation

VHDL testbenches are located in the /sim directory.

The `tbPSK_QAM_APSK_modem.vhd` connects the modulator and demodulator back to back. End-to-end BER tests can be performed as the modulator includes a built-in pseudo-random sequence generator and the receiver includes a built-in Bit Error Rate Tester.

The `tbPSK_QAM_APSK_demod.vhd` testbench reads a tab-delimited stimulus files of modulated I/Q baseband complex input samples. The sampled waveform `input.txt` can be generated by the matlab program `siggen_psk_qam_apsk.m` The testbench demodulates the signal and measures the resulting BER.

.Matlab simulation

Matlab programs are located in the /matlab directory.

The `siggen_psk_qam_apsk.m` program generates a stimulus file `sim/input.txt` for use as input to the demodulator VHDL simulation (`tbPSK_QAM_APSK_demod.vhd`). The stimulus file includes a continuous stream of pseudo-random (PRBS11) data bits, PSK/QAM/APSK modulation, sync marker insertion, additive white Gaussian noise, channel filtering, frequency translation and quantization.

Care must be taken to match the modulator configuration in `siggen_psk_qam_apsk.m` and the demodulator configuration in `tbPSK_QAM_APSK_demod.vhd`.

This setup allows end-to-end BER testing, as the demodulator `PSK_QAM_APSK_DEMOD.vhd` includes a built-in bit error rate tester.

.Acronyms

Acronym	Definition
ADC	Analog to Digital Converter
AGC	Automatic Gain Control (loop)
APSK	Amplitude and Phase-Shift Keying modulation
AWGN	Additive White Gaussian Noise
BRAM	Dual-port Block RAM
BER	Bit Error Rate
CCSDS	Consultative Committee for Space Data Systems
CIC	Cascaded Integrator Comb filter
DAC	Digital to Analog Converter
DVB	Digital Video Broadcast
FIR	Finite Impulse Response filter
FPGA	Field Programmable Gate Arrays
LSb	Least Significant bit
LSB	Least Significant Byte
M&C	Monitoring and Control
MSb	Most Significant bit
MSB	Most Significant Byte
NCO	Numerically Controlled Oscillator
N/A	Not Applicable
PSK	Phase-Shift Keying modulation
PRBS-11	Pseudo-Random Binary Sequence, 2047-bit period
QAM	Quadrature Amplitude Modulation
ROM	Read-Only Memory
SCPC	Single Channel Per Carrier
SRRC	Square Root Raised Cosine filter

.ComBlock Ordering Information

COM-1801SOFT PSK/QAM/APSK Modem,
VHDL source code / IP core

.Contact Information

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