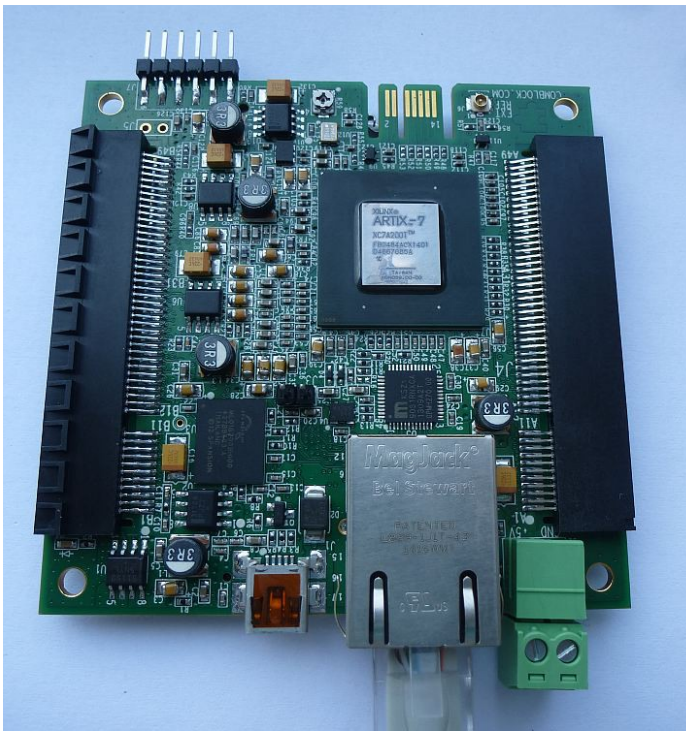
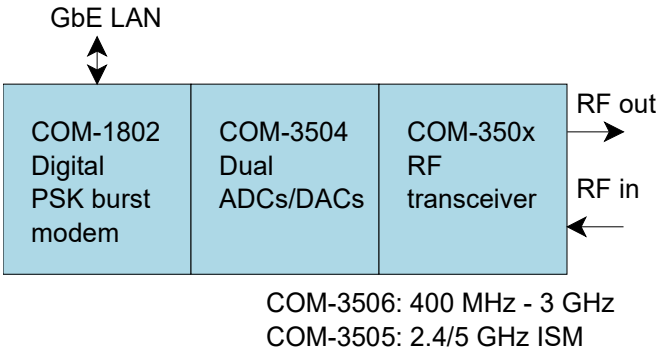
COM-1802 PSK Burst Modem 40 Msymbols/s

Key Features

- Digital modem with flexible configuration:
  - Variable data rates up to 39.5 Mbits/s
  - Frequency acquisition range: +/- 20% of symbol rate with no apriori knowledge.
  - Selectable payload field length up to 8000 symbols/frame. A burst can comprise one or multiple frames.
  - Usable as continuous mode, random access burst mode, or time-division multiple access (TDMA)
  - Includes convolutional (K=9, R=1/2) error correction
  - Modulation: BPSK, QPSK
  - Coherent demodulation for operation at low SNR
  - Modulator and demodulator are independently configured.
- Demodulator inputs: Digital (12-bit complex, up to 160Msamples/s)
- Modulator outputs: Digital (2 * 16-bit complex, up to 160 Msamples/s)
- Modem data I/Os:
  - 10/100/1000 Ethernet LAN/UDP
- Extensive test & monitoring:
  - BER measurement when transmitting PRBS-11 test sequence or frame sync.
  - PRBS-11 test sequence generator
  - Loopback mode
- Input for an external, higher-stability 10 MHz frequency reference.
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.



COM-1802



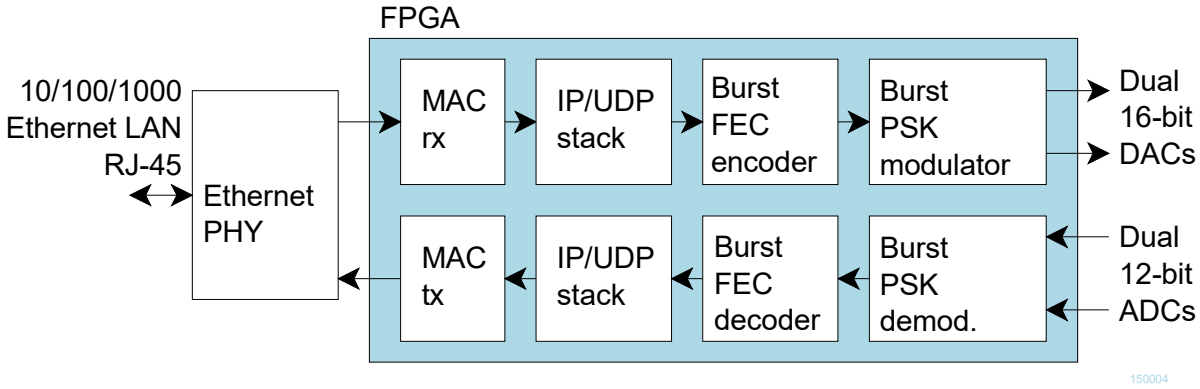
Assembly example

For the latest data sheet, please refer to the **ComBlock** web site: comblock.com/download/com1802.html.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to comblock.com/product_list.html .

MSS • 845 Quince Orchard Boulevard Ste N • Gaithersburg, Maryland 20878-1676 • U.S.A.
Telephone: (240) 631-1111 Facsimile: (240) 631-1676 www.ComBlock.com
 Issued 4/30/2016

Functional Block Diagram



Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

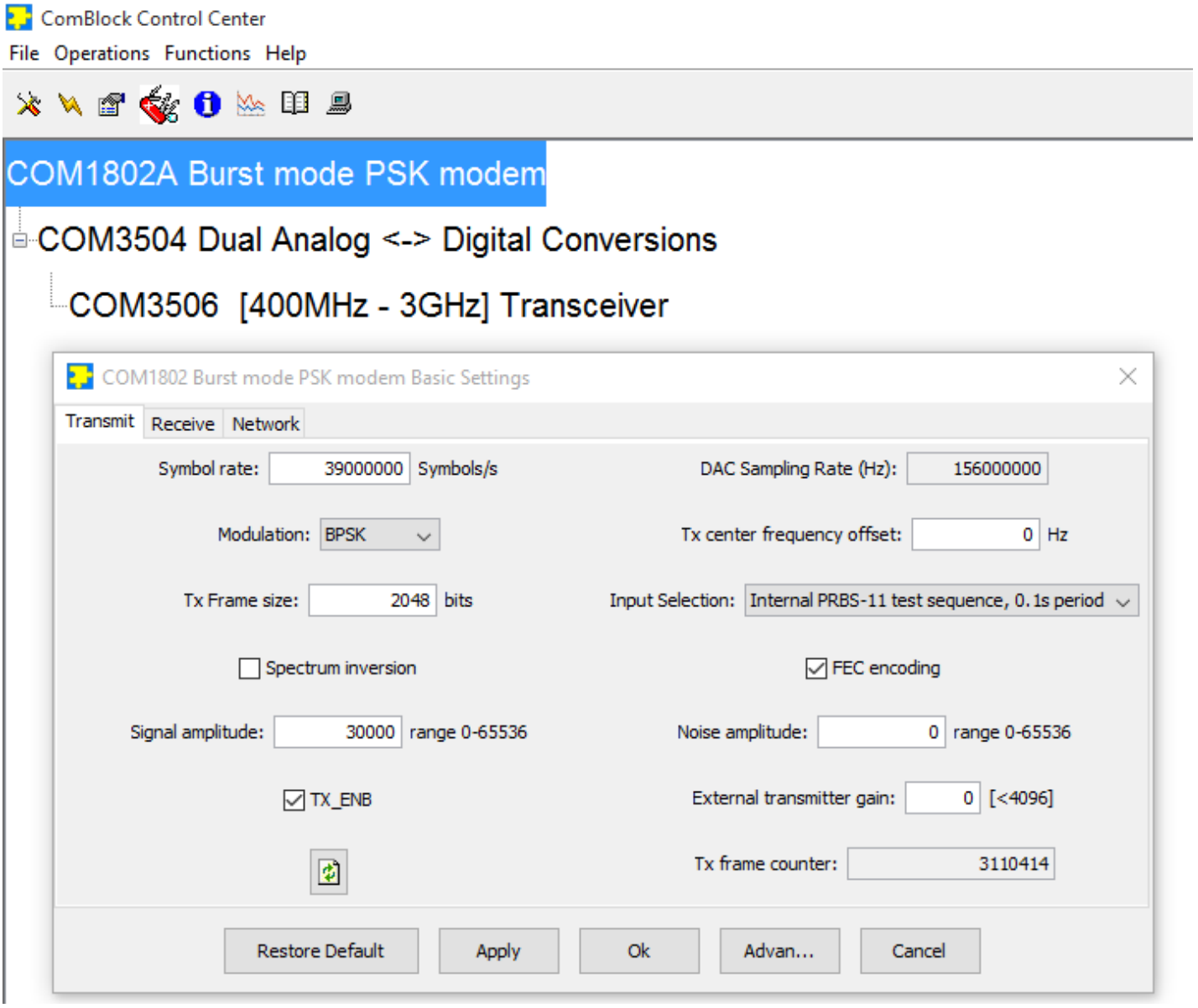
- USB, TCP-IP/LAN

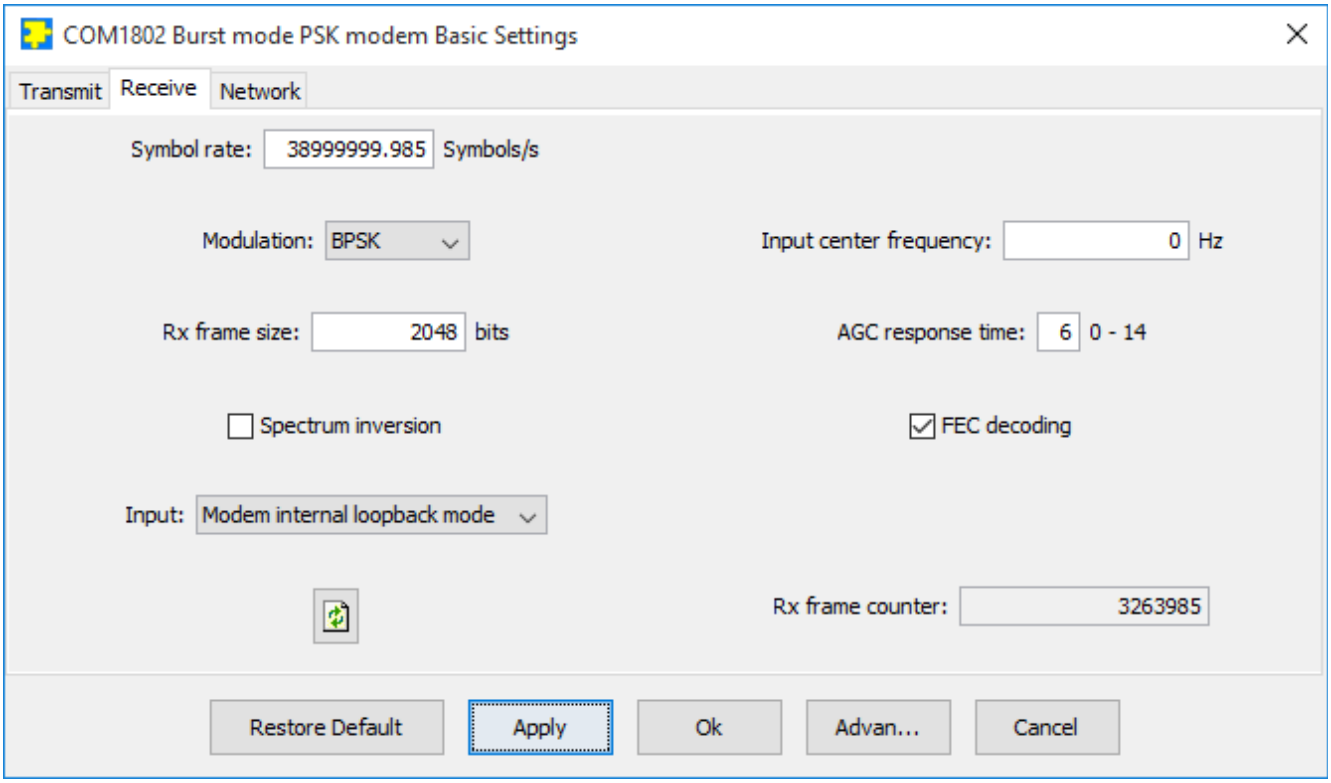
or connections via adjacent ComBlocks

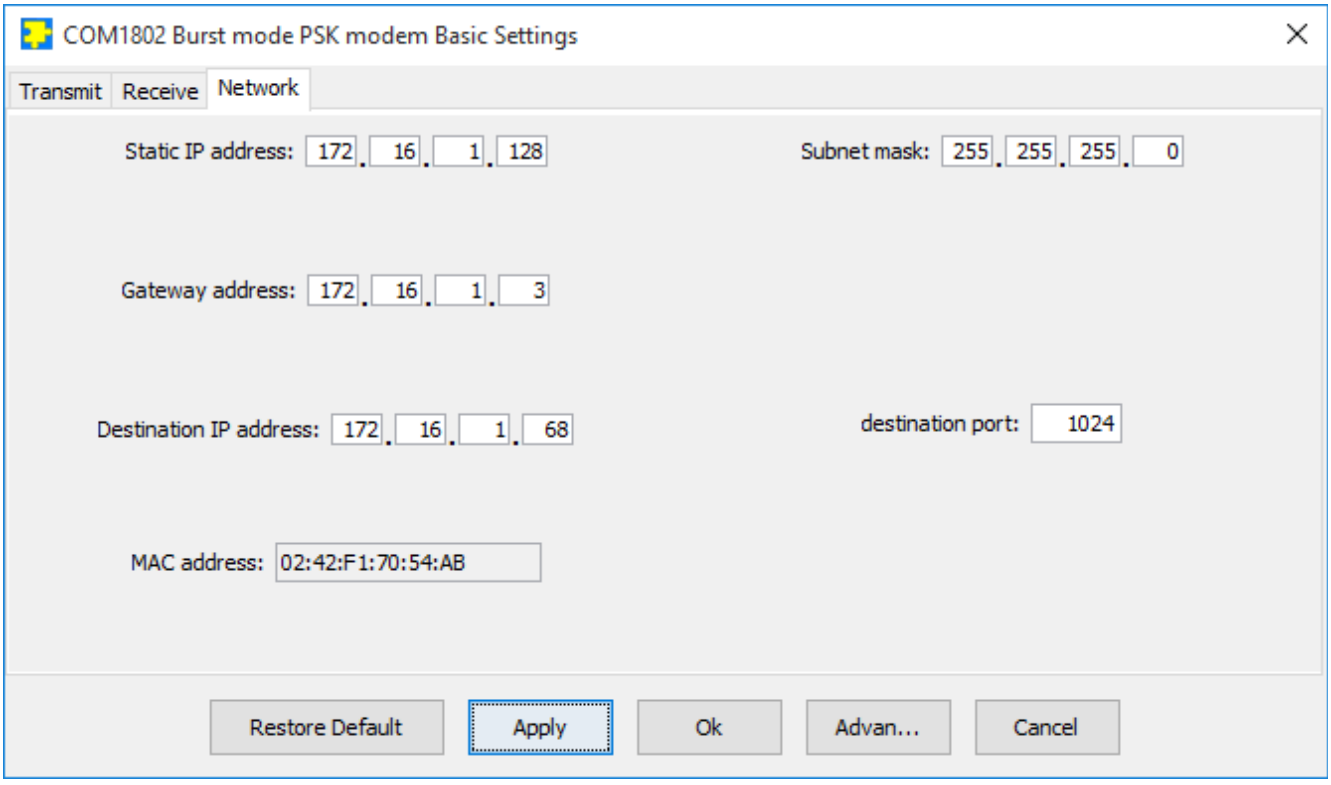
The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1802 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1802 module to be configured, next click the *Settings* button to display the *Settings* window shown below.


ComBlock Control Center
File Operations Functions Help
COM1802A Burst mode PSK modem
COM3504 Dual Analog <-> Digital Conversions
COM3506 [400MHz - 3GHz] Transceiver
COM1802 Burst mode PSK modem Basic Settings
Transmit
Receive
Network
Symbol rate:
39000000
Symbols/s
DAC Sampling Rate (Hz):
156000000
Modulation:
BPSK
Tx center frequency offset:
0
Hz
Tx Frame size:
2048
bits
Input Selection:
Internal PRBS-11 test sequence, 0.1s period
Spectrum inversion
FEC encoding
Signal amplitude:
30000
range 0-65536
Noise amplitude:
0
range 0-65536
TX_ENB
External transmitter gain:
0
[<4096]
Tx frame counter:
3110414
Restore Default
Apply
Ok
Advan...
Cancel


COM1802 Burst mode PSK modem Basic Settings
Transmit
Receive
Network
Symbol rate:
38999999.985
Symbols/s
Modulation:
BPSK
Input center frequency:
0
Hz
Rx frame size:
2048
bits
AGC response time:
6
0 - 14
Spectrum inversion
FEC decoding
Input:
Modem internal loopback mode
Rx frame counter:
3263985
Restore Default
Apply
Ok
Advan...
Cancel


COM1802 Burst mode PSK modem Basic Settings
Transmit
Receive
Network
Static IP address:
172
16
1
128
Subnet mask:
255
255
255
0
Gateway address:
172
16
1
3
Destination IP address:
172
16
1
68
destination port:
1024
MAC address:
02:42:F1:70:54:AB
Restore Default
Apply
Ok
Advan...
Cancel

Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write. Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

Several key parameters are computed on the basis of the 160 MHz ADC clock f_{clk_adc} or the 120 MHz internal processing clock f_{clk_p}.

Modulator	
Parameters	**Configuration**
Reserved	REG0
Processing clock f_{clk_tx}	Modulator processing clock. Also serves as DAC sampling clock. Expressed as as $f_{clk\_tx} = f_{clk\_p} * M / (D * O)$) where D is an integer divider in the range 1 - 106 M is a multiplier in the range 2.0 to 64.0 by steps of 1.0. Fixed point format 7.3 O is a divider in the range 2.0 to 128.0 by steps of 1.0. Fixed point format 7.3 Note: the graphical use interface computes the best values for M, D and O. f_{clk_tx} recommended range 80-160 MHz. REG1(6:0) = D REG2 = M(7:0) REG3(1:0) = M(9:8) REG4 = O(7:0) REG5(2:0) = O(10:8)
Symbol rate $f_{symbol\ rate\ tx}$	The modulator symbol rate is in the form $f_{symbol\ rate\ tx} = f_{clk\_tx} / 2^n$ where n ranges from 2 (4 samples per symbol) to 15 (symbol rate = f_{clk_tx} / 32768). n is defined in REG6(3:0)
Output center frequency (f_c)	The modulated signal center frequency can be shifted in frequency 32-bit signed integer (2's complement representation) expressed as $f_c * 2^{32} / f_{clk\_tx}$ REG10 (LSB) – REG7 (MSB)
Digital Signal gain	16-bit amplitude scaling factor for the modulated signal. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Please check for saturation (see test points) when changing either the symbol rate or the signal gain. REG19 = LSB REG20 = MSB
Additive White Gaussian Noise gain	16-bit amplitude scaling factor for additive white Gaussian noise. Because of the potential for saturation, please check for saturation (see test points) when changing this parameter. REG21 = LSB REG22 = MSB
Modulation type	0 = BPSK 1 = QPSK REG23(5:0)
Spectrum inversion	Invert Q bit. This is helpful in compensating any frequency spectrum inversion occurring in a subsequent RF frequency translation. 0 = off 1 = on REG23(6)
Reserved	REG23(7) = '0'
Input selection	0 = from UDP port 1024 1 = internal pseudo-random test sequence. 100ms repetition 2 = internal pseudo-random test sequence continuous transmission 3 = unmodulated test mode (carrier only) REG24(1:0)
Reserved	REG24(7:2) = "000001"
FEC encoding	K=9 rate ½ convolutional code with zero tail bits. 1 = enabled

	0 = bypassed REG25(0)

External transmitter gain control	When using an external transceiver such as the COM-350x family, the transmitter gain can be controlled through the TX_GAIN_CNTRL1 analog output signal. Range 0 – 3.3V. REG26: LSB, REG27(3:0): MSb
TX_ENB control	The TX_ENB signal at the interface controls the RF transmit circuit. During normal operations, the transmitter and ancillary circuits (RF LO) are muted outside of a transmit burst. REG27(4) = 0 However, during tests, the transmitter can be forced to stay ON at all times, for example when the AWGN is generated within. REG27(4) = 1
Transmit payload size	TX_PAYLOAD_SIZE Encoded frame size in symbols, as seen by the modulator. Payload only, does not include preamble or sync word. Must equal (ENC_FRAME_IN_SIZE * 2 + 16) when BPSK and FEC rate ½ encoding, or (ENC_FRAME_IN_SIZE + 8) when QPSK and FEC rate ½ encoding Constraint: TX_PAYLOAD_SIZE+preamble+sync word must be less than 8191 symbols. REG28 = LSB REG29(4:0) MSB
Encoder input frame size	ENC_FRAME_IN_SIZE Frame size in bits before encoding. Must be consistent with the modulator payload field size (see above). REG30 = LSB REG31(5:0) MSB

Demodulator	
Parameters	**Configuration**
Nominal symbol rate $f_{symbol\_rate\_rx}$	32-bit integer expressed as $f_{symbol\_rate\_rx} * 2^{32} / f_{clk\_adc}$. The maximum practical symbol rate is f_{clk_adc} / 4. The maximum allowed error between transmitted and received symbol rate is +/- 100ppm. REG35 (LSB) – REG38 (MSB)
Nominal input center frequency (f_{c_rx})	The nominal center frequency is a fixed frequency offset applied to the input samples. It is used for fine frequency corrections, for example to correct clock drifts. 32-bit signed integer (2's complement representation) expressed as $f_{c\_rx} * 2^{32} / f_{clk\_adc}$ In addition to this fixed value, an optional time-dependent frequency profile can be entered. See frequency profile table. REG39 (LSB) – REG42 (MSB)
Modulation type	0 = BPSK 1 = QPSK REG43(5:0)
Spectrum inversion	Invert Q bit. This is helpful in compensating any frequency spectrum inversion occurring during RF frequency translations. 0 = off 1 = on REG43(6)
FEC decoding enabled	K=9 rate ½ Viterbi decoding '1' enabled, '0' bypassed REG45(0)
AGC1 response time	Users can to optimize AGC1 response time while avoiding instabilities (depends on external factors such as gain signal filtering at the RF front-end and symbol rate). The response time is approximately: 0 = 8 symbols, 1 = 16 symbols, 2 = 32 symbols, 3 = 64 symbols, etc…. 10 = every thousand symbols. Note: a x4 faster AGC is used during the packet preamble. Valid range 0 to 14. REG46(4:0)

Demod input selection	0 = baseband input (I/Q complex samples) 1 = IF input (I as real input, Q is ignored) 7 = internal loopback REG46(7:5)
Receiver payload size	RX_PAYLOAD_SIZE Encoded frame size in symbols, as seen by the demodulator. Payload only, does not include preamble or sync word. Must equal (DEC_FRAME_OUT_SIZE * 2 + 16) when BPSK, or (DEC_FRAME_OUT_SIZE + 8) when QPSK Minimum size: (58.6 us + 256/nominal symbol rate) Relevant transmitter constraint: TX_PAYLOAD_SIZE+preamble+sync word must be less than 8191 symbols. REG47 = LSB REG48(4:0) MSB
Decoder output frame size	DEC_FRAME_OUT_SIZE Frame size in bits after decoding. Must be consistent with the modulator payload field size (see above). REG49 = LSB REG50(5:0) MSB

Network Interface	
Parameters	**Configuration**
LAN MAC address LSB	REG70. To ensure uniqueness of MAC address. The MAC address most significant bytes are tied to the FPGA DNA ID. However, since Xilinx cannot guarantee the DNA ID uniqueness, this register can be set at the time of manufacturing to ensure uniqueness.
Static IP address	4-byte IPv4 address. Example : 0x AC 10 01 80 designates address 172.16.1.128 REG71: MSB REG72 REG73 REG74: LSB
Subnet mask	REG75 (MSB) – REG78(LSB)
Gateway IP address	REG79 (MSB) – REG82(LSB)
Destination IP address	4-byte IPv4 address Destination IP address for UDP frames with decoded data. REG83 (MSB) – REG86(LSB)
Destination ports	I-channel data is routed to this user-defined port number: REG87(LSB) – REG88(MSB) Q-channel data is routed to the incremented port number.

(Re-)Writing to control register REG99 is recommended after a configuration change to enact the change (Note: this is done automatically when using the graphical user interface).

Status Registers

Parameters	Monitoring
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-9 Properly operating hardware will result in the following sequence being displayed: 01 F1 1D xx 1F 93 10 00 22 07.
FEC decoder input BER measurement	The burst-mode FEC decoder computes the input BER prior to decoding. Mesasured in a frame. This method works with any bit sequence. SREG11 (LSB) - SREG13 (MSB)
BER tester synchronized	SREG14(0): 1 when the BERT is synchronized with the received PRBS-11 test sequence.
Bit error rate	Monitors the BER (number of bit errors over 10,000 received bytes) when the modulator is sending a PRBS-11 test sequence. SREG15 (LSB) – 17 (MSB)
Number of transmitted frames	SREG18 (LSB) – 20 (MSB)
Number of received frames	SREG21 (LSB) – 23 (MSB)
MAC address	Unique 48-bit hardware address (802.3). In the form SREG35:SREG36:SREG37:…:SREG40
Preamble + sync field length	Length in symbols for the current active FPGA configuration SREG24 (LSB) – SREG25 (MSB)

ComScope Monitoring

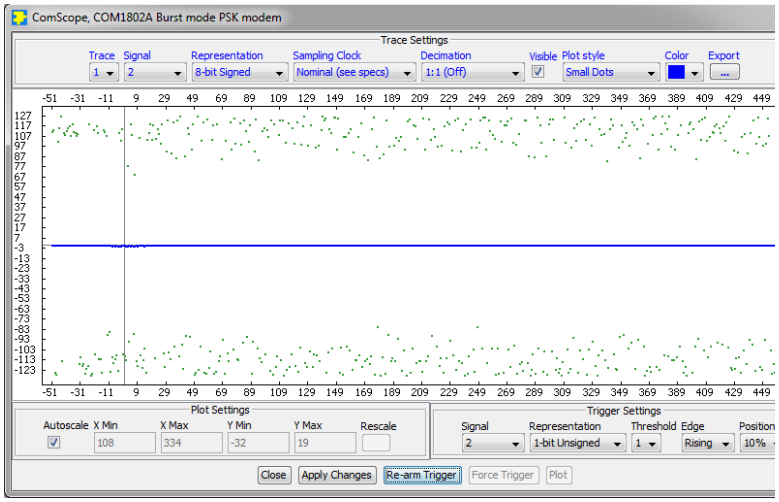
Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-1802 signal traces and trigger are defined as follows:

Trace 1 signals (demod)	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: I-channel samples, directly from ADC (after IF undersampling or baseband). Real-time.	8-bit signed	ADC clock f_{clk_adc}	512
2: Demodulated Q-channel at optimum sampling instant. (after elastic input buffer: use T2 trigger)	8-bit signed	1 samples / symbol	512
3: FFT magnitude	8-bit unsigned	ADC clock f_{clk_adc}	512
Trace 2 signals (demod)	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: I-channel input at near-zero center frequency	8-bit signed	ADC clock f_{clk_adc}	512
2: Reconstructed carrier phase (coarse)	8-bit unsigned	ADC clock f_{clk_adc}	512
Trace 3 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Demodulated I-channel at optimum sampling instant. (after elastic input buffer: use T2 trigger)	8-bit signed	1 samples / symbol	512
2: Cumulative symbol timing error	8-bit signed	symbol rate	512
3: Reconstructed carrier phase (fine)	8-bit unsigned	ADC clock f_{clk_adc}	512
Trigger Signal	**Format**		
1: transmit burst boundaries	1-bit		
2: end of first sync word in rx burst	1-bit		

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk} processing clock as real-time sampling clock.

In particular, selecting the f_{clk} processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope Window Sample: showing BPSK demodulated bits (green = I channel, blue = Q channel). Trigger on start of payload field.

Digital Test Points

Test points are routed to the J4(left) connector.

Demodulator Test Points	
J4/A1	Transmit burst boundaries (0 = idle)
J4/A2	Modulator saturation
J4/A3	Signal presence detected in receiver (FFT)
J4/A4	Sync word detected in receiver (matched filter)
J4/A5	Rx: payload data field
J4/A6	Rx: sync field
J4/A7	Rx: demodulated I data
J4/A8	Rx: recovered symbol center
J4/A9	Rx: recovered carrier frequency
J4/A10	Rx: saturation in rx path
J4/A11	Rx: missed data field (presence detected but never entered demod state4
J4/A12	Rx: demod state 0 (idle)
J4/A13	Rx: demod state 1 (searching for sync word)
J4/A14	Rx: demod state 2 (demodulating payload field)
J4/A15	Rx: demod state 5 (performing FFT frequency acquisition)
J4/A16	Rx: first frame in burst
J4/A17	FEC decoder bit error
J4/A18	BER tester synchronized
J4/A19	BER tester: matched filter detection of PRBS11 test sequence
J4/A20	BER tester: byte error
Other test points	
TP1/DONE	‘1’ indicates proper FPGA configuration.

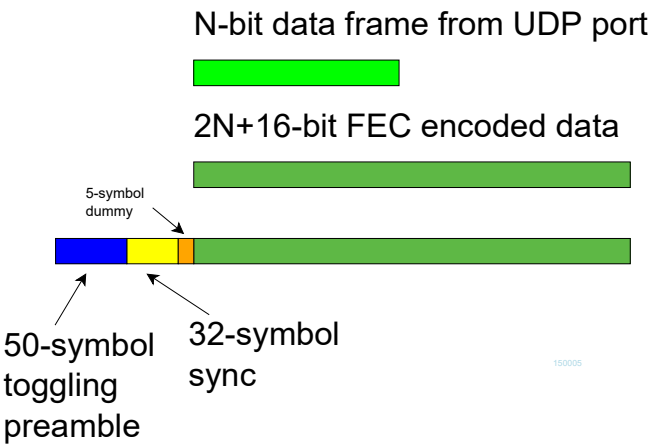
Operation

Burst format

The modulator input receives fixed-length data frames over LAN/UDP. The size, ENC_FRAME_IN_SIZE is user-defined but should remain fixed during operation.

Upon UDP reception, the data frame is immediately encoded with a convolutional code K=9, rate ½, resulting in an encoded frame of length 2*ENC_FRAME_IN_SIZE+16 bits (including the 16 tail bits).

The encoded frame is then encapsulated into a PSK frame comprising a short (50 symbols typically) preamble, a 32-symbol synchronization field and a 5-symbol dummy field.



When transmitting multiple frames, follow-on frames are appended without preamble, separated only with a 32-bit sync word + 5 symbol dummy field.

Transmission timing

A data frame received over UDP is transmitted without delay. The transmission time uncertainty is small (< TBD us). The user application is therefore fully in control of the burst scheduling, for example to prevent collisions in a multi-node radio network.

When the modulator is configured in PRBS11 test mode, the PRBS11 pseudo-random test sequence is generated internally, packetized in a fixed-length frame and transmitted one frame every 100 ms. The UDP input is ignored while in this test mode.

Input elastic buffer

When longer data is needed, multiple data frames can be queued for transmission in an input elastic buffer. The modulator expects any follow-on frame to be entirely within the input elastic buffer before the previous frame transmission is complete (so as to avoid transmitting another preamble). In this case, the modulator only inserts a 37-bit synchronization word between payload frames.

The input elastic buffer size is 8Kbit

Minimum burst duration

To guarantee receiver detection, the burst duration, including preamble and sync word must be greater than
(58.6 us + 256/nominal symbol rate),

For example, at 20 Msymbols/s, the minimum burst duration is 71.4 us.

Spacing between successive receive bursts (no a priori time-of-arrival information)

At high symbol rates, and when there is no a priori information about the time of arrival of bursts, there must be a minimum separation in time between successive bursts. The minimum time between the starts of two successive bursts is a complex function of the symbol rate and payload length:

65us + (256/symbol rate) +
4*(burst payload symbols+(symbol rate * 117.2us))/ f_{clk_adc}

Example1:
22 Msymbols/s, 2048-symbol burst: 192.3us min separation between starts of successive bursts.
In this case, the bursts are 96.8us long.

At lower symbol rates, this constraint does not apply because the minimum separation is less than the burst duration. For example:
5 Msymbols/s, 2048-symbol burst: 182.1us min separation between starts of successive bursts.
However, the bursts are always longer (426 us), so this constraint is practically void.

Spacing between successive receive bursts (with a priori time-of-arrival information)

Shorter constraint. TBD

Symbol Rate

The receiver is capable of handling any symbol rate up to the specified 39.5 Msymbols/s.

The modulator implementation imposes a coarser granularity in the selected symbol rate. The modulator symbol rate steps are uneven but always within 0.2% of the target value. See the constraints when computing the modulator processing clock f_{clk_tx} (page 5)

The GUI calculates the precise modulation symbol rate based on the user's requirement. Please be sure to set the nominal demodulation symbol rate accordingly.

Threshold Eb/No

TBD

Frequency acquisition window

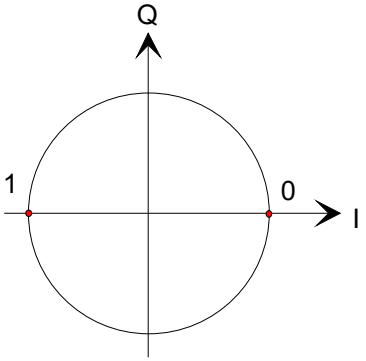
TBC +/- 20% of symbol rate

Constellation: Symbol Mapping

The packing of serial data stream into symbols is done with the Most Significant bit first.

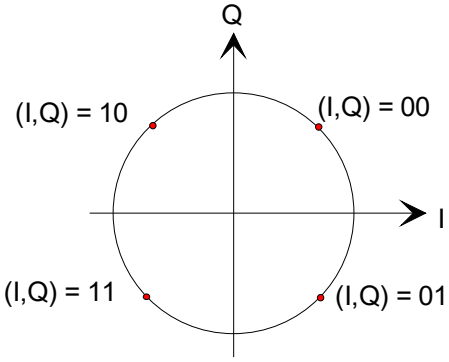
BPSK

REG23(5:0) = 0



QPSK

REG23(5:0) = 1
Gray encoding.



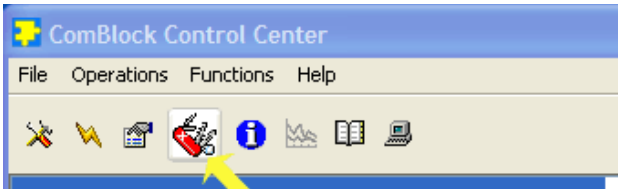
Format Conversion

Serial to parallel conversion occurs when converting the demodulated data stream into 8-bit byte over the UDP-IP link. The general rule is that the first received bit is placed at the MSb position in the byte.

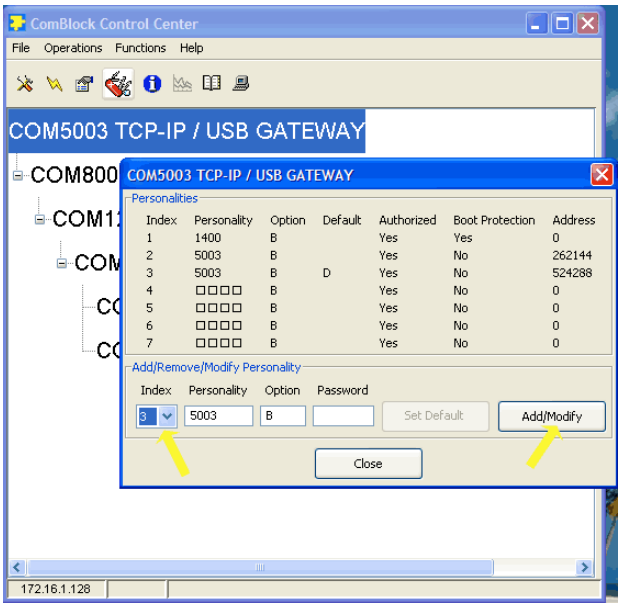
Load Software Updates

From time to time, ComBlock software updates are released.

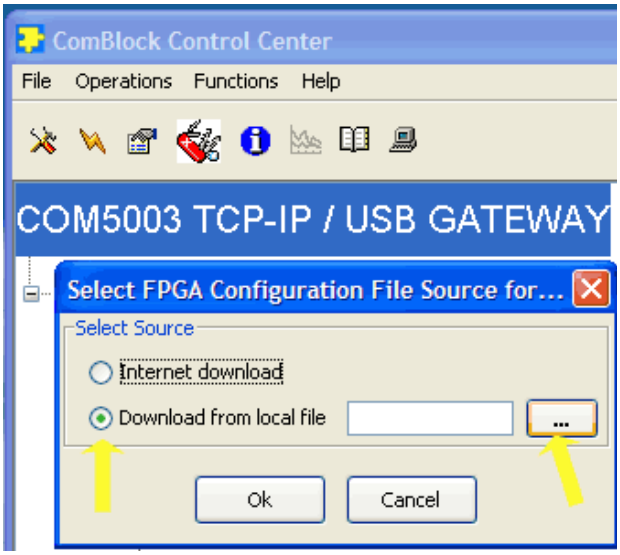
To manually update the software, highlight the ComBlock and click on the Swiss army knife button.



The receiver can store multiple personalities. The list of personalities stored within the ComBlock Flash memory will be shown upon clicking on the Swiss army knife button.



The default personality loaded at power up or after a reboot is identified by a ‘D’ in the Default column. Any unprotected personality can be updated while the Default personality is running. Select the personality index and click on the “Add/Modify” button.



The software configuration files are named with the .bit extension. The bit file can be downloaded via the Internet, from the ComBlock CD or any other local file.

The option and revision for the software currently running within the FPGA are listed at the bottom of the advanced settings window.

Two firmware options are available for this receiver:
-A firmware uses an internal VCTCXO frequency reference.
-B firmware option requires an external 10 MHz frequency reference.

Recovery

This module is protected against corruption by an invalid FPGA configuration file (during firmware upgrade for example) or an invalid user configuration. To recover from such occurrence, connect a jumper in J3 and during power-up. This prevents the FPGA configuration and restore USB communication [LAN communication is restored only if the IP address is known/defined for the personality index selected as default]. Once this is done, the user can safely re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center.

Electrical Interface

Other Digital Modem Interfaces	Definition
USB 2.0	Mini-USB connector, type AB. This interface is used exclusively for monitoring and control. It does not support payload data.
LAN / UDP-IP	10/100/1000 Mbits/s Ethernet LAN. RJ-45 connector.

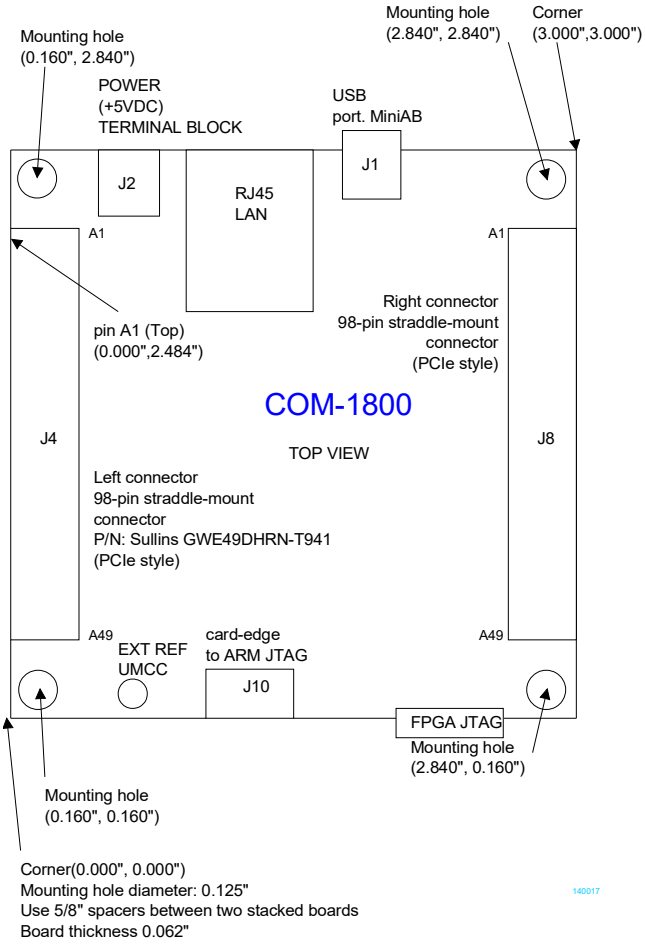
Operating input voltage range

Supply voltage	+4.5V min, +18V max 450 mA under 5V typ.

Absolute Maximum Ratings

Supply voltage	-0.5V min, +20V max
98-pin connector inputs	-0.5V min, +3.6V max

Mechanical Interface



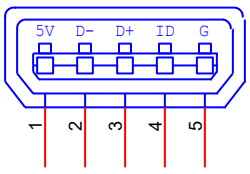
Schematics

The board schematics are available on-line at
http://comblock.com/download/com_1800schematics.pdf

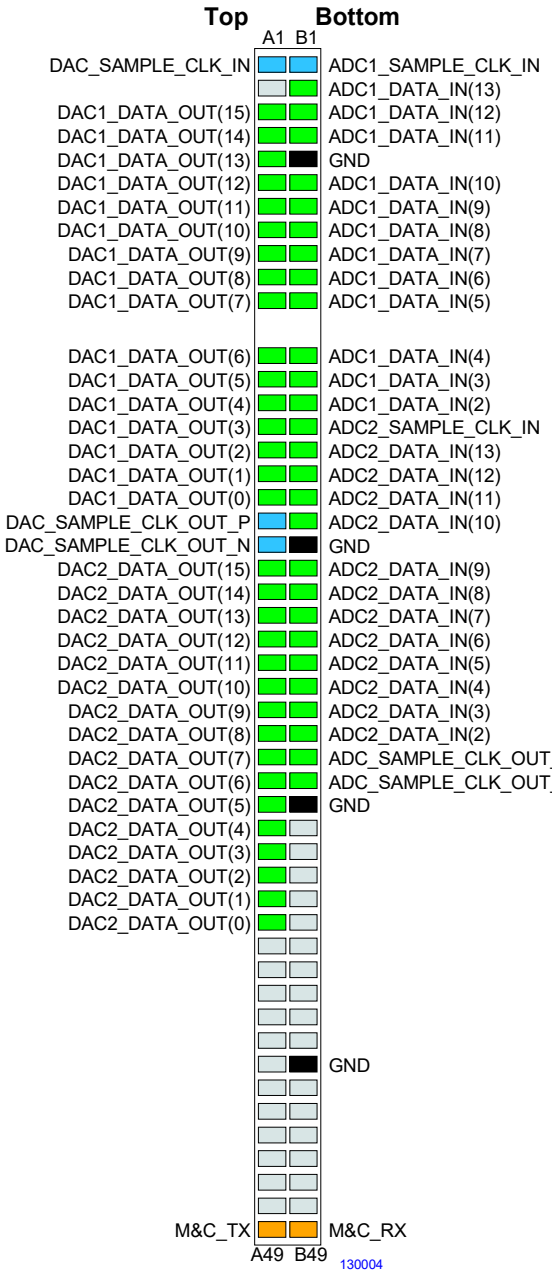
Pinout

USB

Both USB ports are equipped with mini type AB connectors. (G = GND). In both cases, the COM-1802 acts as a USB device.



Right Connector J9



2*16-bit output samples, 2*12-bit input samples. This interface is compatible with the COM-3504 dual Analog<->Digital Conversions.

I/O Compatibility List

(not an exhaustive list)

Right connector (J9)
COM-3504 Dual Analog <-> Digital Conversions 2*16-bit 250 MSamples/s

Configuration Management

This specification is to be used in conjunction with VHDL software revision 1 and ComBlock control center revision 3.11c and above.

It is possible to read back the option and version of the FPGA configuration currently active. Using the ComBlock Control Center, highlight the COM-1802 module, then go to the advanced settings. The option and version are listed at the bottom of the configuration panel.

ComBlock Ordering Information

COM-1802
PSK burst modem, 40 Msymbols/s

MSS • 845 Quince Orchard Boulevard Ste N•
Gaithersburg, Maryland 20878-1676 • U.S.A.
Telephone: (240) 631-1111
Facsimile: (240) 631-1676
E-mail: sales@comblock.com