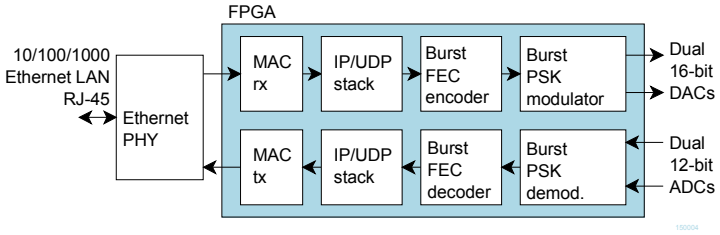
COM-1802SOFT PSK burst modem
VHDL source code overview / IP core

Overview

The COM-1802SOFT is a burst-mode PSK modem, written in generic VHDL.



The entire **VHDL source code** is deliverable. It is portable to a variety of FPGA targets.

Key features and performance:

- Digital modem with flexible configuration:
  - Variable data rates up to $f_{clk}/4$
  - Selectable payload field length up to 8000 symbols/frame. A burst can comprise one or multiple frames.
  - Usable as continuous mode, random access burst mode, or time-division multiple access (TDMA)
  - Includes burst-mode convolutional or turbo-code error correction
  - Modulation: BPSK, QPSK
  - Coherent demodulation for operation at low SNR
  - Modulator and demodulator are independently configured.
- Modem data I/Os:
  - 10/100/1000 Ethernet LAN/UDP
-
- Performance:
  - Frequency acquisition range: +/- 20% of symbol rate with no apriori knowledge.
  - ±50ppm symbol timing tracking
  - Acquisition threshold < 2dB Eb/No
  - Near theoretical BER vs Eb/No
- Provided with IP core:
  - Complete VHDL source code, including burst modem, burst FEC codec [4][5], IP/UDP stack [2] and gigabit Ethernet MAC [3].
  - Matlab .m file for generating stimulus files for VHDL simulation of the demodulator for end-to-end BER performance analysis at various signal to noise ratios
  - VHDL testbenches (back-to-back modem or stimulus file input)
  - PRBS11 test sequence generator, AWGN noise generator, BER tester

Target Hardware

The code is written in generic standard VHDL and is thus portable to a variety of FPGAs. The code was developed and tested on a Xilinx 7-series FPGA but is expected to work similarly on other targets.

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Configuration

Synthesis-time configuration parameters

The following constants are user-defined in the component's generic section prior to synthesis. These parameters generally define the size of the embodiment.

SIMULATION	'1' during simulation, 0 for release
COM1802_TX.vhd modulator	
FIRST_PREAMBLE_EXTENSION	Depending on the hardware AGC speed, a preamble may be needed to improve the sync word detection. Expressed as a number of symbols. Depends on the receiver AGC design and on the modulation symbol rate. Valid range 0 to max. Typical value: 50 symbols. Composite limit: preamble+sync+ BURST_LENGTH < 8191
SYNC_LENGTH	Sync word length, expressed in number of symbols. Typical value: 32 for a 2048 symbol frame (1.5% overhead) Composite limit: preamble+sync+ BURST_LENGTH < 8191
SYNC_WORD	Sync pattern. LEFT-aligned when SYNC_LENGTH is less than the maximum 128 bits. Typical sync word: 0x5A0FBE66 MSb is sent first.
GAP_LENGTH	Optional gap between sync word and payload field Expressed in number of symbols Justification: demodulator may need a short time to correct phase/amplitude/etc after detecting the sync word. Typical value: 12 symbols. In the case of multi-frame bursts, the gap is inserted only once, after the first sync word.
AWGN_EN	Instantiate (1)/do not instantiate (0) a built-in AWGN noise generator

COM1802_RX.vhd demodulator	
CLK_FREQUENCY	CLK frequency in MHz
FIRST_PREAMBLE_EXTENSION	Same settings as modulator
SYNC_LENGTH	Same settings as modulator
SYNC_WORD	Same settings as modulator
GAP_LENGTH	Same settings as modulator
BER_EN	Instantiate (1)/do not instantiate (0) a built-in Bit Error Rate tester. Default: 0 (disabled), as the BER is better measured using the other BER tester located after FEC decoding.

Convolutional FEC codec:

ENCODER_GMR_3G.vhd FEC encoder
see [4]
VITERBI_DECODER_GMR_3G.vhd FEC decoder
see [4]

Turbo code FEC codec:

TC_ENCODER_DVB_RCS2.vhd FEC encoder
see [5]
TC_DECODER_DVB_RCS2.vhd FEC decoder
see [5]

Run-time configuration parameters

The user can set and modify the following controls at run-time through the top level component interface:

COM1802_TX.vhd modulator	
SYMBOL_RATE _NDIV	Symbol rate expressed as (modulator processing clock)/2^NDIV Range 0 to 15 for division ratios ranging from 1 to 32768
MOD_GAIN	Modulated signal amplitude scaling factor. 16-bit unsigned
NOISE_GAIN	Noise amplitude scaling factor. 18-bit signed
CENTER_FREQ	Modulated signal center frequency. Expressed as f_c/modulator processing clock * 2^32
BURST_LENGTH	Payload data field length in a burst or frame. Expressed in number of symbols. Constraint: BURST_LENGTH* NBITSPERSYMBOLS is a multiple of 8 bits. composite limit: preamble+sync+ BURST_LENGTH < 8191
CONTROL	bits 5:0 modulation 0 = BPSK 1 = QPSK bit 6: spectrum inversion. invert Q. on (1) or off (0) bit 7: output spectrum shaping filter (square root raised cosine) bypass (1) or enable (0) bits 9:8 test mode: 00 no test, 01 = PRBS11 burst, 10 = PRBS11 continuous, 11 = unmodulated carrier bit 10: always '1' to enable sync word insertion
TX_WINDOW	Start of burst transmission is only allowed if TX_WINDOW = '1' Usage: 1 CLK-wide pulse to trigger one frame transmission, solid '1' for continuous transmission

COM1802_RX.vhd demodulator	
AGC_RESPONSE	Adjust the AGC response time. approximately log2(NSymbols).
RECEIVER_ CENTER_FREQ	Nominal (i.e. expected) center frequency. Expressed as f_c/demodulator processing clock * 2^32 This frequency is subtracted from the input signal center frequency.
NOMINAL_ SYMBOL_RATE	$f_{symbol\ rate}$ / f_{clk} * 2^32
PAYLOAD_SIZE	Payload data field length in a burst or frame. Expressed in number of symbols. Note: from the demodulator's perspective, the "payload" includes FEC-encoded bits, but not the preamble, sync word or gap symbols.
DEMOD_ CONTROL	bits 5:0 modulation 0 = BPSK 1 = QPSK bit 6: spectrum inversion. invert Q. on (1) or off (0) bit 10: output format, must be 1 for 4-bit soft quantization

Convolutional FEC codec:

ENCODER_GMR_3G.vhd FEC encoder
see [4]
VITERBI_DECODER_GMR_3G.vhd FEC decoder
see [4]

Turbo code FEC codec:

TC_ENCODER_DVB_RCS2.vhd FEC encoder
see [5]
TC_DECODER_DVB_RCS2.vhd FEC decoder
see [5]

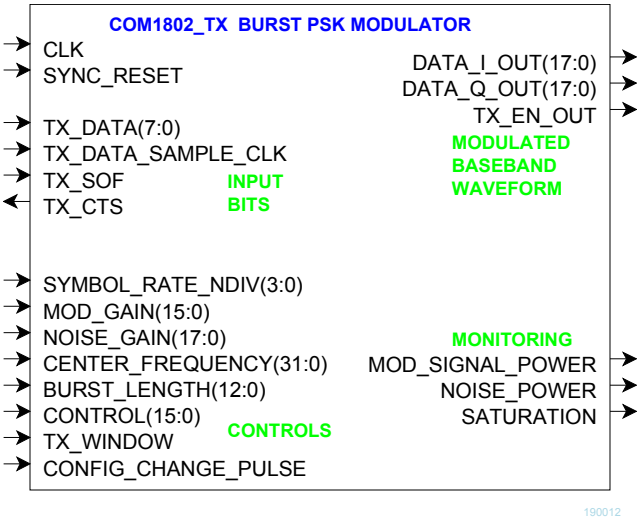
I/Os

General

CLK: input
DAC clock. The user must provide this global clock (use BUFG). The CLK timing period must be constrained in the .xdc file associated with the project.

SYNC_RESET: input
Synchronous reset. The reset MUST be exercised at least once to initialize the internal variables. It must be exercised whenever a control parameter is changed.

Modulator

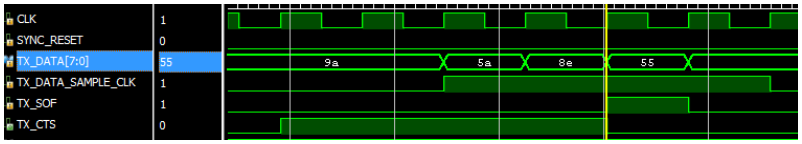


TX_DATA(7:0): Input data byte. The MSb is sent first.

TX_DATA_SAMPLE_CLK: input.
1 CLK-wide pulse indicating that TX_DATA is valid.

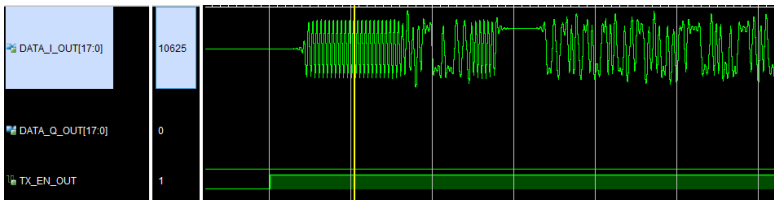
TX_SOF: optional input Start Of Frame. 1 CLK-wide pulse.
The SOF is aligned with **TX_DATA_SAMPLE_CLK**.

TX_CTS: output.
Clear-To-Send flow control. '1' indicates that the modulator is ready to accept another input byte. Thanks to an input elastic buffer, the data source is allowed to send a few more bytes after TX_CTS goes low.



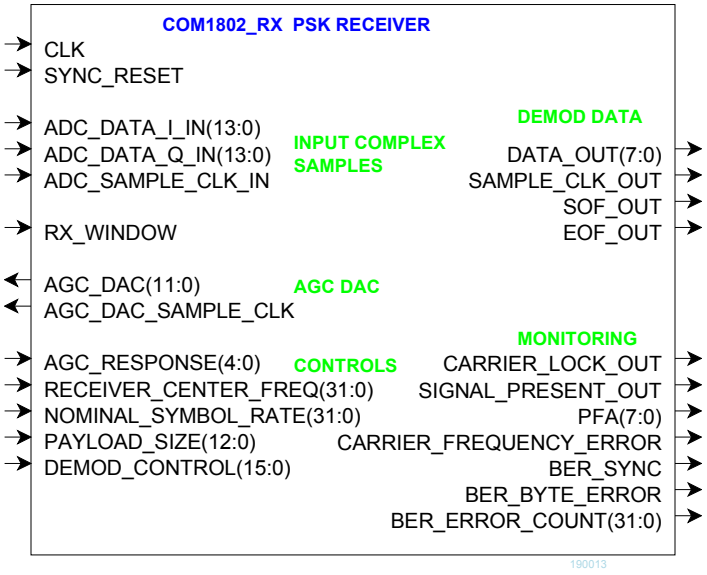
Modulator input flow control example

DATA_I/Q_OUT(17:0): Modulated baseband output samples (I = in-phase, Q = quadrature). One output sample every clock. Format: 2's complement (signed)



TX_EN_OUT: goes low to turn off an external power amplifier when the modulator is not receiving any input data.

Receiver



ADC_DATA_I/Q_IN(13:0): input samples from one or two external ADCs. (one in the case of IF undersampling, two for near-zero frequency complex inputs). If the ADCs have fewer than 14-bit precision, align the most significant bit with ADC_DATA_IN(13). Format: 2's complement (signed).

RX_WINDOW: expected burst receive window. Mostly serves to identify missed bursts.

AGC_DAC(11:0): output to an external DAC to control an external AGC. Read when **AGC_DAC_SAMPLE_CLK** is '1'

DATA_OUT(7:0): demodulated data bit, 4-bit soft-quantized. The demodulated bit is bit 3. The three lower bits indicate the level of confidence: "0000" for a solid '0', "1111" for a solid '1', "1000" for a '1' barely above the threshold.
An alternative format is also available whereby 8 demodulated bits are packed into DATA_OUT, MSb first.
Read when **SAMPLE_CLK_OUT** = '1'.
Start-Of-Frame and End-Of-Frame are marked by 1-CLK pulses **SOF_OUT** and **EOF_OUT** respectively.

SIGNAL_PRESENT_OUT is the first detection stage of incoming bursts, performed by the FFT, together with the coarse center frequency estimate.

PFA(7:0): number of false alarms in a 100ms window. The demodulator includes an adaptive threshold for detecting the presence of incoming bursts. The algorithm takes typically 10 seconds after power up to converge. When tracking, the algorithm will aim at 1 false alarm per 100ms as the probability of false alarm

The built-in BER tester measures the bit error rate of the demodulated data stream prior to error correction when the transmitted sequence is a raw (non-FEC encoded) PRBS-11 test sequence. The **BER_ERROR_COUNT** is meaningful only when **BER_SYNC** = '1'

The **CARRIER_LOCK_OUT** is rarely useful.

Operation

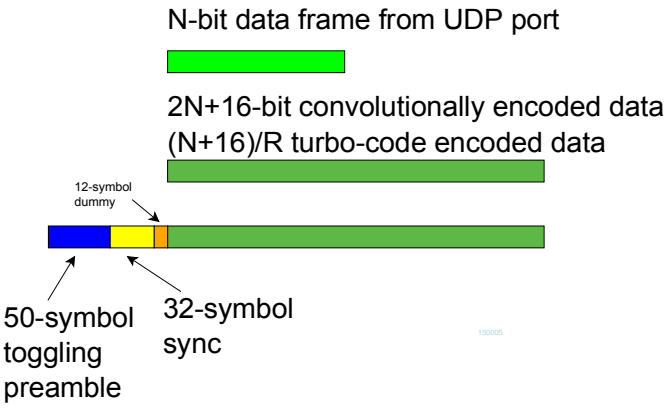
Burst format

The modulator input receives fixed-length data frames over LAN/UDP. The size, ENC_FRAME_IN_SIZE is user-defined but should remain fixed during operation.

Upon UDP reception, the data frame is immediately encoded with a convolutional code K=9, rate ½, resulting in an encoded frame of length 2*ENC_FRAME_IN_SIZE+16 bits (including the 16 tail bits).

Alternatively, the data frame can be turbo-code encoded at rates ranging from 1/3 to 7/8.

The encoded frame is then encapsulated into a PSK frame comprising a short (50 symbols typically) preamble, a 32-symbol synchronization field and a 12-symbol dummy field.



When transmitting multiple frames, follow-on frames are appended without preamble, separated only with a 32-bit sync word + 12 symbol dummy field.

The default sync word is 0x5A0FBE66. It can be changed in the code.

These parameters are defined in *COM1802_TOP.vhd*

```
constant FIRST_PREAMBLE_EXTENSION: integer range 0 to 8191 := 50;  -- better if < PAYLOAD_SIZE
constant SYNC_LENGTH: integer range 0 to 128 := 32;
constant SYNC_WORD: std_logic_vector(127 downto 0) := x"5A0FBE66000000000000000000000000";
constant GAP_LENGTH: integer := 12; -- same for mod/demod
```

Transmission timing

A data frame received over UDP is transmitted without delay. When using Gigabit Ethernet LAN, the transmission time uncertainty is small (a few us). The user application is therefore fully in control of the burst scheduling, for example to prevent collisions in a multi-node radio network.

When the modulator is configured in PRBS11 test mode, the PRBS11 pseudo-random test sequence is generated internally, packetized in a fixed-length frame and transmitted one frame every 100 ms. The UDP input is ignored while in this test mode.

Input elastic buffer

When longer data is needed, multiple data frames can be queued for transmission in an input elastic buffer. The modulator expects any follow-on frame to be entirely within the input elastic buffer before the previous frame transmission is complete (so as to avoid transmitting another preamble). In this case, the modulator only inserts a 44-symbol synchronization word plus gap between payload frames.

The input elastic buffer size is 16Kbit

Minimum burst duration

To guarantee receiver detection, the burst duration, including preamble and sync word must be greater than (58.6 us + 256/nominal symbol rate in MSymbols/s),

For example, at 20 MSymbols/s, the minimum burst duration is 71.4 us.

Spacing between successive receive bursts (no a priori time-of-arrival information)

At high symbol rates, and when there is no a priori information about the time of arrival of bursts, there must be a minimum separation in time between successive bursts. The minimum time between the starts of two successive bursts is a complex function of the symbol rate and payload length:

65us + (256/symbol rate) +
4*(burst payload symbols+(symbol rate * 117.2us))/ f_{CLK_ADC}

Example1:
22 Msymbols/s, 2048-symbol burst: 192.3us min separation between starts of successive bursts.
In this case, the bursts are 96.8us long.

At lower symbol rates, this constraint does not apply because the minimum separation is less than the burst duration. For example:
5 Msymbols/s, 2048-symbol burst: 182.1us min separation between starts of successive bursts.
However, the bursts are always longer (426 us), so this constraint is practically void.

Symbol Rates

The receiver is capable of handling any symbol rate up to the specified f_{CLK_ADC} /4 Msymbols/s where f_{CLK_ADC} is the fixed-frequency ADC sampling clock. The expected symbol rate is specified with fine 32-bit precision.

On the modulator side, one must generate a DAC sampling clock CLK_TXg with a sampling frequency $\mathbf{f_{clk\_tx}}$ related to the symbol rate: $\mathbf{f_{clk\_tx}}$ = symbol_rate * 2^NDIV, where NDIV is an integer.

On Xilinx 7-series FPGAs, the DAC sampling frequency steps are uneven but always within 1% of the target value. The constraints when computing the DAC sampling rate $\mathbf{f_{clk\_tx}}$ are listed below:

$\mathbf{f_{clk\_tx}}$	DAC sampling frequency. Expressed as $\mathbf{f_{clk\_tx}}$ = $\mathbf{f_{clk\_p}}$ * M / (D * O)) where $\mathbf{f_{clk\_p}}$ is a frequency reference (in the baseline code, this is the digital signal processing clock) D is an integer divider in the range 1 - 106 M is a multiplier in the range 2.0 to 64.0 by steps of 1.0. Fixed point format 7.3 O is a divider in the range 2.0 to 128.0 by steps of 1.0. Fixed point format 7.3 Note: the graphical use interface computes the best values for M, D and O. $\mathbf{f_{clk\_tx}}$ recommended range 80-160 MHz (on Artix-7 –1 speed grade) REG1(6:0) = D REG2 = M(7:0)

	REG3(1:0) = M(9:8) REG4 = O(7:0) REG5(2:0) = O(10:8)

The GUI calculates the precise modulation symbol rate based on the user's requirement. Please be sure to set the nominal demodulation symbol rate accordingly.

PSK modulation rolloff

A square-Root Raised Cosine filter is filtering the transmit signal to reduce the out-of-band energy.
Likewise, the same filter type is applied to the received signal to reject out-of-band noise.
By default, the RRC filter rollof factor is 20%.
FIRRCOS20_40TAPS.vhd component is the tx RRC filter.
RAISED_COS5A.vhd is the rx RRC filter

Error correction

Two error correction schemes are available:

- Burst-mode convolutional code and Viterbi decoding. The default configuration is K=9, rate 1/2 but other constraint lengths and punctured rates are also user-configurable. The detailed specifications are in reference document [4].
- Turbo-code codec. The detailed specifications are in reference document [5].

The COM-1802SOFT package is ready to use with the convolutional code K=9 rate = ½ by default.

The COM-1902SOFT package (included) is ready to use with both convolutional code K=9 rate = 1/2 and the turbo-code encoder and decoder.

When changing the FEC codec and/or the coding rate R, the frame length parameters must be changed as well. The rules and constraints are defined below:

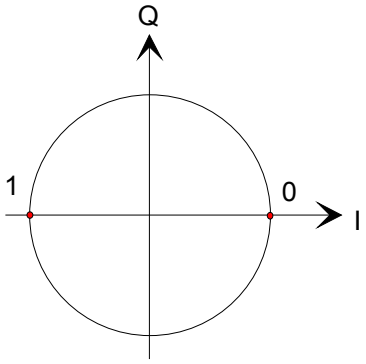
Transmit payload size	TX_PAYLOAD_SIZE Encoded frame size in modulation symbols, as seen by the PSK modulator. Must be consistent with the FEC code and modulation selections. This includes payload data and tail bits (Convolutional FEC) or CRC16 (turbo code FEC) but does not include preamble, sync word, or dummy bits. Must equal (ENC_FRAME_IN_SIZE/R + 16) when BPSK and convolutional FEC rate R encoding, or (ENC_FRAME_IN_SIZE/R + 16)/2 when QPSK and convolutional FEC rate R encoding, or (ENC_FRAME_IN_SIZE + 16)/R when BPSK and turbo code FEC rate R encoding, or (ENC_FRAME_IN_SIZE + 16)/2R when QPSK and turbo code FEC rate R encoding Constraint #1: Minimum burst size (including preamble, sync word) for best signal presence detection at the first frame: (58.6 us + 256/nominal symbol rate)
Encoder input frame size	ENC_FRAME_IN_SIZE Frame size in bits before FEC encoding. Must be consistent with the modulator payload field size (see above).

	Constraint #2: when using convolutional code, the uncoded frame size is limited to 8191 bits. When using turbo code, the preferred frame sizes are 12,61 and 248 Bytes (96,488,1984 bits). Constraint #3: when using turbo code, the frame size is limited to 253 Bytes (2024 bits) Constraint #4: when using turbo code rates 2/3,3/4,5/6,6/7, ENC_FRAME_IN_SIZE must be in the form rate 2/3 case: (ENC_FRAME_IN_SIZE+16)/2 is multiple of 2 rate 3/4 case: (ENC_FRAME_IN_SIZE+16)/2 is multiple of 6 rate 4/5 case: (ENC_FRAME_IN_SIZE+16)/2 is multiple of 4 rate 5/6 case: (ENC_FRAME_IN_SIZE+16)/2 is multiple of 20 rate 6/7 case: (ENC_FRAME_IN_SIZE+16)/2 is multiple of 12 rate 7/8 case: (ENC_FRAME_IN_SIZE+16)/2 is multiple of 28
Receiver payload size	RX_PAYLOAD_SIZE Encoded frame size in modulation symbols, as seen by the PSK demodulator. This includes payload data and tail bits (Convolutional FEC) or CRC16 (turbo code FEC) but does not include preamble, sync word, or dummy bits. Must equal (DEC_FRAME_IN_SIZE/R + 16) when BPSK and convolutional FEC rate R encoding, or (DEC_FRAME_IN_SIZE/R + 16)/2 when QPSK and convolutional FEC rate R encoding, or (DEC_FRAME_IN_SIZE + 16)/R when BPSK and turbo code FEC rate R encoding, or (DEC_FRAME_IN_SIZE + 16)/2R when QPSK and turbo code FEC rate R encoding Constraint #1: Minimum burst size (including preamble, sync word) for best signal presence detection at the first frame: (58.6 us + 256/nominal symbol rate)
Decoder output frame size	DEC_FRAME_OUT_SIZE Frame size in bits after decoding. Must be consistent with the modulator payload field size (see above). Constraint #2: when using convolutional code, the decoded frame size is limited to 8191 bits. When using turbo code, the preferred frame sizes are 12,61 and 248 Bytes (96,488,1984 bits). Constraint #3: when using turbo code, the frame size is limited to 253 Bytes (2024 bits) Constraint #4: when using turbo code rates 2/3,3/4,5/6,6/7, ENC_FRAME_IN_SIZE must be in the form rate 2/3 case: (DEC_FRAME_OUT_SIZE +16)/2 is multiple of 2 rate 3/4 case: (DEC_FRAME_OUT_SIZE +16)/2 is multiple of 6 rate 4/5 case: (DEC_FRAME_OUT_SIZE +16)/2 is multiple of 4 rate 5/6 case: (DEC_FRAME_OUT_SIZE +16)/2 is multiple of 20 rate 6/7 case: (DEC_FRAME_OUT_SIZE +16)/2 is multiple of 12 rate 7/8 case: (DEC_FRAME_OUT_SIZE +16)/2 is multiple of 28

Constellation: Symbol Mapping

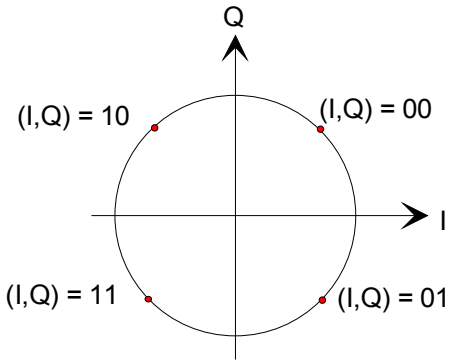
The packing of serial data stream into symbols is done with the Most Significant bit first.

BPSK



QPSK

Gray encoding.



Format Conversion

Serial to parallel conversion occurs when converting the demodulated data stream into 8-bit byte over the UDP-IP link. The general rule is that the first received bit is placed at the MSb position in the byte.

Performance

Threshold Eb/No

When configured for BPSK, turbo code rate 1/3, 1984 bits/frame, the frame error rate (FER) is as follows:
3.8 dB E_b/N_o, FER = 2%.
5.8 dB E_b/N_o, FER = 2.10^{-3}

Frequency acquisition window

The frequency acquisition window is +/- 20% of symbol rate with no apriori knowledge.

Once locked, the carrier tracking loops tracks the carrier phase over a very wide frequency range.

Software Licensing

This software is supplied under the following key licensing terms:

1. A nonexclusive, nontransferable license to use the VHDL source code internally, and
2. An unlimited, royalty-free, nonexclusive transferable license to make and use products incorporating the licensed materials, solely in bit stream format, on a worldwide basis.

The complete VHDL/IP Software License Agreement can be downloaded from http://www.comblock.com/download/softwarelicense.pdf

Portability

The VHDL source code is written in generic VHDL and thus can be ported FPGAs from various vendors. See the limitation below.

Limitation

1. The modulator requires a processing and DAC clock in the form (symbol rate * 2^N), where N is an integer in the range 2-15. The COM1802SOFT includes a Xilinx primitive to program the clock frequency, allowing any target symbol rate with a precision of 1% or better. This Xilinx primitive is restricted to the Xilinx 7-series FPGAs (Artix, Kintex, Virtex, Zynq). For other target platforms, the user is responsible for generating the processing/DAC clock.

Configuration Management

The current software revision is 004s.

Directory	Contents
/doc	Specifications, user manual, implementation documents
/src	.vhd source code,.pkg packages, .xdc constraint files (Xilinx) One component per file.
/sim	VHDL test benches
/matlab	Matlab .m file for generating stimulus files for VHDL simulation and for end-to-end BER performance analysis at various signal to noise ratios
/bin	.bit configuration files (for use with ComBlock COM-1800 FPGA development platform)

Project files:

Xilinx ISE 14 project file: com-1802.xise
Xilinx Vivado v2017.4 project file: project_vivado20174.xpr

VHDL development environment

The VHDL software was developed using the following development environment:

(a) Xilinx ISE 14.7 for synthesis, place and route
(b) Xilinx Vivado 2017.4 for synthesis, place and route and VHDL simulation

The entire project fits easily within a Xilinx Artix7-100T. Therefore, the ISE project can be processed using the free Xilinx WebPack tools.

Device Utilization Summary

COM1802_TX.vhd Modulator only no FEC, no AWGN, no LAN/UDP		% of Xilinx Artix7-100T
Registers	5863	4.7%
LUTs	3713	5.9%
36Kb block RAM/FIFO	6	4.5%
DSP48	6	2.5%
GCLKs	1	3.2%
Modulator + FEC encoder + LAN/UDP + AWGN generator		% of Xilinx Artix7-100T
Registers	12278	9.7%
LUTs	8910	14.1%
36Kb block RAM/FIFO	20	14.8%
DSP48	9	3.8%
GCLKs	8	25%
COM1802_RX.vhd Demodulator only no FEC, no BER tester, no LAN/UDP		% of Xilinx Artix7-100T
Registers	8999	7.1%
LUTs	8894	14.1%
36Kb block RAM/FIFO	37.5	27.8%
DSP48	45	18.8%
GCLKs	1	3.2%
Receiver + demodulator + FEC decoder + LAN/UDP + BER tester		% of Xilinx Artix7-100T
Registers	23258	18.4%
LUTs	24546	38.8%
36Kb block RAM/FIFO	60	44.4%
DSP48	42	17.5%
GCLKs	6	18.8%
Modulator + Receiver + demodulator + FEC decoder + LAN/UDP No AWGN generator No BER tester		% of Xilinx Artix7-100T
Registers	29899	23.6%
LUTs	28497	45%
36Kb block RAM/FIFO	67.5	50%
DSP48	48	20%
GCLKs	8	25%

Clock and modulation rate

The design uses three different clocks, all locked onto either a 10 MHz or a 19.2 MHz external frequency reference, as selected by the **OPTION** generic parameter. Other frequency references can also be used by changing the *CLK_GEN_MMCM_ADJ.vhd* multiply, divide and period parameters.

CLK_ADCg: *Fixed*-frequency analog-to-digital converter sampling clock. Drives the external ADCs. Determines the *maximum* receive PSK symbol rate = $f_{CLK\_ADC}/4$.

CLK_TXg: Dynamically programmable DAC sampling clock. Used for fine control of the transmit symbol rate. Drives the external DACs. In order to get the cleanest output spectrum with low out-of-band energy, CLK_TXg should be chosen to be in the form symbol_rate * 2^N, where N is an integer (this alleviates the need for re-sampling). In a Xilinx 7 series implementation, the MMCM can always generate CLK_TXg within 1% of the target clock frequency. Values for the integers M,D and O are defined through control registers:

```
D => CLK_TX_GEN_D,  -- range 1 - 106
M => CLK_TX_GEN_M,   -- range 2.0 - 64.0 in increment steps of 0.125 fixed point format 7.3
O => CLK_TX_GEN_O,   -- range 2.0 to 128.0 in increment steps of 0.125 fixed point format 8.3
```

CLK_P: fixed-frequency processing clock used for gigabit Ethernet interface, FEC encoder, and FEC decoder. There is no advantage in increasing this clock frequency beyond 125 MHz. Set to 120 MHz in the VHDL code.

Typical maximum clock frequencies for various FPGA families are listed below:

Device family	CLK_ADCg	CLK_TXg	CLK_P
Xilinx Kintex 7 -2	250 - 300 MHz	250 - 300 MHz	125 MHz
Xilinx Artix 7 Spartan-1	160 MHz	160 MHz	125 MHz

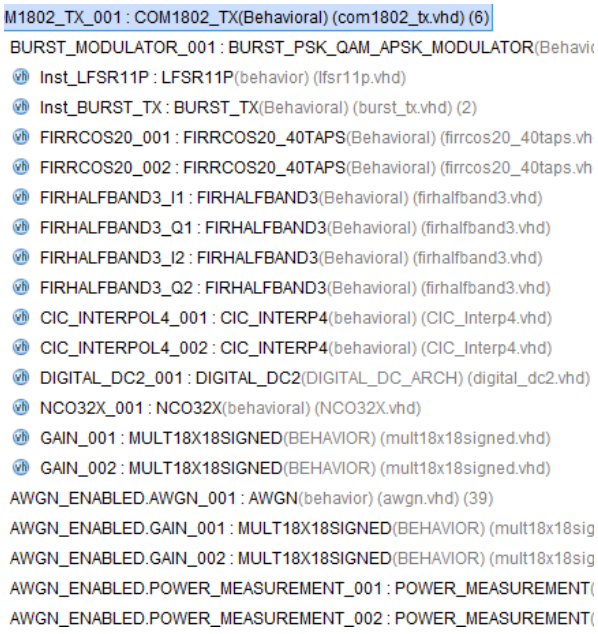
Ready-to-use Hardware

The COM-1802SOFT was developed on, and therefore ready to use on the following commercial off-the-shelf hardware platform:

FPGA development platform
COM-1800 FPGA Artix7-100T + GbE + DDR3 socket + ARM development platform
COM-1902 L/S-band transceiver
Analog peripherals
COM-3504 Dual Analog <-> Digital Conversions
COM-3506 [400 MHz – 3GHz] RF transceiver

VHDL components overview

Modulator



COM1802_TX.vhd generates a complex baseband PSK-modulated waveform from byte-size input data.

BURST_PSK_QAM_APSK_MODULATOR.vhd implements the digital modulation and spectrum shaping. Key controls include modulation symbol rate and output signal amplitude. In this application, only BPSK and QPSK modulation are supported, although the framework allows for fairly simple upgrades to higher-order modulations.

The *BURST_TX.vhd* component stores input data in an elastic input buffer, then packs input bits into symbols (1 or 2 bits/symbol) at the specified symbol rate.

BRAM_DP2.vhd is a generic dual-port memory, used as input and output elastic buffers. Memory is inferred (no Xilinx primitive is used).

FIRCOS20_40TAPS.vhd implements a root raised cosine filter with 20% rolloff to shape the output spectrum. It is implemented as an FIR filter with 40 coefficients. I/O sampling rate is 2 samples/symbol (meaning that the maximum modulation rate could be up to f_{CLK_TXg} /2, although the demod may not be able to match this higher rate)

FIRHALFBAND3.vhd implements a half-band FIR filter used to interpolate by 2. In includes 20-taps, nearly half of them are zero. 60 dB rejection. For lower symbol rates, two half-band filters are concatenated for a x4 interpolation to 8 samples/symbol.

The last interpolation of the modulated waveform is performed by *CIC_INTERPOL4.vhd*. up to the DAC sampling rate f_{CLK_TXg}.The interpolation factor CIC_R must be a power of 2.

Small adjustments in the transmitted signal center frequency are implemented by *DIGITAL_DC2.vhd* as a vector rotation. The sine and cosine values are read from ROM in *SIGNED_SIN_COS_TBL2.vhd*. The translation frequency/phase rotation is generated by *NCO32X.vhd*.

Prior to the DAC, the digital waveform amplitude is adjusted by digital multiplers *MULT18X18SIGNED.vhd*.

Ancillary components

LFSR11P.vhd is a pseudo-random binary sequence sequence generator used for test purposes. The PRBS11 sequence is recognized by the *BER2.vhd* bit error rate tester component as well as most BER testers at the receiving end to measure the link quality. Disabled during normal operation.

AWGN.vhd implements the optional Additive White Gaussian noise by generating precise complex (I,Q) independent random samples once every CLK_TXg.
The noise bandwidth is thus $\mathbf{f_{CLK\_TXg}}$. Instantiation is controlled by the generic flag **AWGN_EN** .

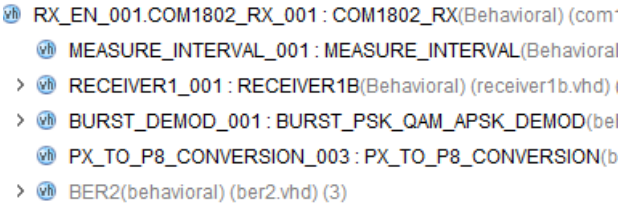
POWER_MEASUREMENT.vhd measures the complex waveform power.

INFILE2SIM.vhd reads a tab-delimited input text file. This component is used by the testbench to read a modulated waveform samples file generated by the `siggen1802.m` Matlab program for various Eb/No and frequency offset cases.

SIM2OUTFILE.vhd writes three 12-bit data variables to a tab delimited file which can be subsequently read by Matlab (load command) for plotting or analysis.

Receiver

The receiver COM1802_RX.vhd comprises three high-level components:



RECEIVER1.vhd is the front-end digital receiver which processes digital samples from the A/D converter(s). It performs non modulation-specific tasks, including fixed frequency translation to (near-zero) baseband, AGC, variable decimation (CIC) filters and one half-band filter for image rejection. Input digital samples can be complex (in the case of baseband input samples) or real (in the case of IF undersampling). This generic component is not modulation-specific.

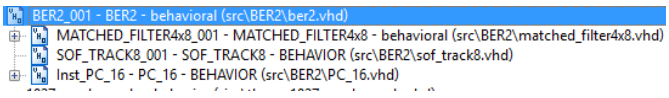
BURST_PSK_QAM_APSK_DEMOD.vhd performs the demodulation, including carrier tracking, symbol timing tracking and AGC. It is currently limited to BPSK/QPSK demodulation.

BER2.vhd is a bit error rate tester expecting to receive a PRBS11 test sequence. It synchronizes with the received bit stream and count errors over a 80,000 bit window.

AGC21.vhd is specifically designed for the fast convergence required by burst demodulation: sharp gain adjustment when a burst comes in, slow decay until the next burst.

Two instances of frequency translation *DIGITAL_DC3.vhd* are used. The first removes the expected center frequency. The second is controlled by the carrier tracking loop to remove the unknown residual phase error. *DIGITAL_DC3.vhd* implements a complex vector rotation. The sine and cosine values are read from ROM in *SIGNED_SIN_COS_TBL3.vhd*.

SIGNED_SIN_COS_TBL3.vhd stores sine and cosine functions in ROM.



Error Correction

ENCODER_GMR_3G.vhd is the convolutional encoder. It supports tail-biting and zero-tail insertion mechanisms. The data source sends a complete frame, as delineated by the SOF_IN and EOF_IN flags. Once a complete input frame is received, the encoder will generate a complete encoded output frame. Thus, the encoding latency is one input frame duration.

VITERBI_DECODER_GMR_3G.vhd is the Viterbi decoder top component in this hierarchical design. It includes state machines to control tail-biting and insertion of zero tail when applicable.

See [4] and [5] for component details.

Networking

COM5402.vhd implements the Internet Protocol stack: IP, UDP, TCP server, PING, ARP, etc, for 10/100/1000 Mbps Ethernet LAN.

COM5401.vhd implements the 10/100/1000 Mbps Ethernet MAC. It interfaces with an external GbE PHY integrated circuit.

See [2] and [3] for component details.

Ancillary components

COM1802_TOP.vhd: is mostly a use example when the PSK modem is implemented on a ComBlock COM-1800 FPGA development platform. Configuration is performed through CREG() control registers (see [1a] and [1b] for details on the control registers definitions)

VHDL simulation

/src/com1802_top.vhd can serve as the top level for VHDL simulation of an end-to-end link, including noise, Doppler and bit error rate measurement. It includes all functions (modem, error correction). To start, configure the top component as follows:

1. In the generic section, instantiate all components by setting
   TX_EN: std_logic := '1';
   AWGN_EN: std_logic := '1';
   RX_EN: std_logic := '1';
   BER_EN: std_logic := '1';
   SIMULATION: std_logic := '1'

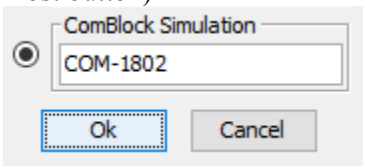
2. In the UC_WRITE_001y process, configure the control registers as defined in the "Control registers" section of reference document [1a]

```
-- initialize control registers for simulation
UC_WRITE_001y: if (SIMULATION = '1') generate
    -- initialize the control registers during simulation
    CREG(1) <= x"01";    -- modulator clock CLK_TXg D
    CREG(2) <= x"28";       -- M format 7.3
    CREG(3) <= x"00";
    CREG(4) <= x"28";       -- O format 8.3
    CREG(5) <= x"00";
```

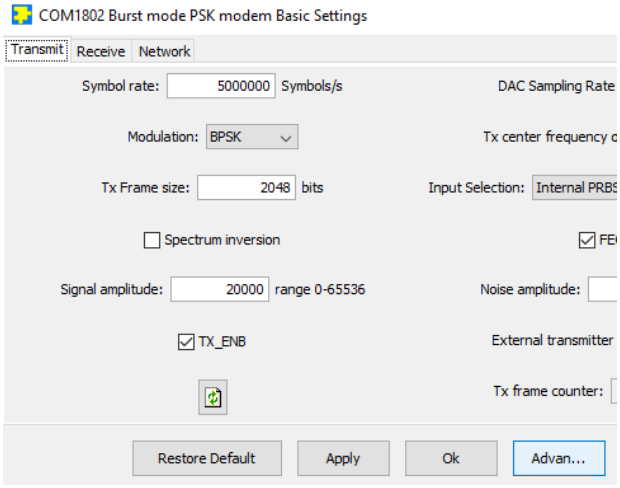
Current code configuration:
Modulator clock CLK_TXg D 160 MHz
Transmit symbol rate 20 MSymbols/s
Modulator amplitude gain: 20000
Noise amplitude gain: 0
BPSK, burst sent periodically
Encoder input frame size: 2048 bits
FEC encoder enabled
TX_PAYLOAD_SIZE in bits: 2048*2 (encoded) +16 (FEC tail)
Nominal demod symbol rate: 20 Msymbols/s
Nominal input center frequency: 0 Hz
FEC decoder enabled
AGC response time: 6
Loopback mode
RX_PAYLOAD_SIZE in symbols: 2048*2+16
Decoder output frame size in bits: 2048

The TX_WINDOW_p pulses trigger each burst transmission. The pulse is ignored if there is no sufficient data to fill a frame. Multiple frames can be packed into a single burst when data is available in a timely manner. See the TX_WINDOW_GEN_SIM process.

Helpful trick: computing the control registers can be tedious. The ComBlock Control Center does compute all control registers through a graphical user interface. To do so, open the ComBlock Control Center, enable the simulation mode (left-most button)



and open the settings panel (3rd button from left)



Once configuration is complete, click on the "Advanced" button to display all control register values.

The **/sim/tbcom1802_demodonly.vhd** testbench reads a tab-delimited stimulus files of modulated I/Q baseband complex sampled waveforms, performs demodulation and measure the BER.
The associated matlab program /matlab/siggen1802.m generates such a waveform file with the properly formatted burst.

Matlab simulation

Matlab programs are located in the /matlab directory.

The /matlab/siggen1802.m program generates a stimulus file input.txt for use as input to the demodulator VHDL simulation tbcom1802_demodonly.vhd. The stimulus file includes a continuous stream of pseudo-random (PRBS11) data bits, segmentation into frames, burst formatting, PSK modulation, additive white Gaussian noise, channel filtering, frequency translation and quantization.

Care must be taken to match the modulator configuration in `siggen1802.m` and the demodulator configuration in `tbcom1802_demodonly.vhd`.

This setup allows end-to-end BER testing, as the demodulator `com1802_rx.vhd` includes a built-in bit error rate tester.

Reference documents

[1a] COM-1802 specifications. Includes the definitions for all programmable control registers (pages 5-).
https://comblock.com/download/com1802.pdf

[1b] COM-1902 specifications. Includes the definitions for all programmable control registers (pages 6-).
https://comblock.com/download/com1902.pdf

[2] COM-5402SOFT IP/TCP/UDP/ARP/PING STACK for GbE, VHDL source code overview / IP core.
https://comblock.com/download/com5402soft.pdf

[3] COM-5401SOFT, Tri-Mode 10/100/1000 Ethernet MAC, VHDL source code overview / IP core
https://comblock.com/download/com5401soft.pdf

[4] COM-1510SOFT Block mode convolutional FEC codec, VHDL source code overview / IP core.
https://comblock.com/download/com1510soft.pdf

[5] COM-7003SOFT Turbo-code FEC codec, VHDL source code overview / IP core.
https://comblock.com/download/com7003soft.pdf

Acronyms

Acronym	Definition
ACS	Add Compare Select circuit in Viterbi decoder
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BRAM	Block RAM
CCSDS	Consultative Committee For Space Data Systems
CTS	Clear-To-Send, flow control signal
DAC	Digital to Analog Converter
GUI	Graphical User Interface (ComBlock Control Center)
FEC	Forward Error Correction
LSb	Least Significant bit
MSb	Most Significant bit
PRBS-11	Pseudo-Random Binary Sequence, 2047-bit period
RTS	Ready-To-Send
RRC	(Square) Root Raised Cosine filter

ComBlock Ordering Information

COM-1802SOFT PSK burst modem,
VHDL source code / IP core

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