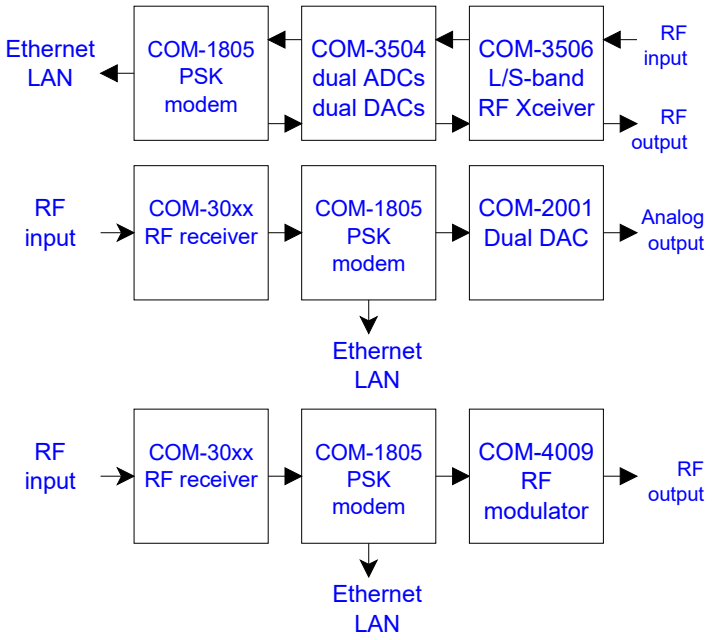
COM-1805 PSK MODEM

Key Features

- Continuous-mode modem for BPSK/QPSK/OQPSK modulation. Programmable symbol rate, up to 40 MSymbols/s
- Convolutional or Turbo-code FEC error correction. V.34 scrambling.
- Frequency reference: internal TCXO or input for an external, higher-stability 10 MHz frequency reference.
- TCP server for modulator data input and demodulator output. UDP server for demodulator output.
- Demodulator performance:
  - BER: < 0.5 dB implementation losses w.r.t. theory
  - Programmable frequency acquisition range.
  - Demodulator acquisition threshold (uncoded) Eb/No = 1dB
- Overall performance: 2.10^{-5} BER @ 4dB Eb/No for K=7 rate ½ FEC.
- Frequency acquisition range > +/- 12% of symbol rate. Tracking symbol rates over +/- 50ppm around nominal setting.
- Built-in tools: PRBS-11 pseudo-random test sequence, BER tester, AWGN generator, internal loopback mode, carrier frequency error measurement.
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Connectorized 3”x 3.5” module for ease of prototyping. Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.

Typical assemblies



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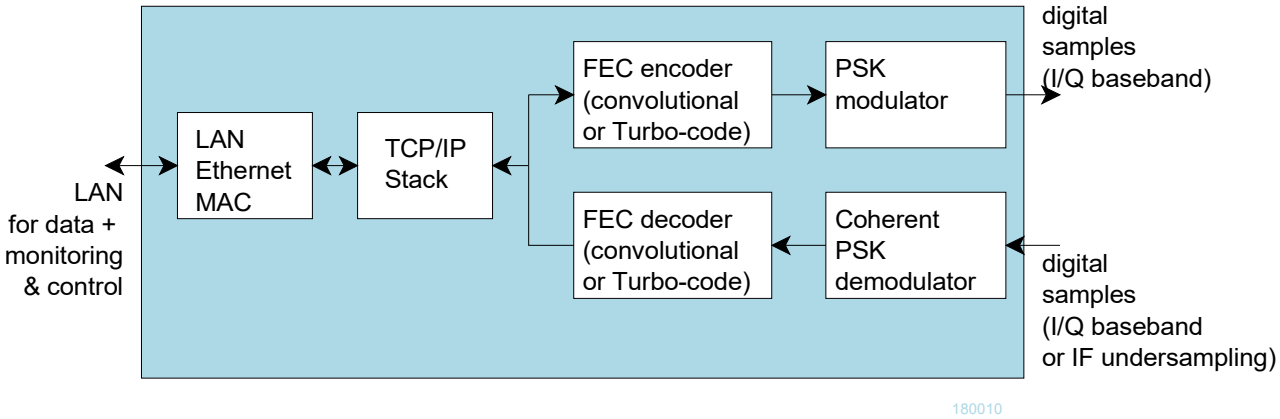
 Issued 1/6/2023

Block Diagram



Overall block diagram

Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

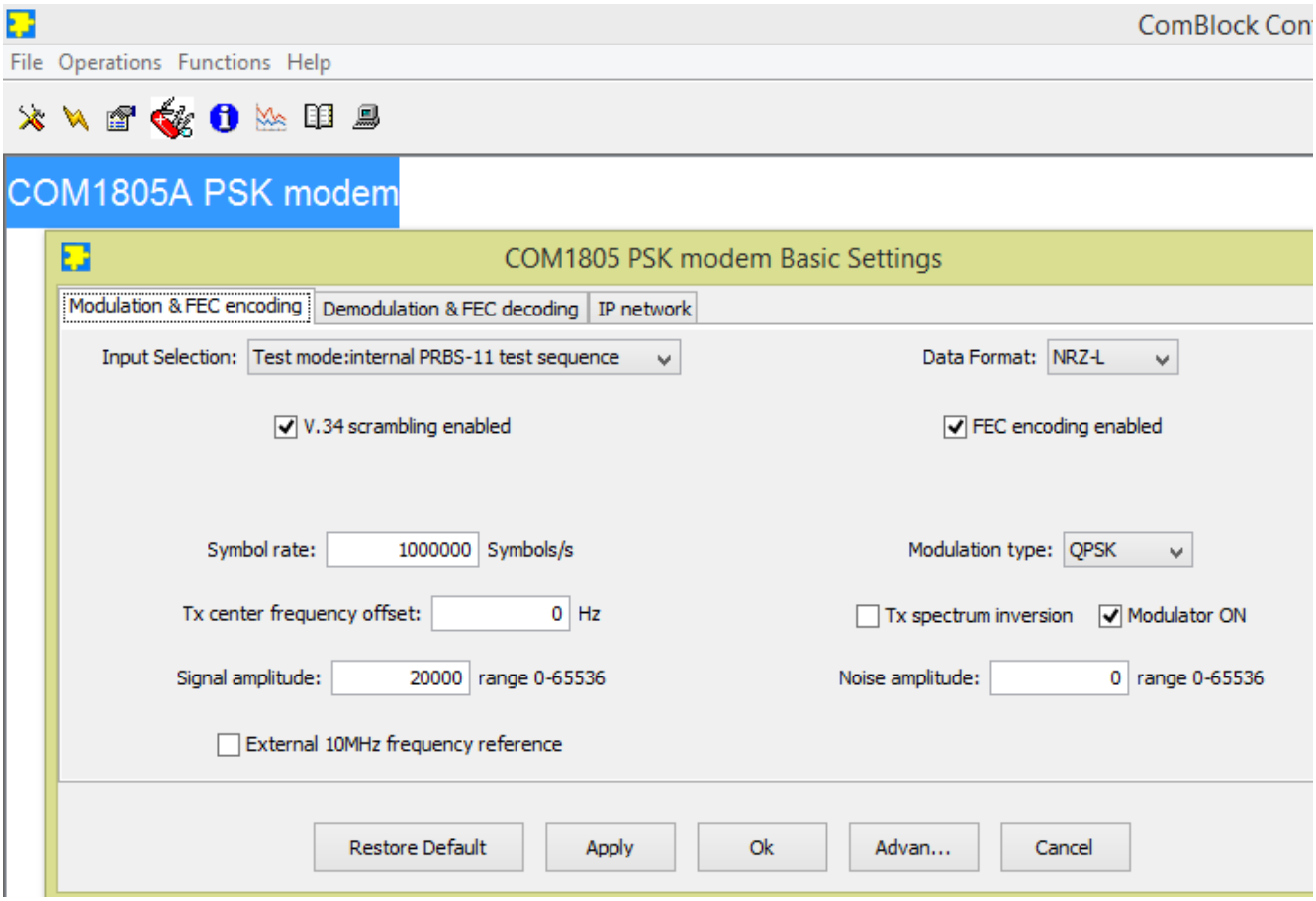
- USB, TCP-IP/LAN

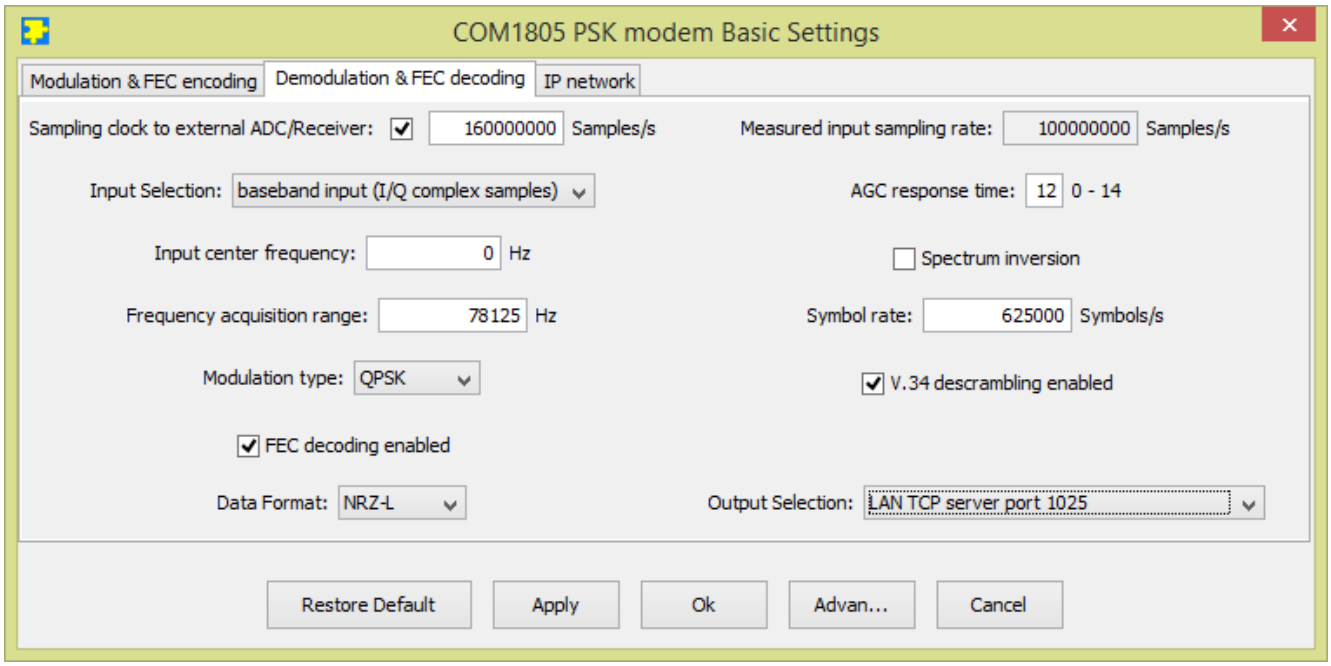
or connections via adjacent ComBlocks

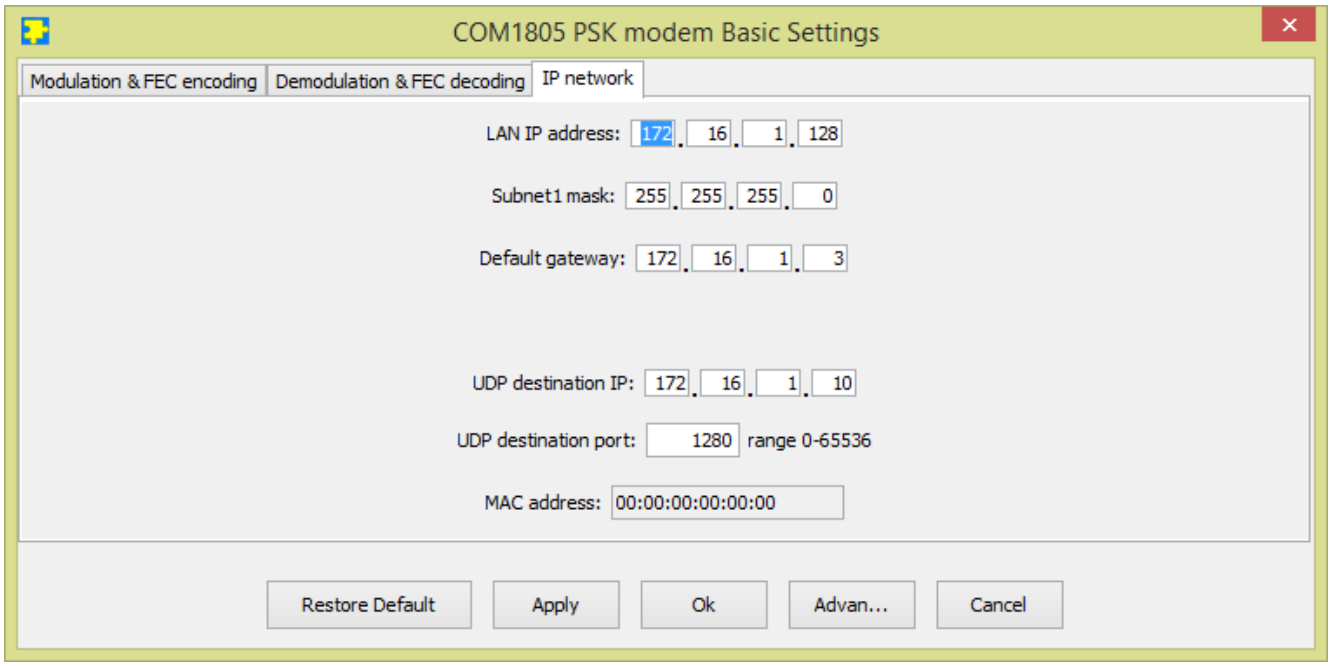
The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1805 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1805 module to be configured, next click the *Settings* button to display the *Settings* window shown below.







Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write. Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

Several key parameters are computed on the basis of the receive sampling clock f_{clk_rx} and transmit sampling clock f_{clk_tx} or the 125 MHz internal processing clock f_{clk_p}.

General	
Parameters	**Configuration**
Internal/External frequency reference	0 = internal TCXO as frequency reference. 1 = external. Use the 10 MHz clock externally supplied through the J7 SMA connector as frequency reference. REG0(7)

Modulator	
Parameters	**Configuration**
Input selection	1 = LAN TCP port 1024 3 = internal pseudo-random test sequence 4 = zero input 5 = serial data bit + bit clock, left connector 6 = clock synchronous serial input (serial data bit, enable, Clear-To-Send input flow control, synchronous clock), left connector 7 = unmodulated test mode* (carrier only) 8 = bypass modem: rx input samples sent to tx output samples after AGC and frequency translation. (*) to prevent the unmodulated output from output DC block, select a non-zero output center frequency. REG0(3:0)
Data formatting	0 = NRZ-L 1 = NRZ-M 2 = NRZ-S REG0(6:4)
V.34 scrambling	0 = disabled 1 = enabled REG45(1)
Transmit sampling clock frequency f_{clk_tx}	Modulator processing clock. Also serves as DAC sampling clock. Expressed as as f_{clk_tx} = 160 MHz * M / (D * O)) where D is an integer divider in the range 1 - 106 M is a multiplier in the range 2.0 to 64.0 by steps of 1.0. Fixed point format 7.3 O is a divider in the range 2.0 to 128.0 by steps of 1.0. Fixed point format 7.3 Note: the graphical use interface computes the best values for M, D and O. f_{clk_tx} recommended range 80-160 MHz. REG1(6:0) = D REG2 = M(7:0) REG3(1:0) = M(9:8) REG4 = O(7:0) REG5(2:0) = O(10:8)
Symbol rate f_{symbol_rate}	The modulator symbol rate is in the form $f_{symbol\ rate\ tx} = f_{clk\_tx} / 2^n$ where n ranges from 1 (2 samples per symbol) to 15 (symbol rate = f_{clk_tx} / 32768). n is defined in REG5(7:4)
Modulation type	Modulation type 0 = BPSK 1 = QPSK 2 = OQPSK REG6(5:0)
Insert periodic sync marker (NEW)	Helpful in removing phase ambiguity at the demodulator. Required for Turbo code decoder frame synchronization. 0 = off 1 = on REG6(7)
Spectrum inversion	Invert Q bit 0 = off 1 = on REG7(6)
Root raised cosine filter rolloff	1 = 20%, 4 = 35%, 7 = 50% REG7(2:0)

Turn output on/off	Controls the external RF modulator through the TX_ENB pin. The TX_ENB control signal to the RF modulator will also be turned off when there is no input data to transmit. 0 = off 1 = on REG7(7)
Digital Signal gain	16-bit amplitude scaling factor for the modulated signal. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Please check for saturation (see test points) when changing either the symbol rate or the signal gain. REG10 (LSB) – REG11 (MSB)
Additive White Gaussian Noise gain	16-bit amplitude scaling factor for additive white Gaussian noise. Because of the potential for saturation, please check for saturation (see test points) when changing this parameter. REG12 (LSB) – REG13 (MSB)
Output center frequency ($\mathbf{f_c}$)	The modulated signal center frequency can be shifted in frequency 32-bit signed integer (2's complement representation) expressed as $\mathbf{f_c} * 2^{32} / \mathbf{f_{clk\_dac}}$ REG14 (LSB) – REG17 (MSB)
External transmitter gain control	When using an external transceiver such as the COM-350x family, the transmitter gain can be controlled through the TX_GAIN_CNTRL1 analog output signal. Range 0 – 3.3V. REG22: LSB, REG23(3:0): MSb

Demodulator	
Parameters	**Configuration**
Generate ADC sampling clock	In some cases, the external receiver/analog-to-digital converter (ADC) may require a sampling clock. The COM-1805 generates such a programmable frequency clock on pin J4.A14 or J8.A14 or J8.B29/30 depending on the firmware option being run. 0 = disable 1 = enable REG24(7)
ADC sampling rate $\mathbf{f_{clk\_rx}}$	When enabled, the programmable ADC sampling clock is defined by the parameters below: Expressed as $\mathbf{f_{clk\_rx}}$ = 160 MHz * M / (D * O)) where D is an integer divider in the range 1 - 106 M is a multiplier in the range 2.0 to 64.0 by steps of 1.0. Fixed point format 7.3 O is a divider in the range 2.0 to 128.0 by steps of 1.0. Fixed point format 7.3 Note: the graphical use interface computes the best values for M, D and O. Maximum $\mathbf{f_{clk\_rx}}$: 160 MHz REG24(6:0) = D REG25 = M(7:0) REG26(1:0) = M(9:8) REG27 = O(7:0) REG28(1:0) = O(10:8)
Demod input selection	0 = baseband input (I/Q complex samples) 1 = IF input (I as real input, Q is ignored) 7 = internal loopback REG28(6:4)

External AGC response time	Users can to optimize AGC response time while avoiding instabilities (depends on external factors such as gain signal filtering at the RF front-end and modulation symbol rate). The AGC_DAC gain control signal is updated as follows 0 = every symbol, 1 = every 2 input symbols, 2 = every 4 input symbols, 3 = every 8 input symbols, etc…. 10 = every 1000 input symbols. Valid range 0 to 14. REG29(4:0)
Nominal input center frequency (f_c)	The nominal center frequency is a fixed frequency offset applied to the input samples. It is used for fine frequency corrections, for example to correct clock drifts. 32-bit signed integer (2's complement representation) expressed as $f_c * 2^{32} / f_{clk\_adc}$ REG30 (LSB) – REG33 (MSB)
Nominal symbol rate f_{symbol_rate}	Nominal symbol rate, defined as $f_{symbol\_rate} * 2^{32} / f_{clk\_adc}$ REG34 (LSB) – REG37 (MSB)
CIC_R	Receiver decimation factor from f_{clk_adc} to 8* f_{symbol_rate}. Valid range 1 - 16384 REG38 (LSB) – REG39 (MSB)
Modulation type	0 = BPSK 1 = QPSK 2 = OQPSK REG40(5:0)
Spectrum inversion	Invert Q bit 0 = off 1 = on REG40(6)
Periodic sync marker detection (NEW)	Helpful in removing phase ambiguity at the demodulator. Required for Turbo code decoder frame synchronization. 0 = off 1 = on REG40(7)
Root raised cosine filter rolloff	1 = 20%, 4 = 35%, 7 = 50% REG42(2:0)

Frequency acquisition range (scan)	The demodulator natural frequency acquisition range is around 20% of the symbol range (depending on modulation, SNR). The frequency acquisition range can be extended by frequency scanning. Scanning steps are spaced ($f_{symbol\ rate\ rx}$ /4) apart. The user can thus trade-off acquisition time versus frequency acquisition range by specifying the number of scanning steps here. For example, 4 steps yield a frequency acquisition range of +/-$f_{symbol\ rate\ rx}$ REG41
V.34 descrambling	0 = disabled 1 = enabled REG44(1)
Data formatting	0 = NRZ-L 1 = NRZ-M 2 = NRZ-S REG44(6:4)
Output selection	1 = LAN TCP port 1025 2 = UDP 3 = serial data bit + bit clock, J4 left connector. 4 = synchronous clock + serial data bit + data valid, J4 left connector. REG45(6:4)

Error correction	
FEC encoding	'1' enabled, '0' bypassed Depending on the firmware loaded, the FEC decoder is either - K=7 rate ½ Viterbi decoding, or - turbo code REG45(0)
FEC decoding enabled	'1' enabled, '0' bypassed REG44(0)
Turbo code encoder **U**ncoded payload size in Bytes.	Preferred sizes: 14, 63, 250 Bytes Must NOT be an integer multiple of 15 Maximum 254 Bytes. REG65
Turbo code encoder rate	0 = rate 1/3 1 = rate 1/2 2 = rate 2/3 3 = rate 3/4 4 = rate 4/5 5 = rate 5/6 6 = rate 6/7 7 = rate 7/8 REG66(3:0)
Turbo code encoder **E**ncoded frame size in bits	Encoded frame size in bits. For example: when payload size is 14, rate 1/3, the encoded frame size is 14*8*3 = 336 bits. Does not include any periodic synchronization field. REG67 LSB REG68(6:0) (MSB)
Turbo code decoder **D**ecoded payload size in Bytes.	Preferred sizes: 14, 63, 250 Bytes Must NOT be an integer multiple of 15 Maximum 254 Bytes. REG69
Turbo code decoder rate	0 = rate 1/3 1 = rate 1/2 2 = rate 2/3 3 = rate 3/4 4 = rate 4/5 5 = rate 5/6 6 = rate 6/7 7 = rate 7/8 REG70(3:0)
Turbo code decoder **C**oded frame size in bits	Coded frame size in bits. For example: when payload size is 14, rate 1/3, the coded frame size is 14*8*3 = 336 bits. Does not include any periodic synchronization field. REG71 LSB REG72(6:0) (MSB)
Turbo code decoder maximum number of iterations	1 – 15. Typical settings is 7. Must be an odd number REG73

Network Interface	
Parameters	**Configuration**
LAN MAC address LSB	REG236. To ensure uniqueness of MAC address. The MAC address most significant bytes are tied to the FPGA DNA ID. However, since Xilinx cannot guarantee the DNA ID uniqueness, this register can be set at the time of manufacturing to ensure uniqueness. This byte is not overwritten when importing configuration data.
Static IP address	4-byte IPv4 address. Example : 0x AC 10 01 80 designates address 172.16.1.128 REG47 (MSB) - REG50 (LSB)
Subnet mask	REG51 (MSB) – REG54(LSB)
Gateway IP address	REG55 (MSB) – REG58(LSB)
Destination IP address	4-byte IPv4 address Destination IP address for UDP frames with decoded data. REG59 (MSB) – REG62(LSB)
Destination ports	REG63(LSB) – REG64(MSB)

(Re-)Writing to the last control register REG73 is recommended after a configuration change to enact the change.

Status Registers

Parameters	Monitoring
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-9 Properly operating hardware will result in the following sequence being displayed: 01 F1 1D xx 1F 93 10 00 22 1F.
LAN PHY ID	0x22 SREG8
FPGA Configuration options enabled in this active firmware	SREG48(0): modulator SREG48(1): demodulator SREG48(2): AWGN generation SREG48(3): error correction type: '0' for convolutional '1' for turbo code
Tx: Modulator saturation	Saturation in the output signal path. 0 when no saturation. These flags are reset upon reading this status register. SREG10(0)
Tx: Measured modulated signal power	SREG11(LSB) – SREG13(MSB)
Tx: Measured AWGN power	Approximation: noise power is uniform over a range of +/- 2*symbol rate SREG14(LSB) – SREG16(MSB)
FEC decoder input BER measurement (convolutional code)	The burst-mode FEC decoder computes the input BER prior to decoding. Mesasured in a frame. This method works with any bit sequence. SREG17 (LSB) - SREG19 (MSB)
Viterbi decoder lock status	(Only when convolutional FEC) 0 = unlocked 1 = locked SREG20(0)
BER tester synchronized	SREG20(2): 1 when the BERT is synchronized with the received PRBS-11 test sequence.
Bit error rate	Monitors the BER (number of bit errors over 80,000 received bits) when the modulator is sending a PRBS-11 test sequence. SREG21 (LSB) – SREG23 (MSB)
AGC	Front-end AGC gain settings. 12-bit unsigned. Inverted (0 for maximum gain) SREG24 (LSB) SREG25(3:0) (MSB)
Carrier frequency offset1	Residual frequency offset with respect to the nominal carrier frequency. Part 1/2. Includes receiver frequency scanning and carrier tracking loop. 32-bit signed integer expressed as fcerror * 2^{32} / f_{clk_rx} SREG26 (LSB) – SREG29 (MSB)
Carrier frequency offset2	Residual frequency offset with respect to the nominal carrier frequency. Part 2/2. Includes FFT-based frequency measurement (fixed after acquisition) 32-bit signed integer expressed as fcerror * 2^{31} / f_{symbol_rate} SREG30 (LSB) – SREG33 (MSB)
Inverse SNR	A measure of noise over signal power. 0 represents a noiseless signal. Valid only when demodulator is locked. SREG34 (LSB)
Demod status	Bit 0: carrier lock Bit 1: rx signal presence Bit 2: Start of frame lock (most reliable status) SREG36
Input sampling rate	The input sampling rate is measured and displayed here. The frequency measurement accuracy is a function of the internal clock stability. The measurement is expressed in Hz. SREG49 (LSB) – SREG52(MSB)

TCP-IP Connection Monitoring	
Parameters	**Monitoring**
MAC address	Unique 48-bit hardware address (802.3). In the form SREG40:SREG41:SREG42: …:SREG45
Ethernet MAC bad CRC counter	SREG46 (LSB) – SREG47(MSB)

Multi-byte status variables are latched upon (re-)reading SREG7.

ComScope Monitoring

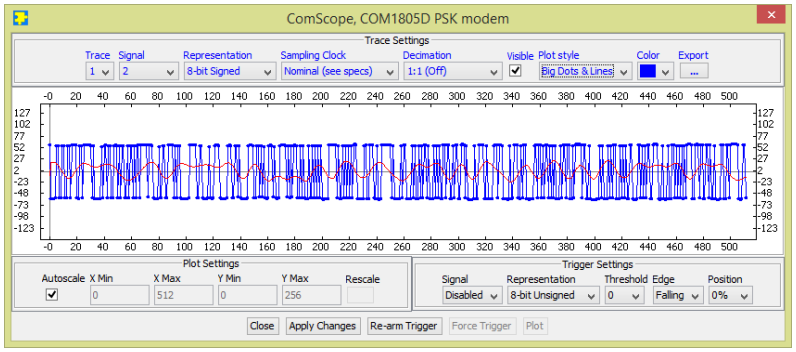
Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. Click on the button to start, then select the signal traces and trigger are defined as follows:

Trace 1 signals	Format	Nominal sampling rate	Buffer length (samples)
1: I-channel input, directly from ADC (could be at IF)	8-bit signed	ADC clock f_{clk_adc}	512
2:Demodulated I-channel (center of eye diagram)	8-bit signed	1 samples/ symbol	512
3: front-end AGC	8-bit unsigned	2 samples/ symbol	512
4: Symbol timing loop: accumulated timing correction	8-bit signed	1 sample / symbol	512
5: Tx bit stream before NRZ and FEC encoding	8-bit signed	1 sample / symbol	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Input Q signal	8-bit signed	ADC clock f_{clk_adc}	512
2: I signal after AGC, frequency translation to baseband, decimation	8-bit signed	Input sampling rate/R	512
3: Carrier tracking loop: accumulated phase correction	8-bit signed	1 sample / symbol	512
4: Inverse SNR	8-bit unsigned	1 sample/ symbol	512
5:Demodulated Q-channel (center of eye diagram)	8-bit signed	1 samples/ symbol	512
Trace 3 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Rx bit stream after FEC and NRZ decoding	8-bit signed	1 sample / symbol	512
2: Tx waveform, I-channel after modulation and AWGN	8-bit signed	f_{clk_adc}	512
3: Tx waveform, Q-channel after modulation and AWGN	8-bit signed	f_{clk_adc}	512

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk_adc} demod clock as real-time sampling clock.

In particular, selecting the f_{clk_adc} demod clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope Window Sample: showing internal PSK demodulator signals (blue = center of symbol, red = baseband received waveform)

Digital Test Points

Test Point	Definition
J4/A18	BER tester synchronized
J4/A19	BER tester matched filter output (detects start of PRBS11 sequence)
J4/A20	Byte error detected by BER tester
J4/A21	Transmit start of frame
J4/A22	Modulator saturation
J4/A23	Receiver SOF locked
J4/A24	Demod signal presence detected at FFT

J4/A25	Demodulator recovered carrier/center frequency
J4/A26	Demodulator recovered symbol timing error frequency

These test points can be placed in high-impedance by setting control register REG46(0) to '0'.

Options

Several interface types are supported through multiple firmware options. All firmware versions are on the supplied CD-ROM and can also be downloaded from
http://www.comblock.com/download.html

Changing the firmware option requires loading the firmware once using the ComBlock control center, then switching between the stored firmware versions The selected firmware option is automatically reloaded at power up or upon software command within 18 seconds

Option	Definition
-A	J8 right connector: 2*12-bit unsigned (offset binary) output samples to an external dual DAC. This interface is compatible with the COM-2001 dual 10-bit DACs. (maximum 125 MSamples/s) J4 left connector: 2*12-bit input, COM-30XX compatible receiver
-B	Receiver-only. J8 right connector: 2*12-bit input samples. Input compatible with COM-30xx receivers J4 left connector: synchronous serial receiver output bit stream.
-C	J8 right connector: 2*16-bit output samples, 2*12-bit input samples. This interface is compatible with the COM-3504 dual Analog<->Digital Conversions. Maximum 160 MSamples/s. J4 left connector: synchronous serial modem input and output bit streams.
-D	J8 Right connector : 2*16-bit LVDS output samples. This interface is compatible with the COM-4009 broadband RF modulator. J4 left connector: 2*12-bit input, COM-30XX compatible receiver
-E	J8 right connector: 2*14-bit unsigned (offset binary) output samples to an external dual DAC. This interface is compatible with the COM-4004 70 MHz [0.2 - 88 MHz] IF modulator, 50 MSamples/s.

	J4 left connector: 2*12-bit input, COM-30XX compatible receiver
-F	Transmitter-only J8 Right connector : 2*16-bit LVDS output samples. This interface is compatible with the COM-4009 broadband RF modulator. J4 left connector: synchronous serial transmitter input bit stream.
-G	Demodulator-only (no error correction). J4 left connector: 2*12-bit input, COM-30XX compatible receiver J8 right connector for demodulator I/Q 4-bit soft-quantized samples. (NEW)

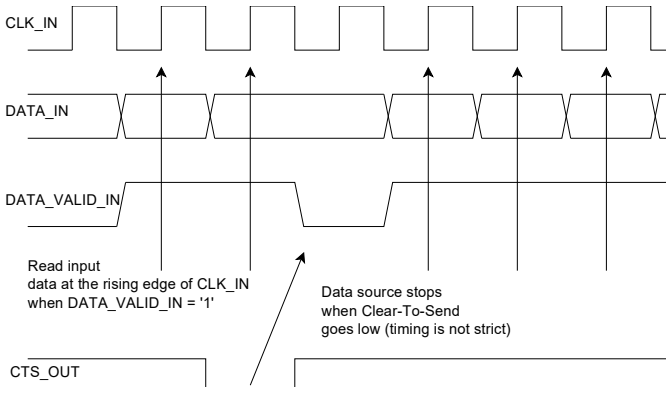
Operation

Transmitter Inputs

The transmitter supports two input types:

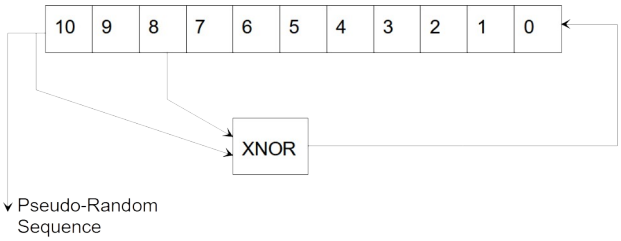
1. A TCP connection from a remote TCP client over Gigabit Ethernet (10/100/1000 Mbps). The modem comprises a TCP server listening at port 1024. The TCP protocol ensures a proper flow control, without any underflow or overflow, as long as the TCP client sends data as fast as allowed by the TCP connection.

2. Clock synchronous serial data through the left connector if available [the left connector could also be used by other modules]. The transmit data flow is controlled by a "Clear-To-Send" flag from the modulator. The data source should stop sending new data when the CTS_OUT flag is low.



Pseudo-Random Bit Stream (Test Pattern)

A periodic pseudo-random sequence can be used as modulator source instead of the input data stream. A typical use would be for end-to-end bit-error-rate measurement of a communication link. The sequence is 2047-bit long maximum length sequence generated by a 11-tap linear feedback shift register:



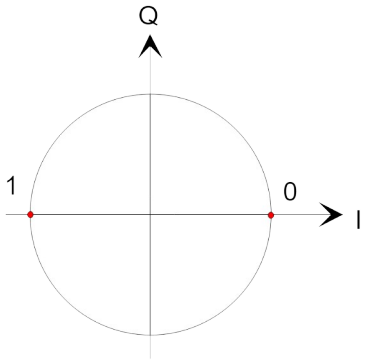
The first 100 bits of the PN sequence are as follows:
0000000000 0111111111 0011111110 0001111100
1100111000 0000010011 1111010001 1110110100
1101001100 0011000001

Constellation: Symbol Mapping

The packing of serial data stream into symbols is done with the Most Significant bit first.

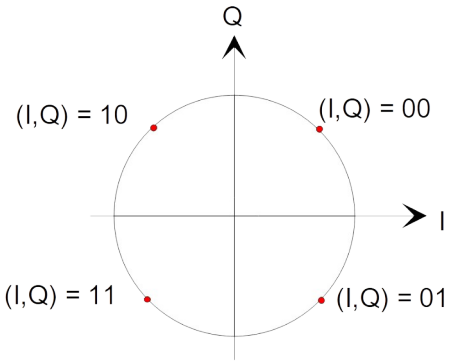
BPSK

REG6(5:0) = 0



QPSK

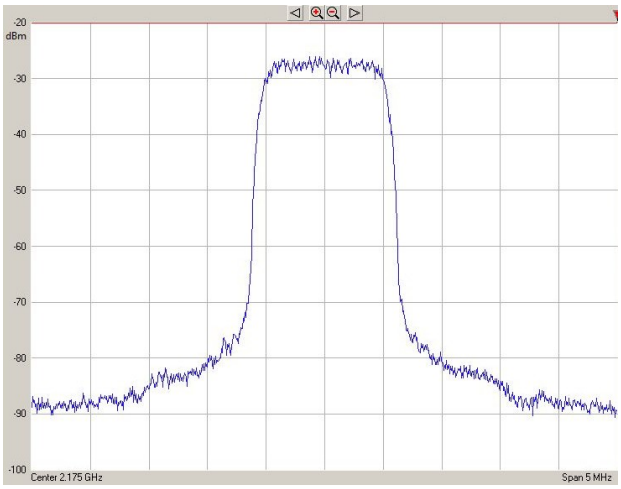
REG6(5:0) = 1
Gray encoding.



Format Conversion

Serial to parallel conversion occurs at the interface between the modem and the LAN. The general rule is that the first received bit is placed at the MSb position in the byte.

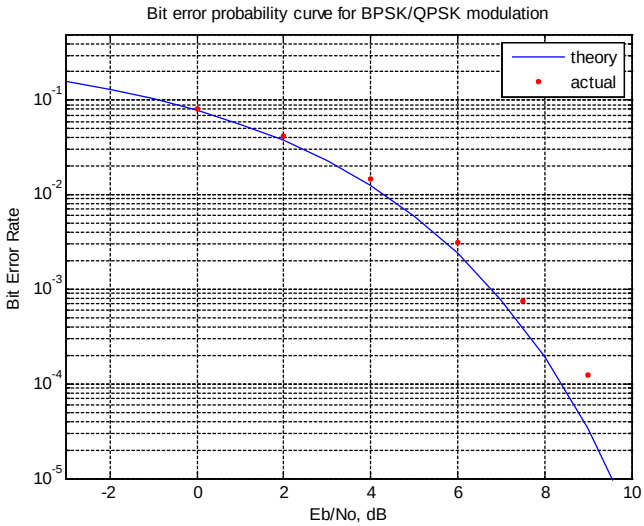
Output Spectrum



QPSK output spectrum 1MSymbols/s
(output of COM-4009 RF modulator, 2.175GHz)

BER vs Eb/No

The plot below shows near-theoretical performance for the PSK demodulators without error correction.



BER performance, demodulator only (no FEC)

Receiver Outputs

The receiver supports four output types:

1. A TCP server listening/waiting for a client connection over Gigabit Ethernet (10/100/1000 Mbps) at port 1025. Once the remote client is connected, the receiver forwards the demodulated data stream to the TCP client.

2. A UDP server sending frames to the user-specified destination IP address. UDP frames are sent when upon receiving 1024 bytes of data or after 0.5 second, whichever event comes first. The UDP frame format is as follows:
16-bit frame size
16-bit frame counter
12 null bytes
up to 1024 data bytes.

Phase Ambiguity Resolution

The QPSK demodulator exhibits an inherent 0/90/180/270 phase ambiguity. To resolve this ambiguity, a periodic 32-bit synchronization word (0x5A0FBE66) is transmitted at the start of every frame and detected at the receiver. The frame size depends on the FEC codec selection:
- 2048+32 bit for convolutional code or no FEC, or
- one, two, four or eight turbo code encoder frames

Bit Timing Tracking

A first order loop is capable of acquiring and tracking bit timing differences between the transmitter and the receiver of at least ± 50 ppm.

AGC

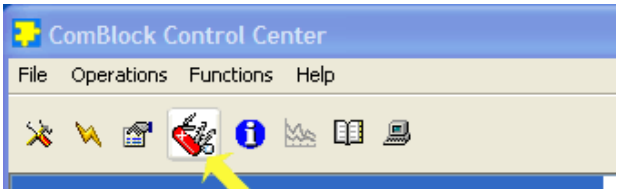
To maintain linearity throughout the receive path, several AGC loops control the signal level. While most AGC loops are internal, an additional AGC loop is dedicated to controlling an RF front-end.

The purpose of this AGC is to prevent saturation at the external A/D converter(s) while making full use of the A/D converter(s) dynamic range. The controlling analog signal is J4.B13 or J8.B13.

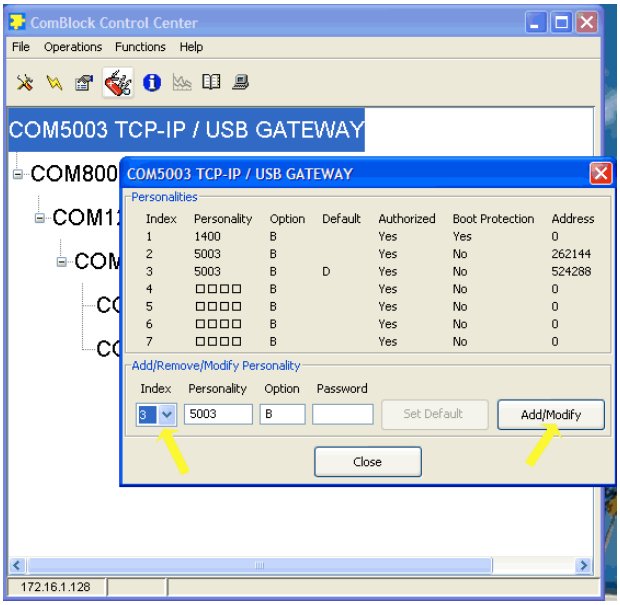
Load Software Updates

From time to time, ComBlock software updates are released.

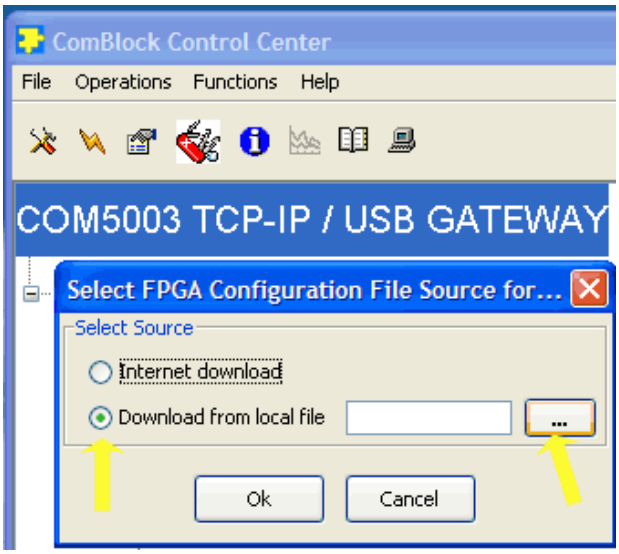
To manually update the software, highlight the ComBlock and click on the Swiss army knife button.



The receiver can store multiple personalities. The list of personalities stored within the ComBlock Flash memory will be shown upon clicking on the Swiss army knife button.



The default personality loaded at power up or after a reboot is identified by a ‘D’ in the Default column. Any unprotected personality can be updated while the Default personality is running. Select the personality index and click on the “Add/Modify” button.



The software configuration files are named with the .bit extension. The bit file can be downloaded via the Internet, from the ComBlock CD or any other local file.

The option and revision for the software currently running within the FPGA are listed at the bottom of the advanced settings window.

Recovery

This module is protected against corruption by an invalid FPGA configuration file (during firmware upgrade for example) or an invalid user configuration. To recover from such occurrence, connect a jumper in J3 and during power-up. This prevents the FPGA configuration and restore USB communication [LAN communication is restored only if the IP address is known/defined for the personality index selected as default]. Once this is done, the user can safely re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center.

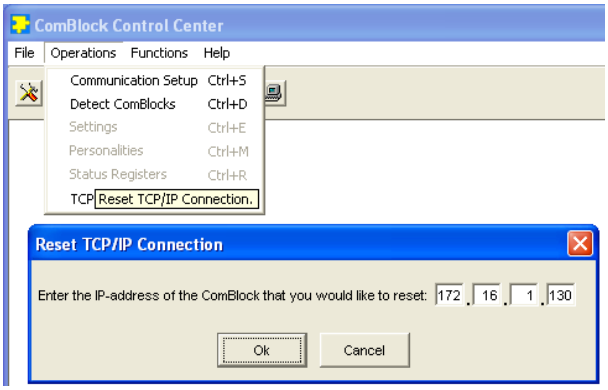
UDP Reset

Port 1029 is open as a UDP receive-only port. This port serves a single purpose: being able to reset the modem (and therefore the TCP-IP connection) gracefully. This feature is intended to remedy a common practical problem: it is a common occurrence for one side of a TCP-IP connection to end abnormally without the other side knowing that the connection is broken (for example when a client 'crashes'). In this case, new connections cannot be established without first closing the previous ones.

The problem is particularly acute when the COM-1805 is at a remote location.

The command "@001RST<CR><LF>" sent as a UDP packet to this port will reset all TCP-IP connections within the COM-1805.

TCP-IP connections can also be cleared remotely from the ComBlock Control Center as illustrated below:

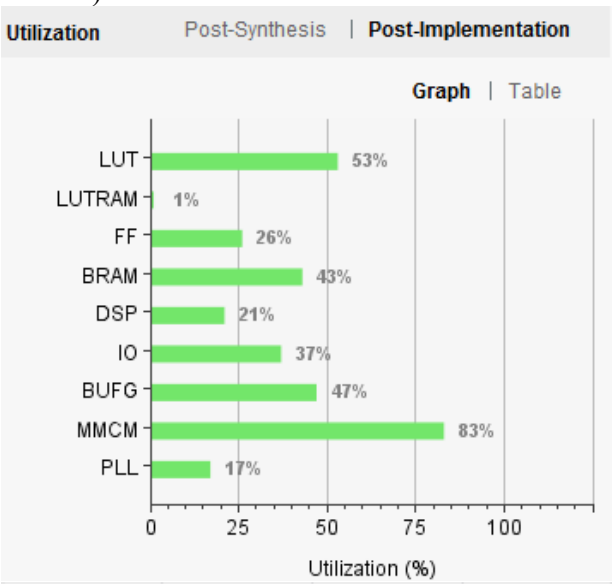


Troubleshooting Checklist

1. The module is performs self-checks at power up. Click on  to display the status registers. Properly operating hardware will result in the following sequence being displayed: SREG0-SREG8 = 01 F1 1D xx 1F 93 10 00 22.
2. Check status register SREG4 bits 0 – 5: if not 111111, the power supply voltage may be outside the nominal range of 4.9 to 5.5V.
3. Demodulator can't achieve lock even at high signal-to-noise ratios:
   - Make sure the modulator baseband I/Q signals do not saturate, as such saturation would strongly distort the modulation phase information. (this is a phase demodulator!)

VHDL code

The FPGA code is written in VHDL. It does not use any IP core or third-party software.
It occupies the following FPGA resources (when including modulator, demodulator, turbo code, AWGN):



Resource	Utilization	Available	Utilization...
LUT	33405	63400	52.69
LUTRAM	138	19000	0.73
FF	32452	126800	25.59
BRAM	57.50	135	42.59
DSP	50	240	20.83
IO	105	285	36.84
BUFG	15	32	46.88
MMCM	5	6	83.33
PLL	1	6	16.67

Interfaces

ADC/DAC Interface	Definition
ADC_SAMPLE_CLKOUT_P ADC_SAMPLE_CLKOUT_N	ADC sampling clock output: 160 MHz.
ADC*x*_DATA_IN[13:2]	ADC*x* digital samples input. 12-bit unsigned (also known as "offset binary") format. The two least significant bits (1:0) are unused (reserved for future use). 0x0000: lowest output level 0x3FFF: highest output level 0x1FFF or 0x2000 ≈ center level CMOS 0 – 3.3V.

	Read at the rising edge of ADC*x*_SAMPLE_CLK_OUT.
ADC*x*_SAMPLE_ CLK_IN	Sampling clock input. Pinpoints the center of the ADC*x*_DATA_IN bits for reclocking at the receiving end. Index *x* is 1 or 2 CMOS 0 – 3.3V.
DAC_SAMPLE_CLKOUT_P DAC_SAMPLE_CLKOUT_N	DAC sampling clock output. Sets the DAC sampling rate. 0-3.3V LVCMOS differential signal. 160 Msamples/s
DAC*x*_DATA_OUT[15:0]	DAC*x* digital samples output. 16-bit unsigned (also known as "offset binary") format. 0x0000: lowest input level 0xFFFF: highest input level 0x7FFF or 0x8000 ≈ center level CMOS 0 – 3.3V. Read at the rising edge of DAC_SAMPLE_CLK_IN
AUX_SPI[5:1]	SPI interface to control the two auxiliary DACs and ADC in real-time. See AD5621 serial 12-bit DAC specifications. See AD7276 serial 12-bit ADC specifications.

Operating input voltage range

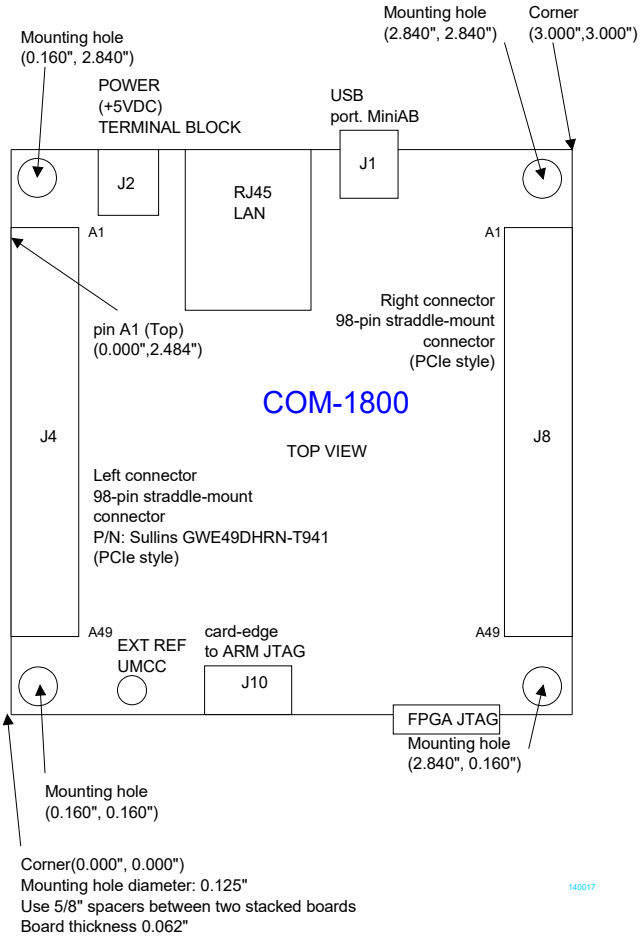
Supply voltage	+4.5V min, +12V max 650mA typ.

Absolute Maximum Ratings

Supply voltage	-0.5V min, +20V max
98-pin connector inputs	-0.5V min, +3.6V max

Important:
The I/O signals connected directly to the FPGA are NOT 5V tolerant!

Mechanical Interface



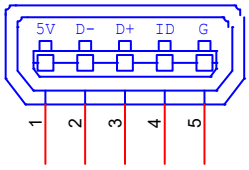
Schematics

The board schematics are available on-line at
http://comblock.com/download/com_1800schematics.pdf

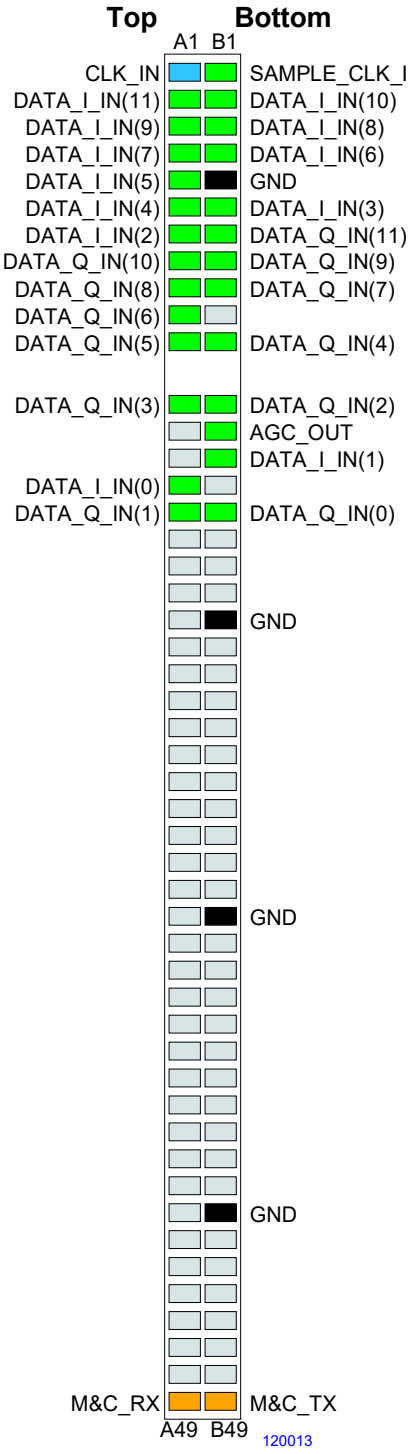
Pinout

USB

The USB port is equipped with mini type AB connectors. (G = GND). The COM-1805 acts as a USB device.

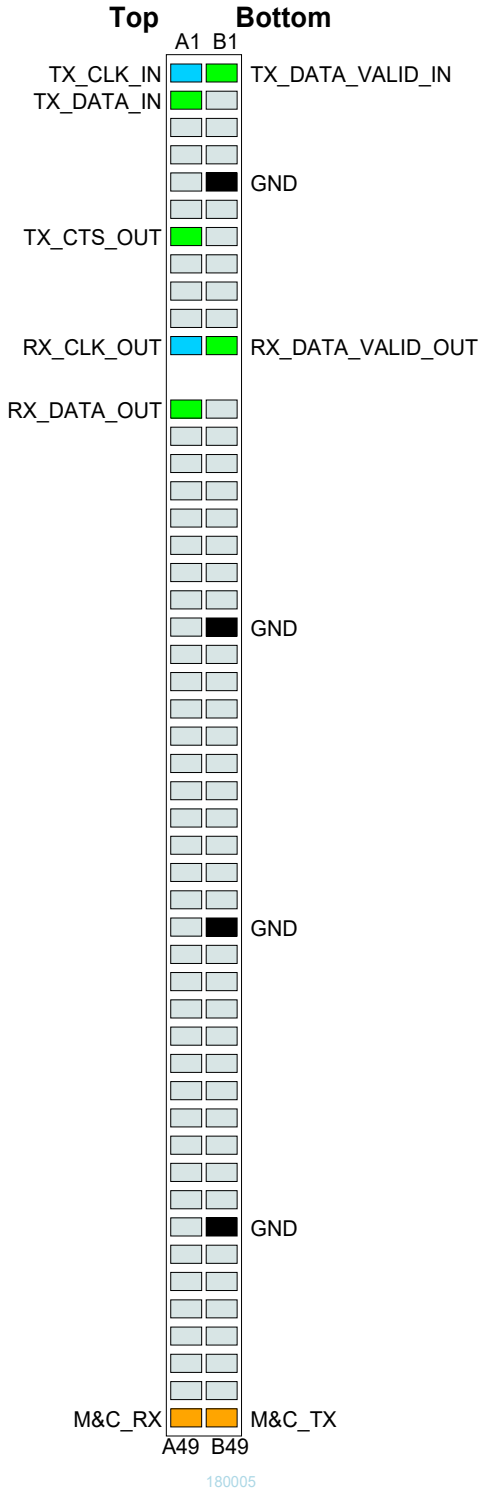


Left Connector J4



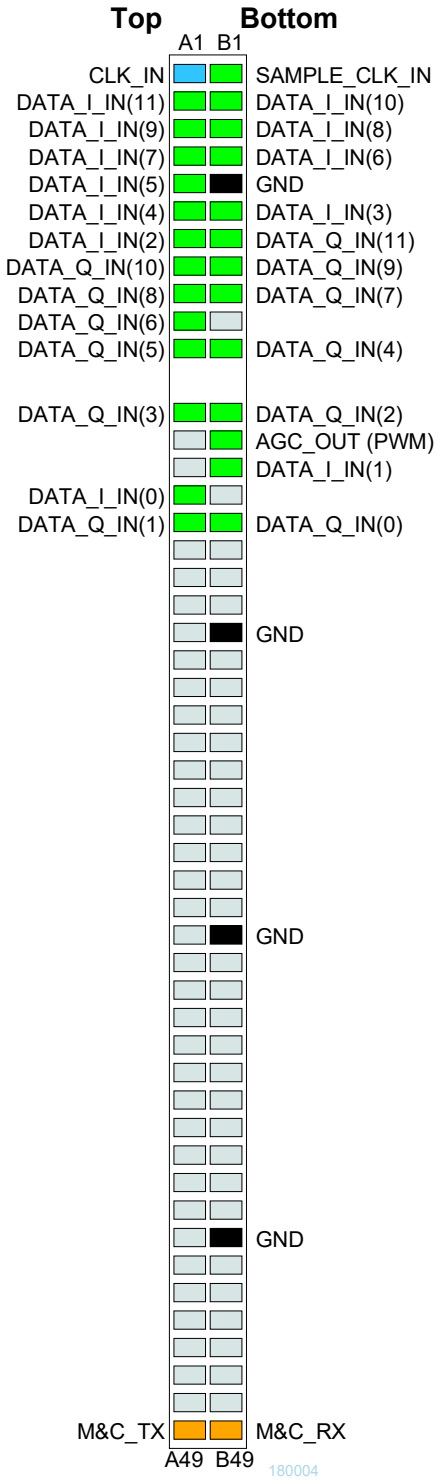
2*12-bit baseband input samples, compatible with COM-30xx receivers (**-A/-D** firmware options)

Left Connector J4



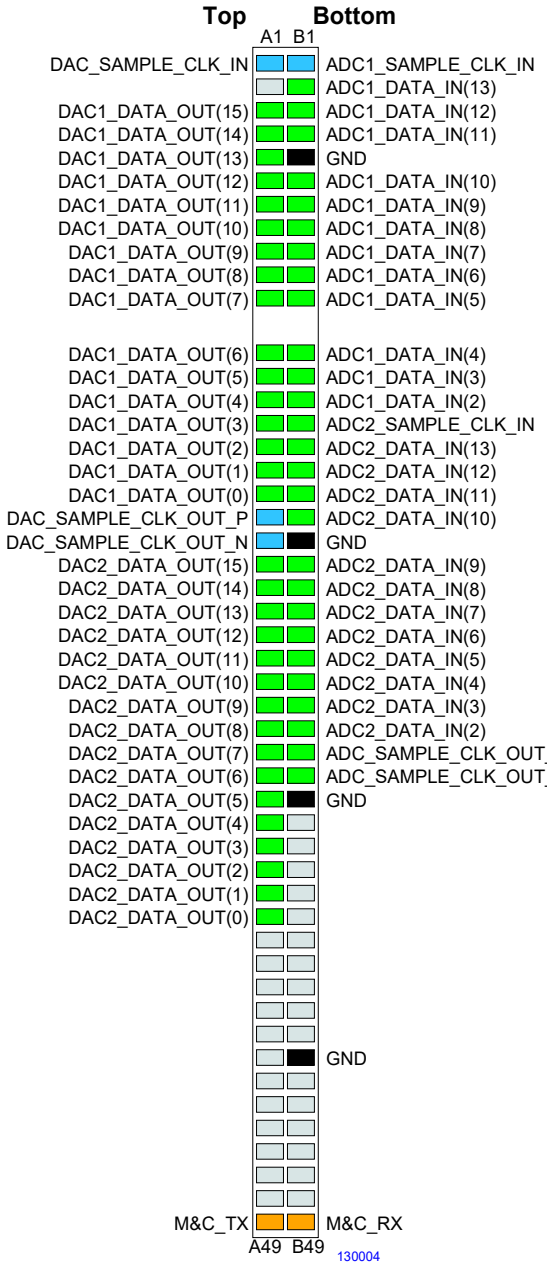
Modem synchronous serial input/output data, compatible with other digital ComBlock modules (COM-1800, etc). (**-B/-C** firmware options)

Right Connector J8



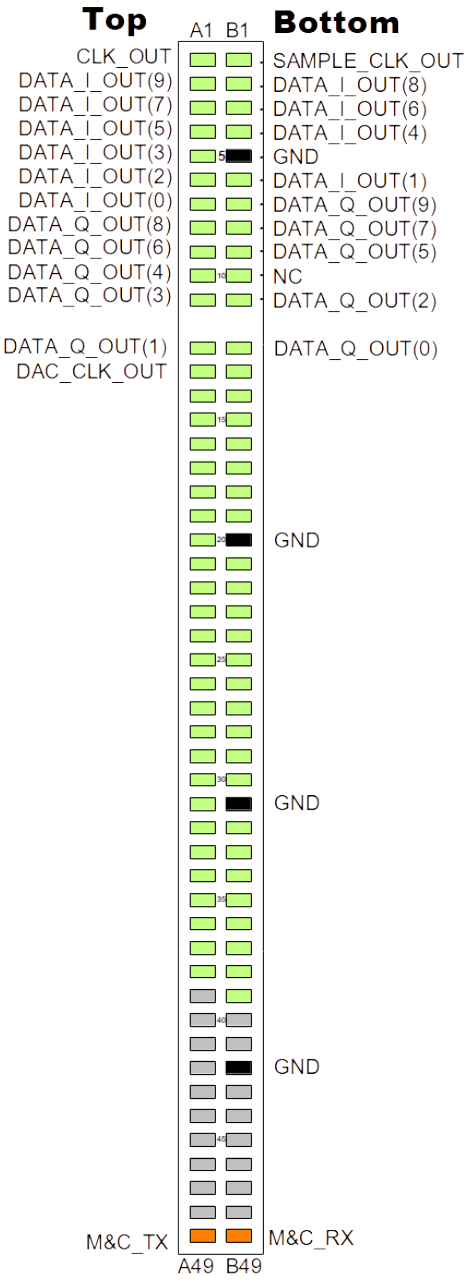
2*12-bit baseband input samples, compatible with COM-30xx receivers (**-B** firmware option)

Right Connector J8



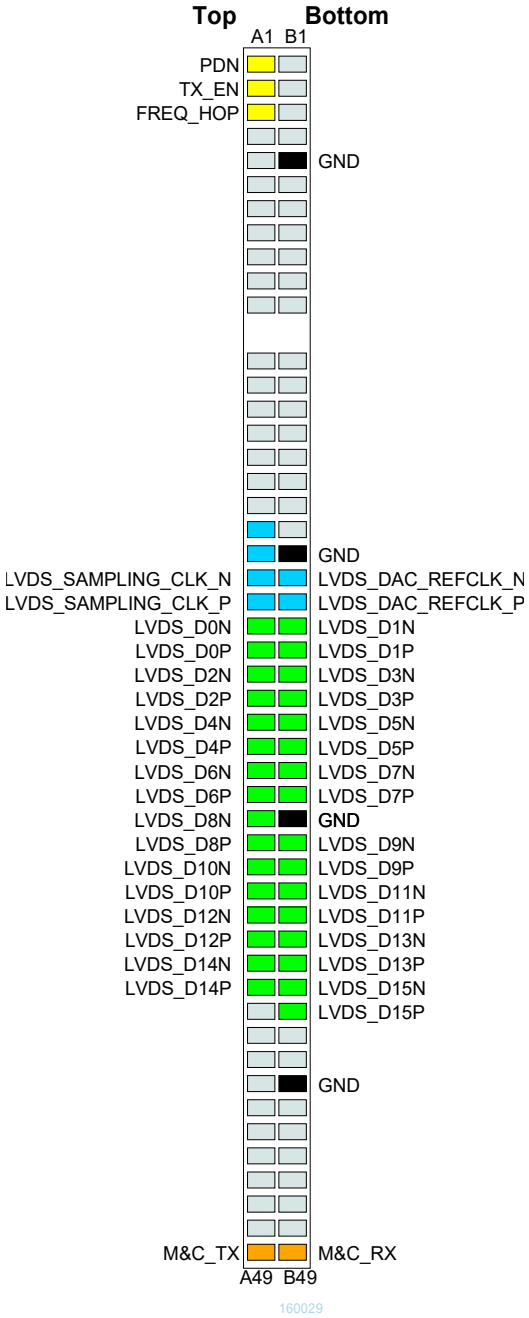
2*16-bit output samples, 2*12-bit input samples. This interface is compatible with the COM-3504 dual Analog<->Digital Conversions.
(**-C** firmware option)

Right Connector J8



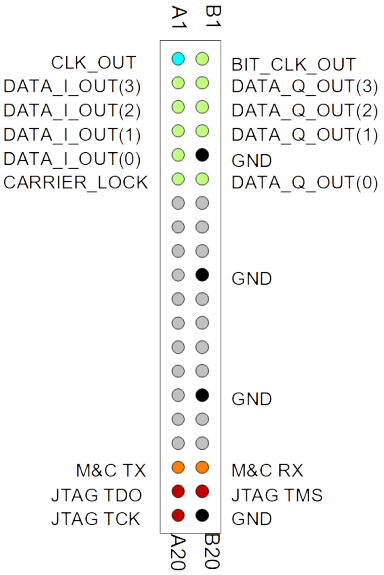
This interface is compatible with the COM-2001 dual DACs. (**-A** firmware option)

Right Connector J8



This interface is compatible with the COM-4009 RF modulator (**-D** firmware option)

Right Connector J8



This interface emulates the COM-1001 demodulator output. (**-G** firmware option)

I/O Compatibility List

(not an exhaustive list)

Right connector (J9)
COM-3504 Dual Analog <-> Digital Conversions 2*16-bit 250 MSamples/s
COM-4009 400 MHz – 4.4 GHz Broadband RF modulator
COM-30xx RF/IF/Baseband receivers for frequencies ranging from 0 to 3 GHz.
COM-2001 digital-to-analog converter (baseband).
COM-5404 IP gateway / router

Configuration Management

This specification is to be used in conjunction with VHDL software revision 1 and ComBlock control center revision 3.13g and above.

It is possible to read back the option and version of the FPGA configuration currently active. Using the ComBlock Control Center, highlight the COM-1805 module, then go to the advanced settings. The option and version are listed at the bottom of the configuration panel.

For the latest data sheet, please refer to the **ComBlock** web site: http://www.comblock.com/download/com1805.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

ComBlock Ordering Information

COM-1805 PSK modem

ECCN: 5A991.b.1

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