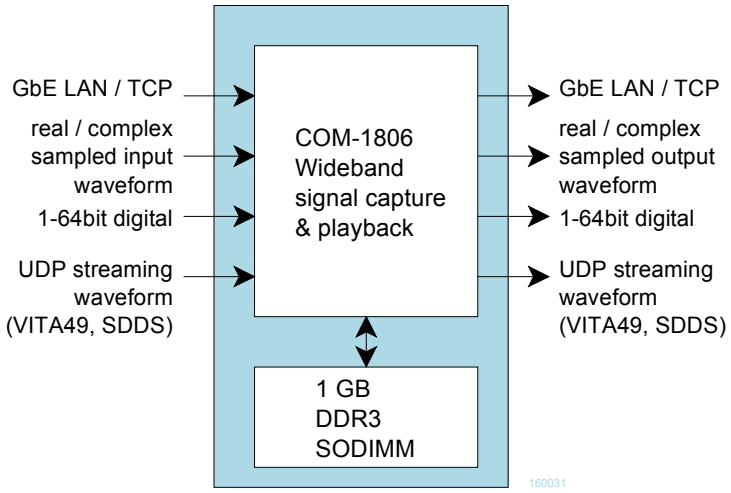
COM-1806
WIDEBAND SIGNAL CAPTURE & PLAYBACK 1GB



Key Features

- Combines the functions of high-speed data acquisition and wideband arbitrary waveform generator into a small 3”x3” module.
- Stores 1GBytes of binary data in DDR3 SDRAM.
- Upload the following high-speed inputs:
  - File transfer from a PC over GbE[1] LAN TCP or UDP
  - Digitized real or complex waveform 2*12-bit up to 125 Msamples/s
  - Digital LVTTL 0-3.3V inputs from 1 to 64-bit per sample, up to 125 Msamples/s.
  - VITA 49 or NASA SDDS formatted streaming waveforms over GbE LAN UDP (future).
- Download SDRAM contents to the following high-speed outputs:
  - File transfer to a PC over GbE LAN TCP or UDP
  - Digitized real or complex waveform 2*16-bit up to 125 Msamples/s
  - Digital LVTTL 0-3.3V outputs from 1 to 64-bit per sample, up to 125 Msamples/s.
  - VITA 49 or NASA SDDS formatted streaming waveforms over GbE LAN UDP (future).
- Upload to SDRAM and download from SDRAM memory can be made concurrent.

- I/O samples widths supported: 1,2,4,8,16,32,64 bits.
- Input signal conditioning includes AGC, DC block, frequency translation, variable decimation with anti-aliasing filtering for lower sampling rates and longer capture time.

[1] Gigabit Ethernet LAN

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- Output signal conditioning includes variable interpolation and frequency translation.
- Input for an external, higher-stability 10 MHz frequency reference.
- Single run or continuous (circular) playback.
- User control over memory segmentation (upload/download start addresses, upload/download window sizes).
- Import from and export to tab-delimited text files or binary files.
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- High-speed 98-pin connectors (left, right). Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.

bottom side

Terminology:

This document uses a memory-centric terminology to describe the data flow:

Upload designates the transfer of data TO the COM-1806 SDRAM memory.

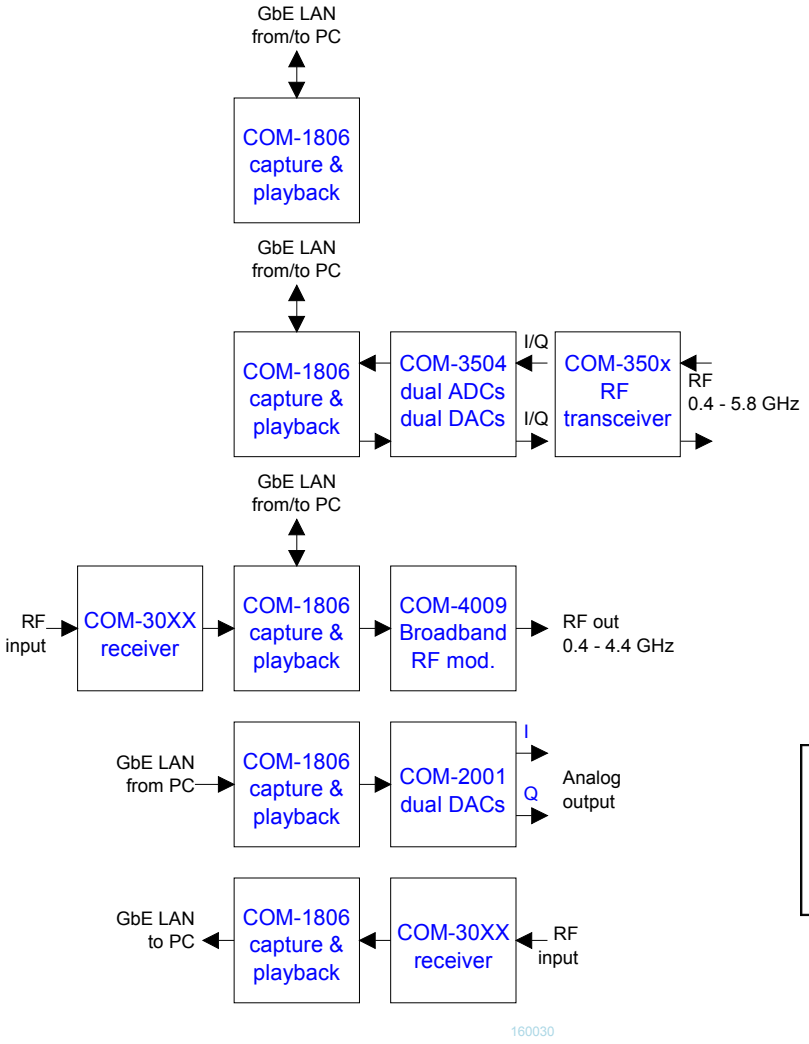
Download refers to the data transfer FROM the SDRAM.

Note: data transfer path and control path can be multiplexed over the same medium (LAN) or independent (for example high-speed data transfer over LAN and control over USB). Data transfer over USB is not supported.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1806.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

Typical Applications

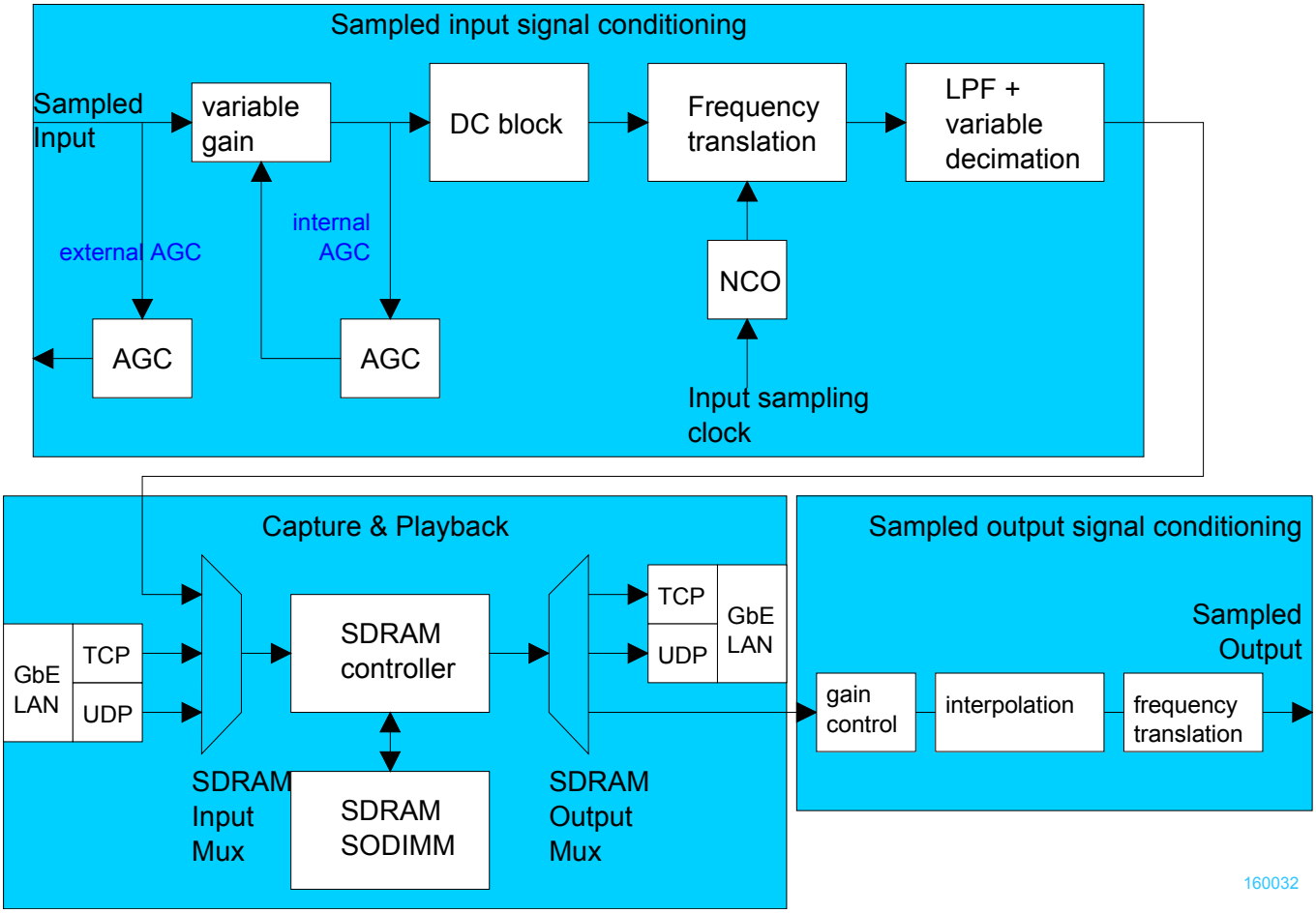


- COM-1806 as stand-alone module, captures a data stream from the GbE LAN, stores it in DDR3 memory for subsequent playback.
- COM-1806+COM-4009 = RF signal generator using a baseband waveform file uploaded from PC via high-speed LAN.
- COM-1806+COM-3504 = Simultaneous complex (I/Q) analog baseband capture (2*12-bit) and playback (2*16-bit). An additional COM-350x RF transceiver extends the functionality to RF signals.
- COM-1806+COM-2001 = Simple arbitrary waveform generator 2*10-bit 125 MSamples/s. Input waveform file can be uploaded from a PC via gigabit Ethernet LAN.
- COM-1806+COM-30xx = RF signal capture and subsequent file download to a PC via gigabit Ethernet LAN.

In this product release a few features in grey are not yet implemented. Future firmware updates will also include

- VITA-49 GbE format
- NASA SDDS GbE format
-

Block Diagram



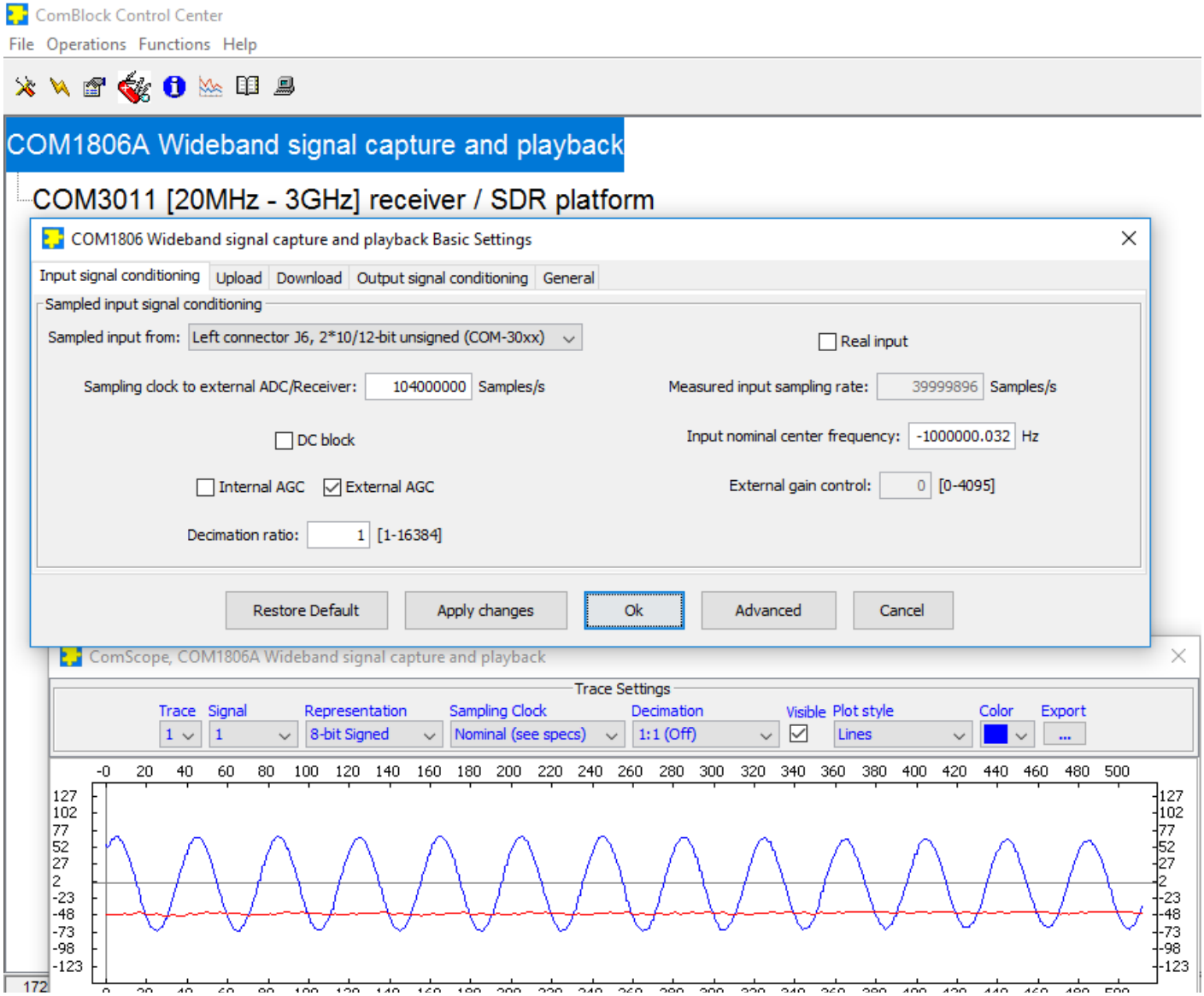
Configuration

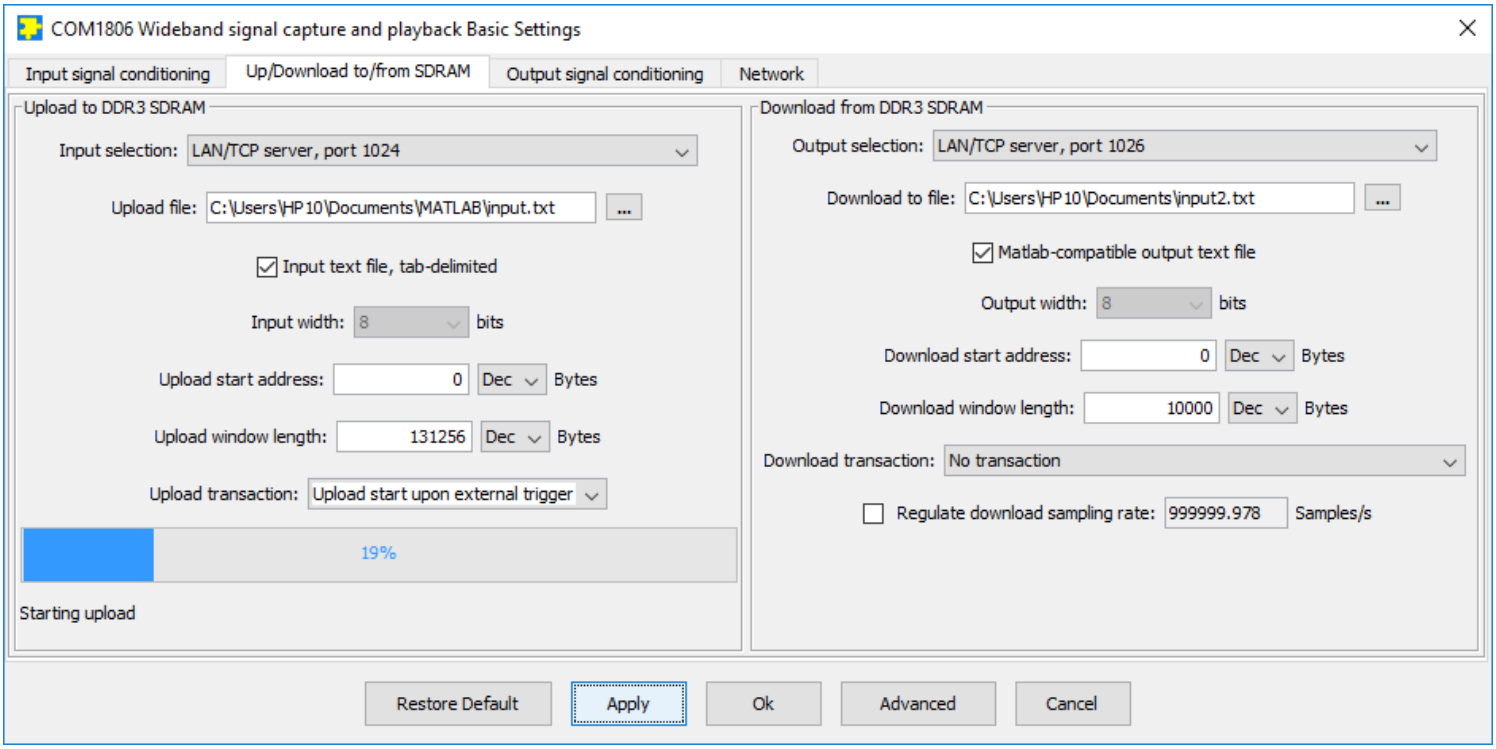
Complete assemblies can be monitored and controlled centrally over a built-in USB or gigabit Ethernet LAN or other media available through adjacent ComBlocks.

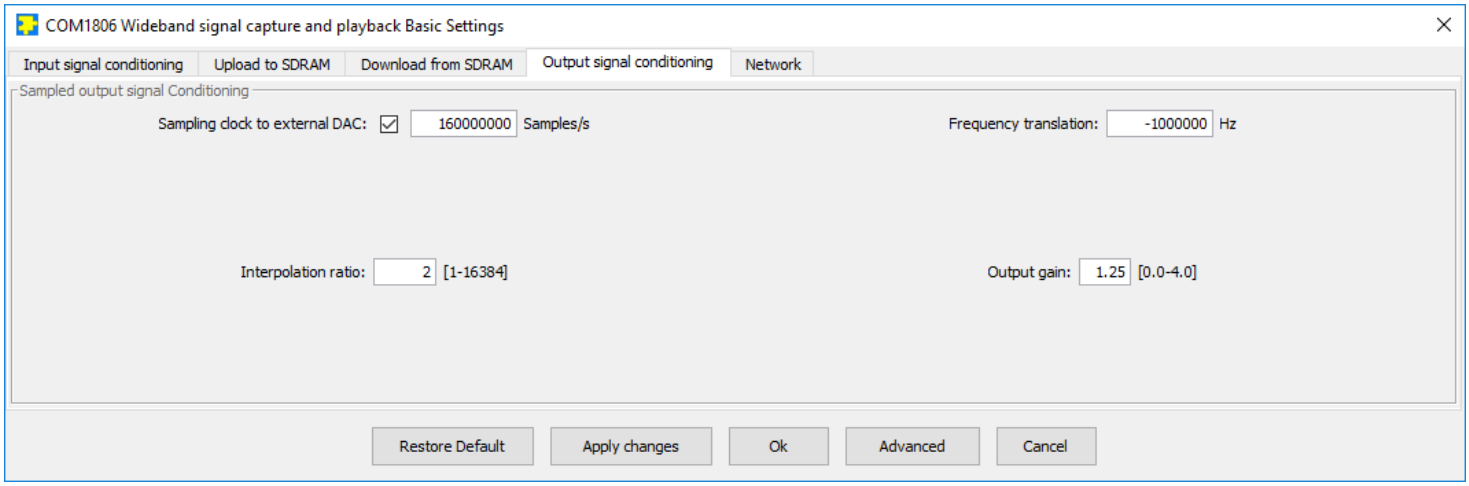
The module configuration is stored in non-volatile memory.

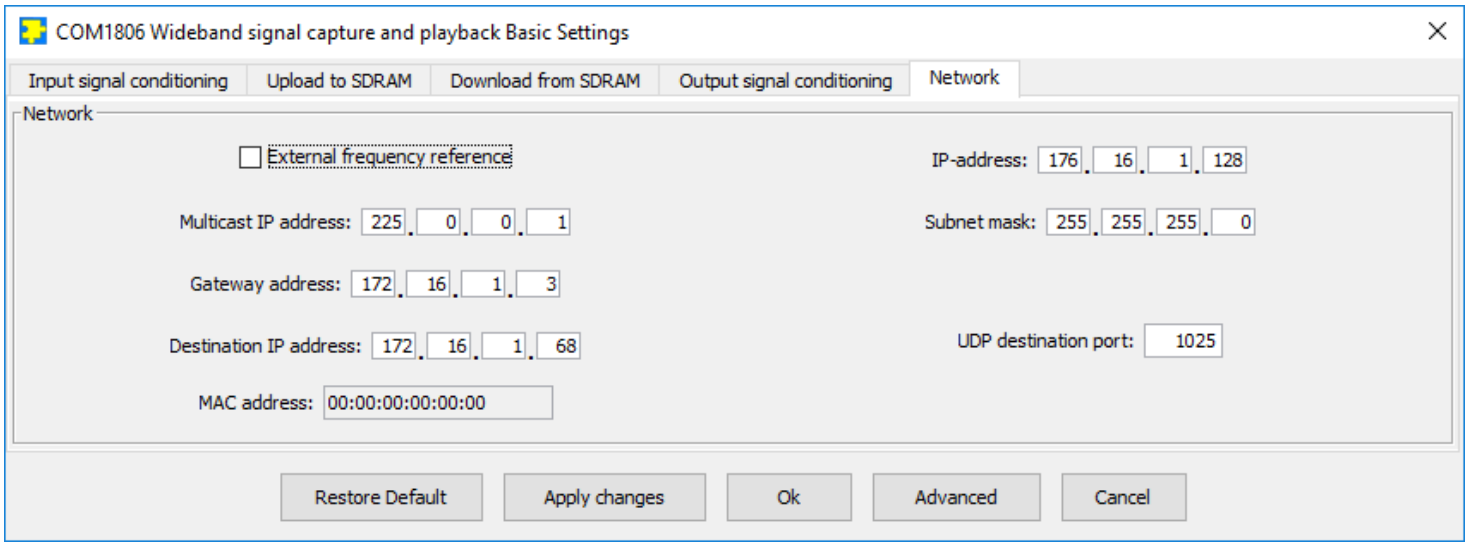
Configuration (Basic)

The easiest way to configure the COM-1806 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1806 module to be configured, next click the *Settings* button to display the *Settings* window shown below.




COM1806 Wideband signal capture and playback Basic Settings
Input signal conditioning
Up/Download to/from SDRAM
Output signal conditioning
Network
Upload to DDR3 SDRAM
Input selection: LAN/TCP server, port 1024
Upload file: C:\Users\HP10\Documents\MATLAB\input.txt
Input text file, tab-delimited
Input width: 8 bits
Upload start address: 0 Dec Bytes
Upload window length: 131256 Dec Bytes
Upload transaction: Upload start upon external trigger
19%
Starting upload
Download from DDR3 SDRAM
Output selection: LAN/TCP server, port 1026
Download to file: C:\Users\HP10\Documents\input2.txt
Matlab-compatible output text file
Output width: 8 bits
Download start address: 0 Dec Bytes
Download window length: 10000 Dec Bytes
Download transaction: No transaction
Regulate download sampling rate: 999999.978 Samples/s
Restore Default
Apply
Ok
Advanced
Cancel


COM1806 Wideband signal capture and playback Basic Settings
Input signal conditioning
Upload to SDRAM
Download from SDRAM
Output signal conditioning
Network
Sampled output signal Conditioning
Sampling clock to external DAC: 160000000 Samples/s
Frequency translation: -1000000 Hz
Interpolation ratio: 2 [1-16384]
Output gain: 1.25 [0.0-4.0]
Restore Default
Apply changes
Ok
Advanced
Cancel


COM1806 Wideband signal capture and playback Basic Settings
Input signal conditioning
Upload to SDRAM
Download from SDRAM
Output signal conditioning
Network
Network
External frequency reference
IP-address: 176 16 1 128
Multicast IP address: 225 0 0 1
Subnet mask: 255 255 255 0
Gateway address: 172 16 1 3
Destination IP address: 172 16 1 68
UDP destination port: 1025
MAC address: 00:00:00:00:00:00
Restore Default
Apply changes
Ok
Advanced
Cancel

Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

The processing clock f_{clkp} is 125 MHz.

General	
Parameters	**Configuration**
Internal/External frequency reference	0 = internal TCXO as frequency reference. 1 = external. Use the 10 MHz clock externally supplied through the J6 SMA connector as frequency reference. REG0(7)

Sampled input signal conditioning	
Parameters	**Configuration**
Sampled input selection	0 = undefined 1 = COM-3504 right connector, 2*12bit unsigned 2 = COM-30XX left connector, 2*12-bit unsigned 3 = COM-30XX right connector, 2*12-bit unsigned 4 = Internally-generated unmodulated carrier. REG0(2:0)
Generate ADC sampling clock	In some cases, the external receiver/analog-to-digital converter may require a sampling clock. The COM-1806 generates such a programmable frequency clock on pin J4.A14. 0 = disable 1 = enable REG1(7)
ADC sampling rate f_{clk_rx}	In some cases, the external receiver/analog-to-digital converter may require a sampling clock. The COM-1806 generates such a programmable frequency clock on pin J4.A14 by defining the parameters below: Expressed as f_{clk_rx} = 125 MHz * M / (D * O)) where D is an integer divider in the range 1 - 106 M is a multiplier in the range 2.0 to 64.0 by steps of 0.125. Fixed point format 7.3 O is a divider in the range 2.0 to 128.0 by steps of 0.125. Fixed point format 8.3 Note: the graphical use interface computes the best values for M, D and O. Maximum f_{clk_rx} : 160 MHz REG1(6:0) = D REG2 = M(7:0)

	REG3(1:0) = M(9:8) REG4 = O(7:0) REG5(2:0) = O(10:8)
Real or complex input?	0 = complex (I,Q) baseband input samples 1 = real samples on I-channel input. Q-channel input is zeroed. Use in the case of IF input. REG6(0)
DC block	The bias removal circuit removes any spurious DC bias that may be introduced by an external A/D convert. Disable this function if the input signal includes a legitimate DC offset. 0 = disable 1 = enable REG6(1)
Internal AGC enable	Enable or disable the input automatic gain control 0 = disabled (unit gain) 1 = enabled REG6(2)
External AGC enable	0 = gain control fixed at a preset level (see below) 1 = enabled The analog gain control output is on pin J4.B13 REG6(3)
External AGC gain	Gain settings for an external variable gain amplifier. This setting is used when the external AGC is disabled. It is also the initial gain value before the AGC takes over. Unsigned 12-bit number. 4095 represents the minimum gain, 0 the maximum gain. REG6(7:4): LSB REG7: MSB
External AGC response time	Users can to optimize AGC response time while avoiding instabilities (depends on external factors such as gain signal filtering at the RF front-end and chip rate). The AGC_DAC gain control signal is updated as follows 0 = every decimated sample, 1 = every 2 decimated samples, 2 = every 4 decimated samples, 3 = every decimated samples, etc…. 10 = every 1000 decimated samples.

	Valid range 0 to 14. REG8(4:0)
Nominal Center frequency (f_{c_rx})	As the signal capture is best implemented at baseband (near-zero center frequency), the input signal must first be translated in frequency. Enter the expected center frequency of the input signal. 32-bit integer expressed as $f_{c_rx} * 2^{32} / f_{input_sampling}$. where $f_{input_sampling}$ is the input sampling rate. In the case of IF undersampling, the residual intermediate frequency can be removed here. For example, in the case of a 150 MHz IF signal sampled at 120 Msamples/s, the 30 MHz residual frequency is removed here by entering 0x40000000. REG9(LSB) – REG12(MSB)
CIC decimation ratio **R**	Combined low-pass filter / decimation. The decimation ratio R is set here. Valid range 1 to 16384. 0 is illegal. Usage: be careful not to decimate too much as the CIC decimation filter is not very sharp and thus can distort the modulation signal. For most applications, select R = 1. REG13: LSB[2] REG14(6:0): MSB
Enable Half-Band Filter	Bypass (0) / Enable (1) Half-Band Filter following the CIC decimation filter. REG14(7)

[2] LSB = Least Significant Byte
MSB = Most Significant Byte

Upload to SDRAM	
Parameters	**Configuration**
Input selection	1 = LAN/TCP server, port 1024 2 = LAN/UDP packets 3 = sampled input waveform after conditioning (1 or 2*16-bit) 4 = digital inputs (no conditioning), left connector 5 = digital inputs (no conditioning), right connector 6 = VITA 49 formatted waveform from LAN/UDP(future) 7 = NASA SDDS formatted waveform from LAN/UDP (future) REG15(3:0)
Upload sample data width	Number of bits in each input sample saved into SDRAM. Valid entries: 1,2,4,8,16,32,64 Must be consistent with the input selection above. For example, LAN/TCP-IP data is always 8-bit wide. REG16(6:0)
Upload start address	It is possible to upload the entire memory or a fraction thereof. The upload section is identified by its start address and length. Unit: number of SDRAM 64-bit words. REG17 (LSB) – REG20 (MSB)
Upload window length	Upload window length. Unit: number of SDRAM 64-bit words. Wrapping around is not allowed, i.e. window start address + length must be less than the memory upper address. REG21 (LSB) – REG24 (MSB)
Upload transaction	0 = no change 1 = immediate upload start. Upload will continue until the specified number of bytes in the upload window length is received. 2 = start upload upon receiving a trigger pulse over the UPLOAD_TRIGGER pin. Starts at the falling edge of the pulse. 3 = immediately stop any on-going upload transaction. REG25(2:0)

Download from SDRAM	
Parameters	**Configuration**
Download start address	It is possible to download the entire memory or a fraction thereof. The download section is identified by its start address and length. Unit: number of SDRAM 64-bit words. REG27 (LSB) – REG30 (MSB)
Download window length	Download window length. Unit: number of SDRAM 64-bit words. Wrapping around is not allowed, i.e. window start address + length must be less than the memory upper address. REG31 (LSB) – REG34 (MSB)
Download transaction	0 = no change 1 = single download, immediate start 2 = continuous (circular) download, immediate start 3 = single download, external trigger 4 = continuous (circular) download, external trigger 5 = immediately stop current transaction. The trigger is a pulse over the DOWNLOAD_TRIGGER pin. Starts at the falling edge of the pulse. REG35(2:0)
Output selection	1 = LAN/TCP server, port 1026 2 = LAN/UDP packets 3 = sampled output waveform through output conditioning (1 or 2*16-bit) 4 = digital outputs (no conditioning), right connector 5 = VITA 49 formatted waveform to LAN/UDP(future) 6 = NASA SDDS formatted waveform to LAN/UDP (future) REG36(3:0)

Output data width	During download, the SDRAM contents is segmented into samples of various bit-widths as specified here. Supported data widths are: 1,2,4,8,16,32,64 Must be consistent with the output selection above. For example, LAN/TCP-IP data is always 8-bit wide. REG37(6:0)
Download sampling rate f_{ds}	Download sampling frequency BEFORE interpolation. Not applicable when the download output is directed to LAN. Used only when the data is pushed out to the next module. (see flow control). Ignored when data is pulled in by the external flow control. The download sampling rate f_{ds} is expressed as $f_{ds} / f_{clk_tx} * 2^{31}$, where f_{clk_tx} is the output (DAC) sampling frequency. The download sampling clock is generated with a numerically controlled oscillator (NCO) It is therefore affected by jitter uniform over the f_{clk_tx} period. Jitter can be alleviated by selecting a power of two ratio f_{clk_tx} / f_{ds} To minimize jitter, select 1/2^n, for example x"80000000" for sampling rate = f_{clk_tx} [= no interpolation] x"40000000" for sampling rate = f_{clk_tx} /2 x"20000000" for sampling rate = f_{clk_tx} /4, etc REG38 (LSB) – REG41 (MSB)

Sampled output signal conditioning	
Parameters	**Configuration**
Output DAC sampling rate f_{clk_tx}	In many cases, the external Digital to Analog Converter requires a sampling clock. The COM-1806 generates such a programmable frequency clock on pins J8.A1 (options –A and -D) J8.A19/A20 (option –C) J8.B21/B22 (option –E) The DAC sampling rate is expressed as f_{clk_tx} = 125 MHz * M / (D * O)) where D is an integer divider in the range 1 - 106 M is a multiplier in the range 2.0 to 64.0 by steps of 0.125. Fixed point format 7.3 O is a divider in the range 2.0 to 128.0 by steps of 0.125. Fixed point format 8.3 Note: the graphical use interface computes the best values for M, D and O. Maximum f_{clk_tx} : 160 MHz REG71(6:0) = D REG72 = M(7:0) REG73(1:0) = M(9:8) REG74 = O(7:0) REG75(2:0) = O(10:8)
Interpolation factor	Download samples can be interpolated up to the output sampling rate f_{clk_tx} to smoothen the output waveform and thus reduce harmonics. Zero will bypass all interpolation stages. The maximum interpolation factor is the ratio of output sampling rate f_{clk_tx} to download sampling rate f_{ds} . The most accurate output waveform is obtained when that ratio is a power of 2. Use 2 to enable one half-band filter. Use 4 to enable two half-band filters

	Use 8 or above to enable both half-band filters and a CIC interpolation filter. Valid range 0 or 1 (no interpolation) to 2^{23} REG76 (LSB) – REG78 (MSB)
Output frequency translation (f_c)	The output signal can be shifted in frequency 32-bit signed integer (2's complement representation) expressed as $f_c * 2^{32} / f_{clk_tx}$ REG79 (LSB) – REG82 (MSB)
Output gain	This 16-bit gain setting is formatted as a 4.12 fixed-point number. The unit gain is thus 0x1000. Beware of possible saturation when increasing the output level. REG83 (LSB) – REG84 (MSB)

Network Interface	
Parameters	**Configuration**
MAC addresses LSB	In order to ensure the uniqueness of MAC addresses, users can define bits 7:1 through REG236(7:1). The MAC addresses upper bits are automatically tied to the nearly unique FPGA DNA_ID. REG236(7:0).
IP address	4-byte IPv4 address. Example : 0x AC 10 01 80 designates the default address 172.16.1.128 Note3 REG44 (MSB) – REG47 (LSB)
Subnet mask	REG48 (MSB) – REG51(LSB)
Gateway IP address	REG52 (MSB) – REG55(LSB)
IP multicast address	4-byte IPv4 address used for SDDS input stream. Example : 0x E1 00 00 01 designates address 225.0.0.1 Use 0.0.0.0 to signify that multicasting is not supported. REG56 (MSB) – REG59 (LSB)
Destination IP address	4-byte IPv4 address Destination IP address for UDP frames. Example : 0x AC 10 01 80 designates address 172.16.1.128 The new address becomes effective immediately (no need to reset the ComBlock). REG60 (MSB) – REG63(LSB)
UDP tx destination ports	Output UDP frames are routed to this user-defined port number: REG64(LSB) – REG65(MSB)

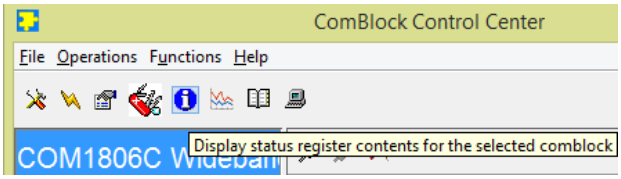
Note1: All upload transactions are enacted upon writing to temporary control register REG25 [use the SRT command. See API].

Note2: All download transaction are enacted upon writing to temporary control register REG35 [use the SRT command. See API].

Note3: Some changes are enacted upon reset or writing to the last control register (REG84).

Monitoring

Status registers



Status registers (SREG) are read-only.

Parameters	Monitoring
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-7 Properly operating hardware will result in the following sequence being displayed: SREG0-SREG7 = 01 F1 1D xx 1F 93 10 22
Clocks status	SREG8(0): 1 when frequency reference (TCXO or external 10 MHz) is present SREG8(1): 25 MHz PLL lock SREG8(2): 125 MHz PLL lock SREG8(3): Tx sampling clock PLL lock SREG8(4): Rx sampling clock PLL lock
Memory status	SDRAM memory ready SREG8(6)
Input sampling rate	The input sampling rate is measured and displayed here. The frequency measurement accuracy is a function of the internal clock stability. The measurement is expressed in Hz. SREG9 (LSB) – SREG12(MSB)
External gain (controlled by external AGC)	SREG13 (LSB) SREG14(3:0) (MSB)
SDRAM write pointer address	Current SDRAM write pointer address. Used to monitor the upload progress. When finished, the write pointer will point to the last address written to. Unit: number of SDRAM 64-bit words. SREG15 (LSB) – SREG18 (MSB)
SDRAM read pointer address	Current SDRAM read pointer address. Used to monitor the download progress. When finished, the read pointer will point to the last address read. Unit: number of SDRAM 64-bit words. SREG19 (LSB) – SREG22 (MSB)
Upload checksum	16-bit checksum obtained by summing all 16-bit words uploaded to the SDRAM. Wait until the upload completion to read this checksum. SREG23 (LSB) – SREG24 (MSB)
Download checksum	16-bit checksum obtained by summing all 16-bit words downloaded from the SDRAM. Wait until the single download completion to read this checksum. The download checksum should match the upload checksum if the sizes and start addresses match for the upload and the single download. Does not work with continuous download. SREG25 (LSB) – SREG26 (MSB)
Saturation	Saturation in the output signal conditioning path. 0 when no saturation. These flags are reset upon reading this status register. SREG27
TCP-IP Connection Monitoring	
Parameters	**Monitoring**
MAC address	Unique 48-bit hardware address (802.3). In the form SREG32:SREG33:SREG34:…:SREG37
TCP-IP server connection status	Bit 0 = port 1028 (M&C) connected Bit 1 = port 1024 (upload data) connected Bit 2 = port 1026 (download data) connected 1 for connected to a remote client, 0 otherwise SREG38(2:0)

Note: reading status register SREG7 latches multi-byte status words.

ComScope Monitoring

Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. Click on the button to open the ComScope panel.

The COM-1806 signal traces and trigger are defined as follows:

Trace 1 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Input signal I-channel	8-bit signed (8MSB)	Input sampling rate	512
2: Input signal (I-channel) after AGC, frequency translation, decimation	8-bit signed (8MSB)	Input sampling rate/R	512
3: Replay signal (I-channel) before output conditioning	8-bit signed (8MSB)	Output sampling rate	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: Input signal Q-channel	8-bit signed (8MSB)	Input sampling rate	512
2: Input signal (Q-channel) after AGC, frequency translation, decimation	8-bit signed (8MSB)	Input sampling rate/R	512
3: Replay signal (Q-channel) before output conditioning	8-bit signed (8MSB)	Output sampling rate	512
Trigger Signal	**Format**		
1: UPLOAD_TRIGGER	Binary		

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clkp} processing clock as real-time sampling clock.

In particular, selecting the f_{clkp} processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.

Operation

Upload from a file

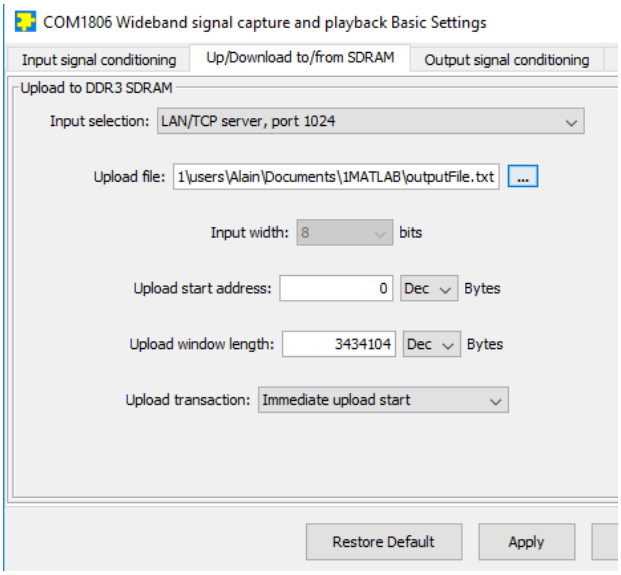
Objective: transfer a file contents into SDRAM memory.

Step 1: Create a file containing the data samples.

The file can be binary (see the file format section on how to pack samples into the binary file) or text file with two tab-delimited columns of 16-bit signed integers (i.e. in the range –32768 to +32767). The GUI automatically performs the conversion from tab-delimited text to binary prior to storage in SDRAM.

Step 2: Using the ComBlock Control Center (Graphical User Interface). Highlight the COM-1806 and click the *Settings* button. Select the up/download tab and select

- Transfer medium (LAN TCP)
- File location
- Start upload address: where the first byte will be stored. Must be an integer multiple of 64 bits.
- Upload window length: the actual length will be automatically adjusted if the file size is smaller than the specified window length.
  Note: in the case of an input text file, the upload window length value shown is the text file size. However, the actual number of bytes uploaded will be computed after text to binary conversion. An upload completion message will show the actual upload window length.
- Upload transaction = Immediate upload start.



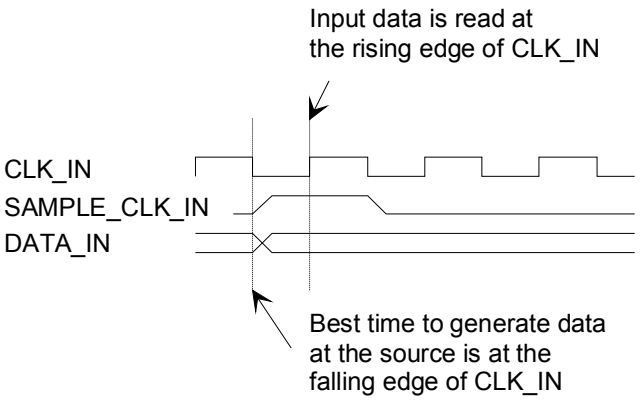
Step 3: To start the upload, simply click on the Apply button. The percentage of completion will be displayed at the bottom of the panel.

Note: when using custom TCP client software (i.e. not the GUI) to upload a file, please pad the transferred file to reach a size multiple of 64 bytes (512 bits).

Upload from a sampled input signal

An input waveform is typically represented by a series of 16-bit precision real or 2*16-bit precision complex samples. Complex samples can represent a near-baseband (zero center frequency) waveform with both In-phase (I) and Quadrature (Q) components. Real samples can represent an intermediate frequency (IF) signal through IF undersampling.

At the interface, input samples are supplied with a synchronous clock and an enable signal. The samples are read at the rising edge of the synchronous clock CLK_IN when the enable signal SAMPLE_CLK_IN is high.



The maximum input sampling rate is 125 MHz.

Input samples can be read through the right or left connector depending on the firmware version currently active (see firmware options).

These interfaces provide a seamless connection with several other ComBlock modules, including RF receivers and Analog-to-Digital converters.

The COM-1806 is capable of providing a low-jitter sampling clock to these external modules if needed. Its frequency is programmable.

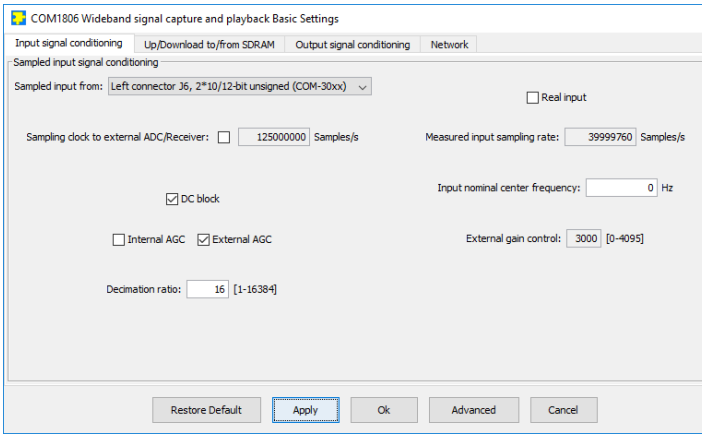
Input samples subsequently undergo user-configured signal conditioning such as

- DC bias removal
- Internal AGC
- External AGC
- Frequency translation
- CIC decimation
- Half-band filtering

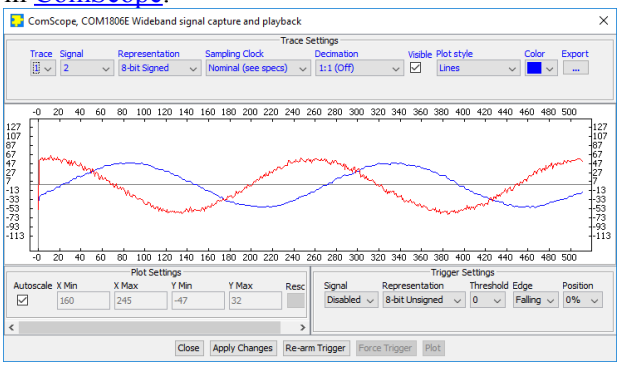
The external AGC controls an external receiver gain. It can be frozen at a user-selected gain level or set to automatic.

Depending on the input signal bandwidth, decimation can be used to reduce the occupied space in SDRAM memory. To prevent aliasing, decimation is always preceeded by anti-aliasing low-pass filters:
Decimation ratio 1: no filtering, no decimation
Decimation ratio 2: one half-band filter
Decimation ratio 4 and above: one CIC decimation filter followed by a half-band filter.

The input signal selection and conditioning is configurable via the panel shown below:

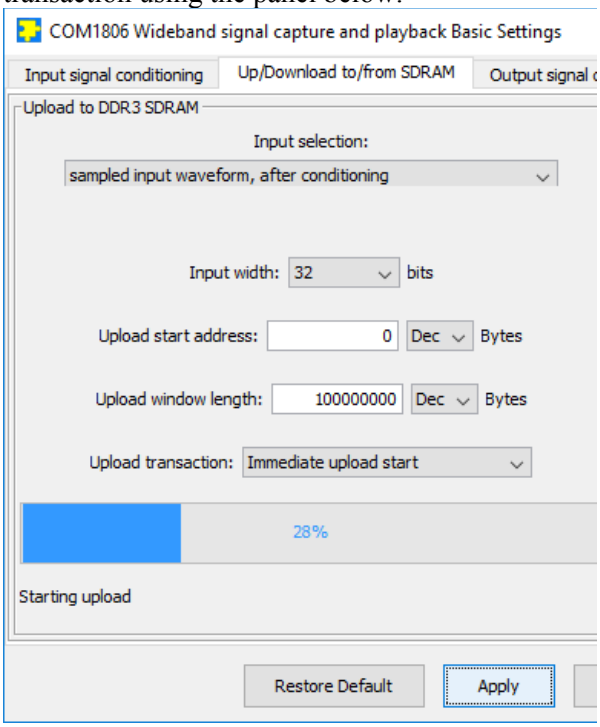


The complex input signal can be visualized, both before and after input conditioning, using the built-in ComScope.



Comscope example: input RF signal after input conditioning, displayed as baseband I/Q signals.

Finally, the user can configure and start an upload transaction using the panel below:



Upload from digital inputs

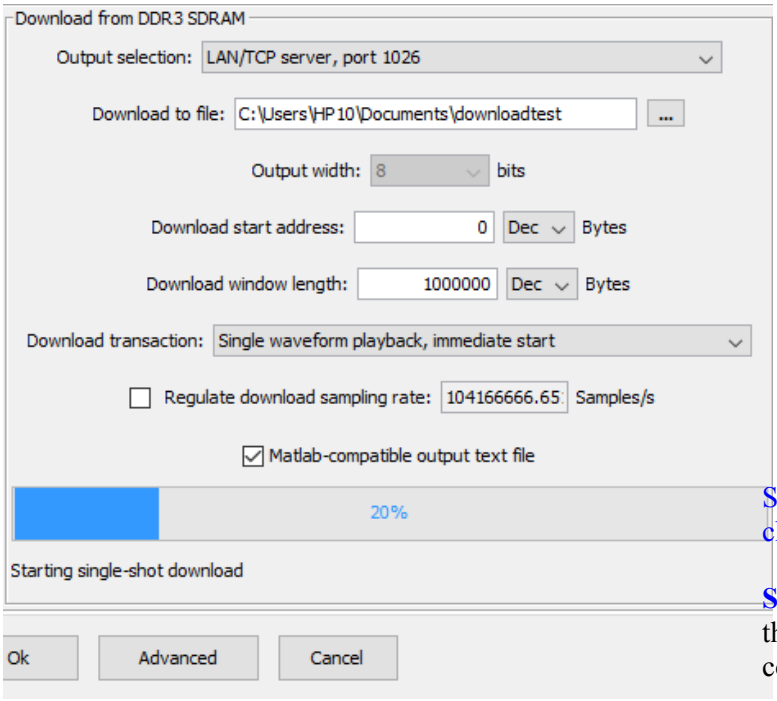
Up to 64 bits can also be captured from the right connector. Unlike the waveform samples above, these raw bits do not undergo any signal conditioning.

The user can select to read 1,2,4,8,16,32 or 64 input bits at each rising edge of the clock when the enable bit is high.

Download to a file

Objective: transfer the SDRAM contents to a file.

This transaction is controlled through the panel below:



The SDRAM contents can be transferred 'as is' to a binary file.

The contents can be also formatted as a two-column, tab-delimited text file representing complex 2*16-bit signed samples. A single Matlab 'load filename' command is sufficient to load the text file into Matlab for subsequent plotting and processing.

Download to a sampled output signal

Step 1: Using the ComBlock Control Center, configure the download parameters:

- The data to be downloaded can be segmented into distinct windows. A window can be the entire SDRAM memory or a fraction thereof. The download window is defined by its start address and a window length.

- Flow control: the download clock can be controlled by an internal numerical oscillator (data is "pushed out"), or by an external clock SAMPLE_CLK_REQ_IN which typically originates from the module to which data is sent (data is "pulled out").

Save the entries above by clicking on the "Apply changes" button before starting any download.

Step 2: Using the ComBlock Control Center, start the download mode by selecting single run or continuous run. Press the Apply button.

Memory segmentation

Upload and download transactions are fully independent:
Upload and download transactions can be simultaneous or can be scheduled one after the other for a store and forward application.
The upload area in SDRAM is fully independent of the download area. For example, upload can use the lower half of the SDRAM while download uses the upper half.

LAN

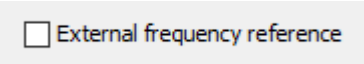
The COM-1806 acts as a TCP-IP server. It listens to port 1024 (upload), port 1026 (download) and port 1028 (Monitoring & Control). The remote TCP client (PC) must first establish a connection before data is transferred over the TCP connection.

The COM-1806 also exchanges UDP frames. It listens to port 1025 (upload) and port 1029 (reboot).

Data transfer over the Gigabit Ethernet LAN can use the TCP protocol (at speed up to 450 Mbits/s) or the UDP protocol (at speed up to 950 Mbits/s).

Frequency reference

By default, the COM-1806 uses a VTCXO as frequency reference for generating the output sampling rate and translation frequencies. This crystal is subject to a typical error of about 5ppm over temperature, aging and initial tolerance. Higher precision is achievable by injecting a high-stability 10 MHz frequency reference in the J6 SMA connector. The internal-vs-external frequency reference selection is software-controlled:



Operation with the external frequency reference requires that the external 10 MHz signal be present at power up.

File format

Upload and download samples files are either binary or ASCII text files. In order to make efficient use of the SDRAM memory space, the GUI will make the conversion from ASCII input text file (when selected by the user) to binary (to the SDRAM), and vice versa. For maximum upload and download speeds of very large files, binary files are preferred.

Example of Matlab .m code to write a complex Matlab array (si,sq) to a binary file before upload:

```
nrows = length(si);
interleaved = zeros(nrows*2, 1);
interleaved(1:2:2*nrows-1) = si;
interleaved(2:2:2*nrows) = sq;
fid1 = fopen('input.bin','w');
fwrite(fid1,interleaved,'integer*2');
fclose(fid1);
```

Example of Matlab .m code to generate a tab-delimited text samples file:

```
[fid_o1,msg]=fopen('input.txt','w');
if(fid_o1 == -1)
  disp('cannot open dest file');
end
for i = 1:length(si)
  fprintf(fid_o1,'%d\t%d\r\n',
si(i),sq(i));
end;
fclose(fid_o1);
```

where the complex signal is represented by its real si and imaginary sq components.

Example of Matlab .m code to read an output binary file into a Matlab complex array s:

```
fileID = fopen('com1806.bin');
a = fread(fileID,
[2,Inf],'int16',0,'b');     % big
endian ordering
% a(1,) is the real part
% a(2,) is the complex part
s = complex(a(1,:),a(2,:));
fclose(fileID);
```

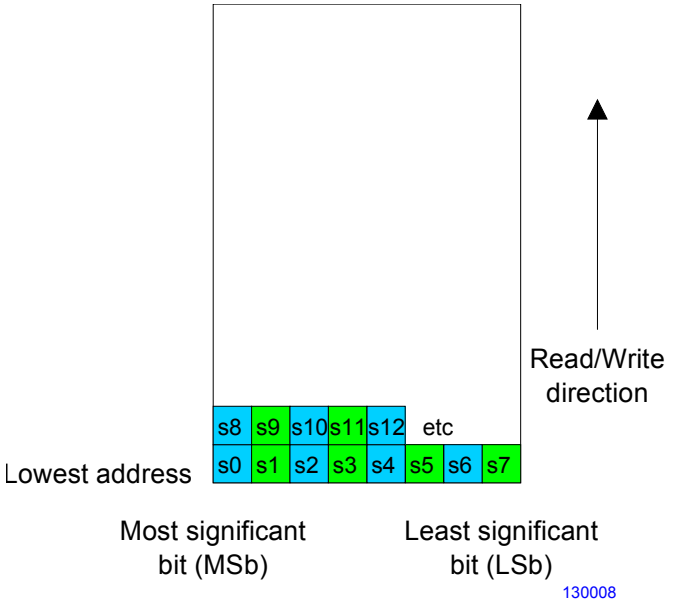
Example of Matlab .m code to load an output tab-delimited text file into a Matlab complex array s:

```
load output.txt;
s = complex(output(:,1),output(:,2));
plot(output(:,1); % plot real
```

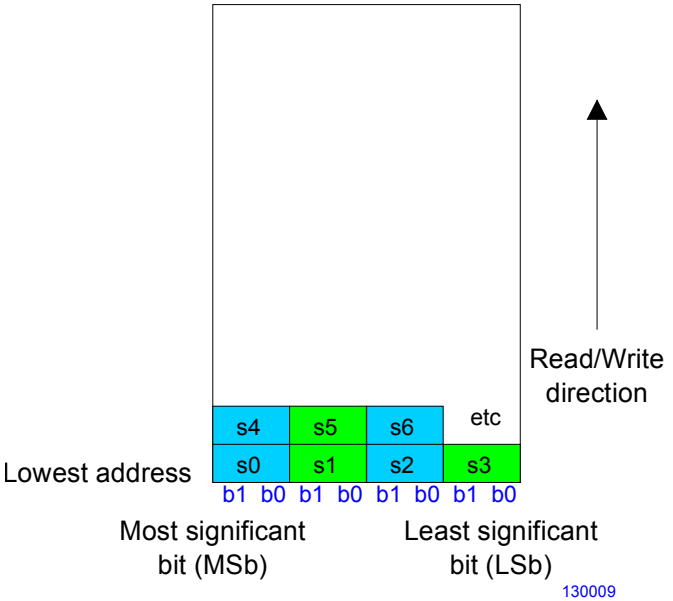
The rules for packing binary files are as follows:

- Samples are stored sequentially in increasing address locations.
- Most significant bit of the most significant byte first (i.e. at the lowest memory address).
- In complex samples, I (real) component is first, before Q (imaginary) component.

The diagrams below illustrates how various sample widths are stored in a binary file: S_i indicate the sample order, whereas b_i indicates the bit order within a sample.

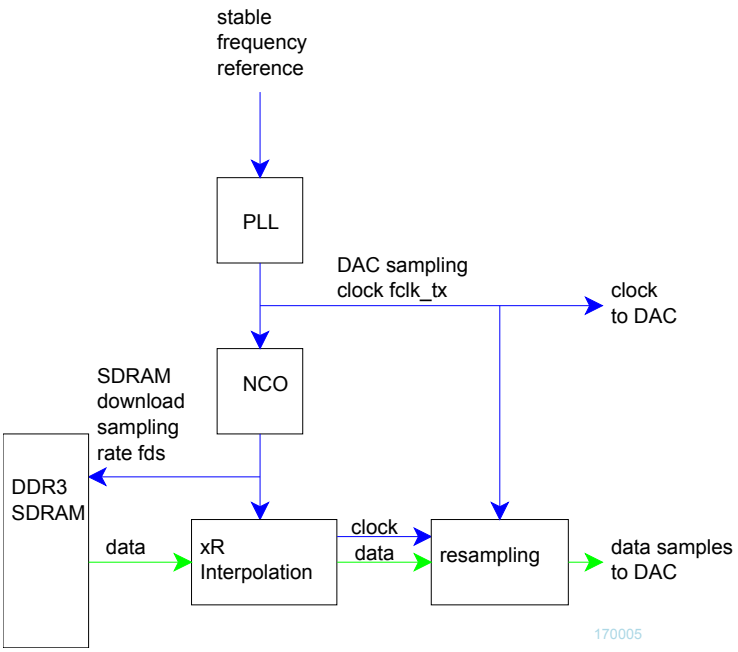


1-bit wide samples file format



2-bit wide samples file format

etc.



Output flow control

There are three controls affecting the speed at which output samples are sent to an external Digital-to-Analog Converter (DAC):

1. the DAC sampling rate f_{clk_tx} is generated by an internal PLL locked onto a stable frequency reference (whether internal VCTCXO or external 10 MHz). Programming steps are 1% or better.
2. the SDRAM download sampling rate f_{ds} is generated by a numerically controlled oscillator with very fine (f_{clk_tx} /2^{31}) steps. Generally, the download sampling rate is chosen to match the upload sampling rate.
3. Downloaded samples can be subsequently interpolated by a integer factor R. Naturally the following contraint must be met:
   $f_{ds} * R \leq f_{clk_tx}$ Naturally

The diagram below illustrates these output flow controls:

Options

Several interface types are supported through multiple firmware options. All firmware versions are on the supplied CD-ROM and can also be downloaded from
http://www.comblock.com/download.html

Changing the firmware option requires loading the firmware once using the ComBlock control center, then switching between the stored firmware versions The selected firmware option is automatically reloaded at power up or upon software command within 18 seconds

Option	Definition
-A	J8 right connector: 2*12-bit unsigned (offset binary) output samples. This interface is compatible with the COM-2001 dual 10-bit DACs.
-B	J8 right connector: 2*12-bit input samples. Input compatible with COM-30xx receivers
-C	J8 right connector: 2*16-bit output samples, 2*12-bit input samples. This interface is compatible with the COM-3504 dual Analog<->Digital Conversions.
-D	J8 Right connector: 1 to 64-bit raw binary output
-E	J8 Right connector : 2*16-bit LVDS output samples. This interface is compatible with the COM-4009 broadband RF modulator.

Troubleshooting

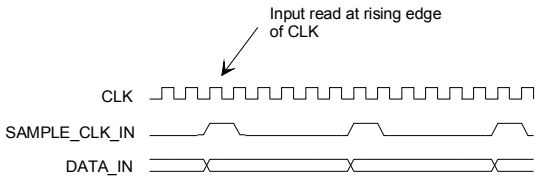
1. The module is performs self-checks at power up. Click on to display the status registers. Properly operating hardware will result in the following sequence being displayed: SREG0-SREG7 = 01 F1 1D xx 1F 93 10 22.
2. Check status register SREG4 bits 0 – 5: if not 111111, the power supply voltage may be outside the nominal range of 4.9 to 5.5V.
3. Check status register SREG8 bit 6: if not '1', the SODIMM memory underneath the module may be absent or not seated properly.
4. Verify the DDR3 memory integrity by comparing the checksums of an upload transaction and the matching download transaction. Compare SREG23/SREG24 with SREG25/SREG26. These 16-bit checksums should match.

Recovery

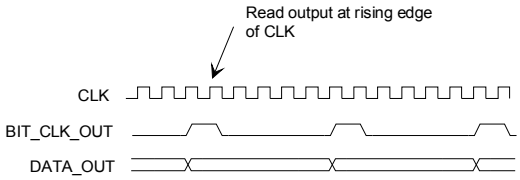
This module is protected against corruption by an invalid FPGA configuration file (during firmware upgrade for example) or an invalid user configuration. To recover from such occurrence, connect a jumper in J3 prior and during power-up. This prevents the FPGA configuration and restore communication. Once this is done, the user can safely re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center.

Timing

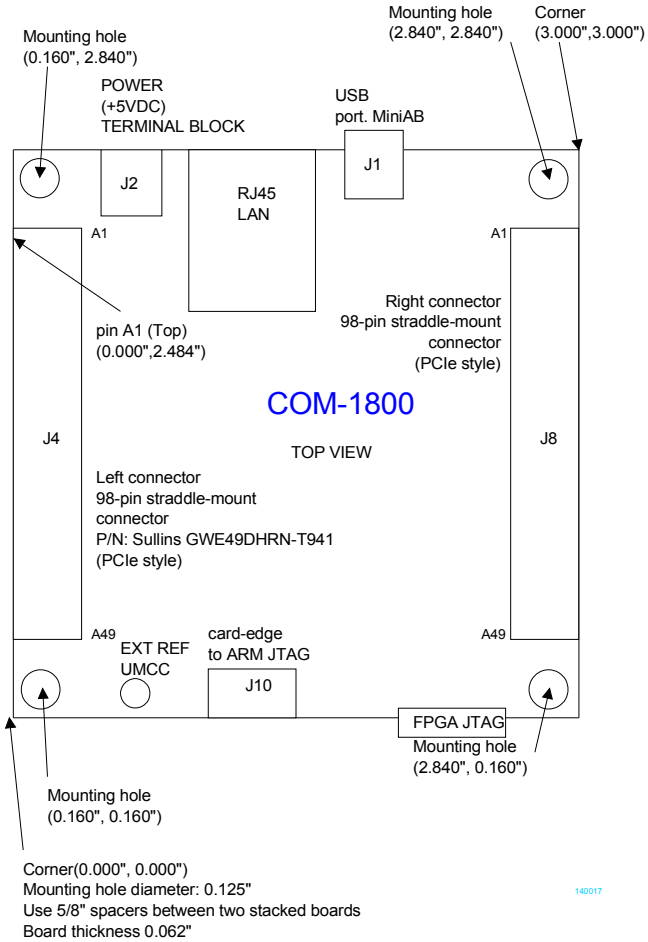
Input



Output



Mechanical Interface



Schematics

The board schematic is available on-line at
ComBlock.com/download/com_1800schematics.pdf

Electrical Interface

Inputs

Input Module Interface	Definition
TCP IP servers over gigabit Ethernet LAN (GbE)	10/100/1000 Mbps Ethernet LAN through RJ45 connector. Supports auto MDIX to alleviate the need for crossover cable. The COM-1806 comprises two TCP servers, one for uploading data at port 1024, the other for downloading data at port 1026. Each TCP server listens for a connection request from a remote TCP client (PC). Once the TCP connection is established, the client can send or receive byte-wide data to or from the COM-1806. No programming is needed when using the supplied ComBlock Control Center. Custom applications can be developed using standard TCP socket programming. A third TCP server at port 1028 is used for the sole purpose of monitoring and control.
USB 2.0	Mini-USB connector Type AB Full speed / Low Speed The COM-1806 acts as a USB device when connected to a PC. Using the supplied USB driver (Windows only) and the ComBlock Control Center, the user can perform all monitoring and control functions. The USB connection cannot be used to upload or download data.
EXT REF	Optional external 10 MHz frequency reference to attain higher frequency stability than the built-in VCTCXO oscillator. Sinewave, clipped sinewave or squarewave. UMCC female connector (J6). Input is AC coupled.

	Minimum level 0.6Vpp. Maximum level: 3.3Vpp.
UPLOAD_ TRIGGER	External trigger pulse to start an upload transaction. When the external trigger mechanism is enabled by software, the requested upload transaction will be placed on hold until the falling edge of this signal. This signal is internally pulled low. Its use is optional.
DOWNLOAD_ TRIGGER	External trigger pulse to start a download transaction. When the external trigger mechanism is enabled by software, the requested download transaction will be placed on hold until the falling edge of this signal. This signal is internally pulled low. Its use is optional.

Power Interface	4.75 – 5.25VDC. Terminal block. The maximum current consumption is 1050mA (1GB)

Use of the COM-1806 requires an oversized power supply capable of supplying a peak current of 2A for a very short period (5ms). Hook-up cable should be 18AWG or thicker to minimize voltage drop between power supply and terminal block.

Absolute Maximum Ratings

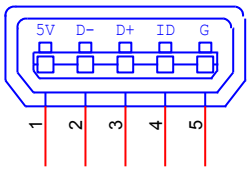
Supply voltage	-0.5V min, +6V max
40-pin connector inputs (LVTTL)	-0.5V min, +3.6V max
40-pin connector inputs (LVDS)	-0.5V min, +2.8V max

Inputs are NOT 5V tolerant!

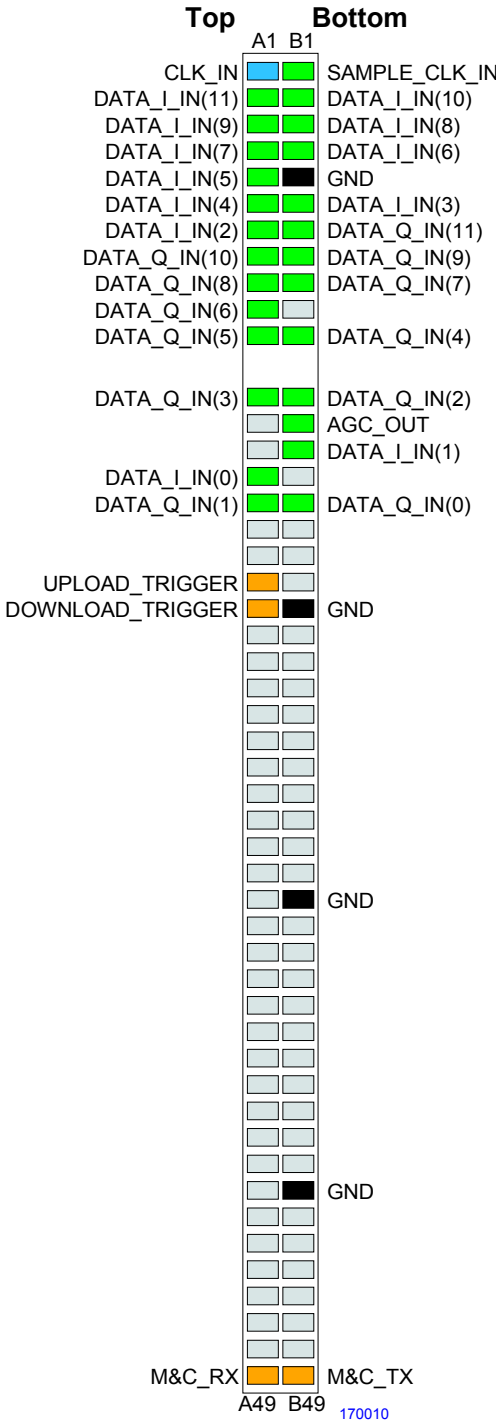
Pinout

USB

The USB port is equipped with a mini type AB connector. (G = GND). The COM-1806 acts as a USB device.

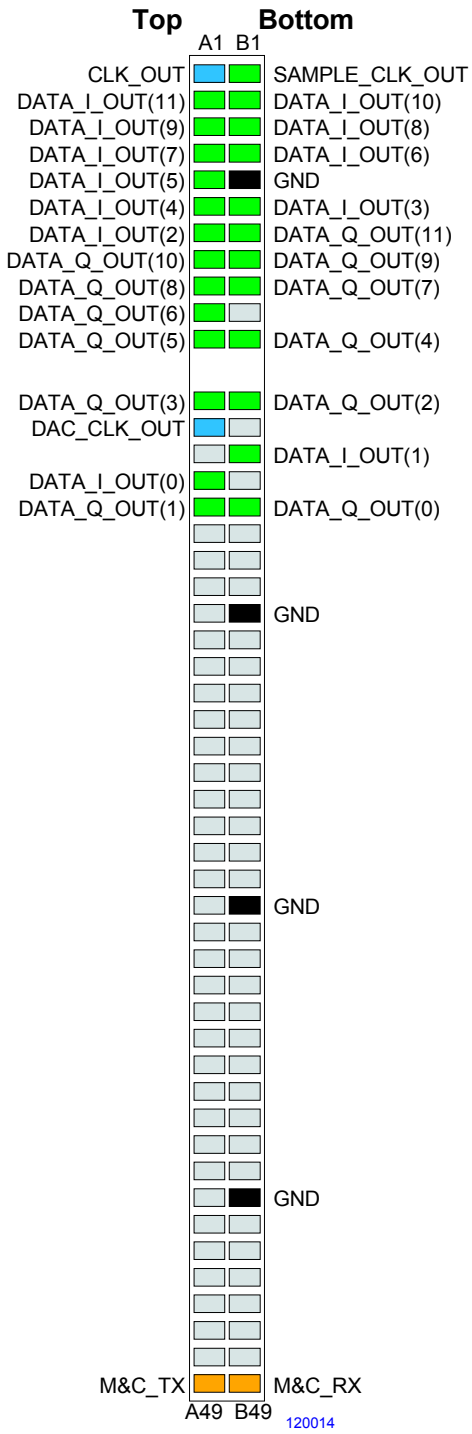


Left Connector J4

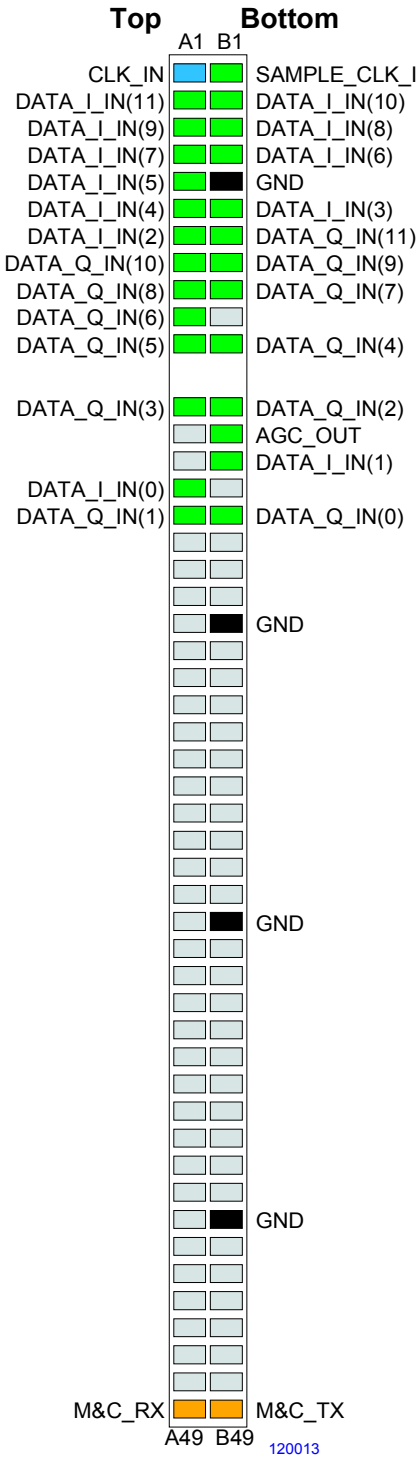


Input compatible with COM-30xx receivers.

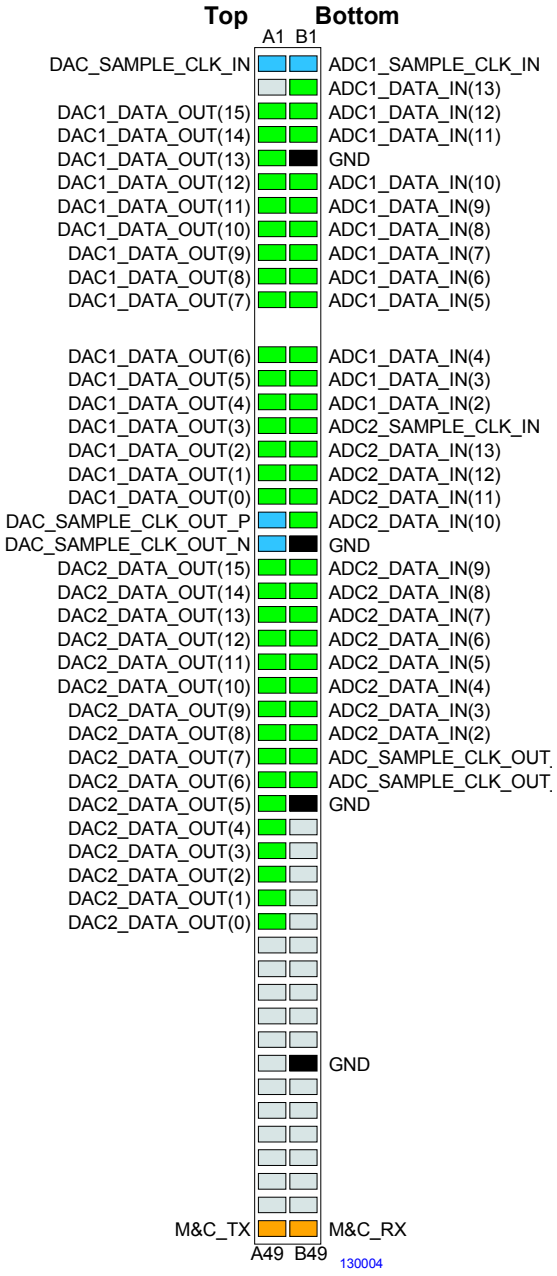
Right Connector J8



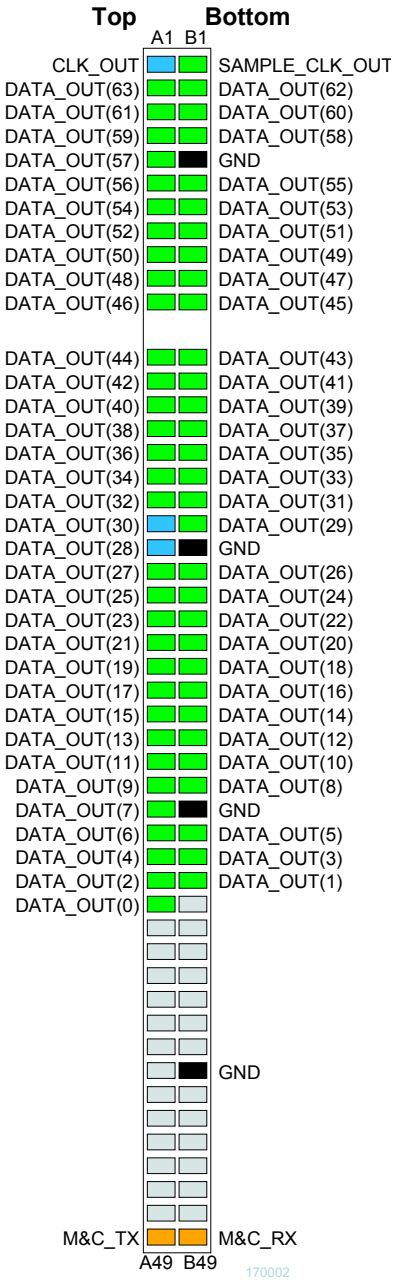
Firmware Option **-A** 2*12-bit output samples. This interface is compatible with the COM-2001 dual 10-bit DACs.



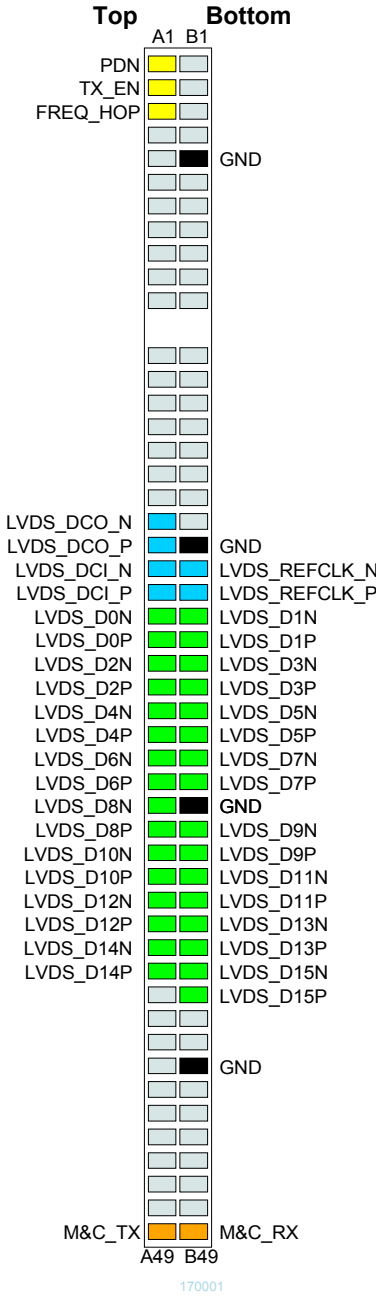
Firmware Option **-B** 2*12-bit input samples.
Input compatible with COM-30xx receivers.



Firmware Option **-C** 2*16-bit output samples, 2*12-bit input samples. This interface is compatible with the COM-3504 dual Analog<->Digital Conversions.



Firmware Option **-D** 1-64bit raw output



Firmware Option **-E** 2*16-bit output samples (2's complement). This interface is compatible with the COM-4009 RF modulator

I/O Compatibility List

(not an exhaustive list)

Left connector (J4)
COM-30xx RF/IF/Baseband receivers for frequencies ranging from 0 to 3 GHz.
Right connector (J8)
COM-2001 Digital-to-Analog Conversion, Baseband 2*10-bit 125 MSamples/s
COM-3504 Dual Analog <-> Digital Conversions 2*16-bit 250 MSamples/s
COM-30xx RF/IF/Baseband receivers for frequencies ranging from 0 to 3 GHz.
COM-1800 FPGA + ARM development platforms
COM-4009 digital to [400MHz – 4.4GHz] broadband RF modulator

Configuration Management

This specification is to be used in conjunction with VHDL software revision 1 and ComBlock Control Center revision 3.12q and above.

ComBlock Ordering Information

COM-1806-1GB WIDEBAND SIGNAL CAPTURE & PLAYBACK 1GB

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