COM-1808SOFT_TX DVB-S2 Transmitter VHDL source code overview / IP core

Overview

The COM-1808SOFT_TX is a DVB-S2 compliant transmitter written in generic VHDL.

The entire **VHDL source code** is deliverable. It is portable to a variety of FPGA targets.

Key features and performance:

- Flexible programmable features:
  - input streams attributes (dynamic: can change every BBFRAME): 16200/64800b frame length, FEC encoding rate, modulation type
  - input streams attributes: stream type (transport stream, generic stream packetized, generic bit stream), user packet length, input stream synchronization, null packet detection
  - modulation attributes: symbol rate, frequency offset, SRRC filter roll-off, common to all input streams.
- Provided with IP core:
  - VHDL source code
  - GNU radio project and Matlab conversion .m program for generating DVB-S2 waveforms.
  - VHDL testbench
  - PRBS11 test sequence generator, AWGN noise generator

Supported features

Feature	Supported
Inputs	• Single or multiple MPEG Transport Stream. 188-Byte fixed length frames, Byte-wide. • Single or multiple Generic Stream (packetized or continuous). Byte-wide. • BBFRAMEs at the mode adaptation input interface.
Payload bit rate example	858 Mbits/s (8-PSK, rate 9/10, Xilinx Ultrascale+ -2)
Input stream synchronizer	Yes
Null packet deletion	Yes
Error correction encoding	LDPC + BCH
Encoding rate	1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
Coding and modulation	CCM, VCM, ACM
FEC frame	normal (64800 bits) short (16200 bits)
Modulation	QPSK, 8-PSK, 16APSK, 32APSK
Maximum modulation symbol rate (Xilinx ultrascale+ -2 speed grade)	318 MSymbols/s 636 MSamples/s
SRRC filter roll-off	0.35, 0.25 and 0.20
Output	complex (I,Q) baseband samples, 16-bit precision. DDR

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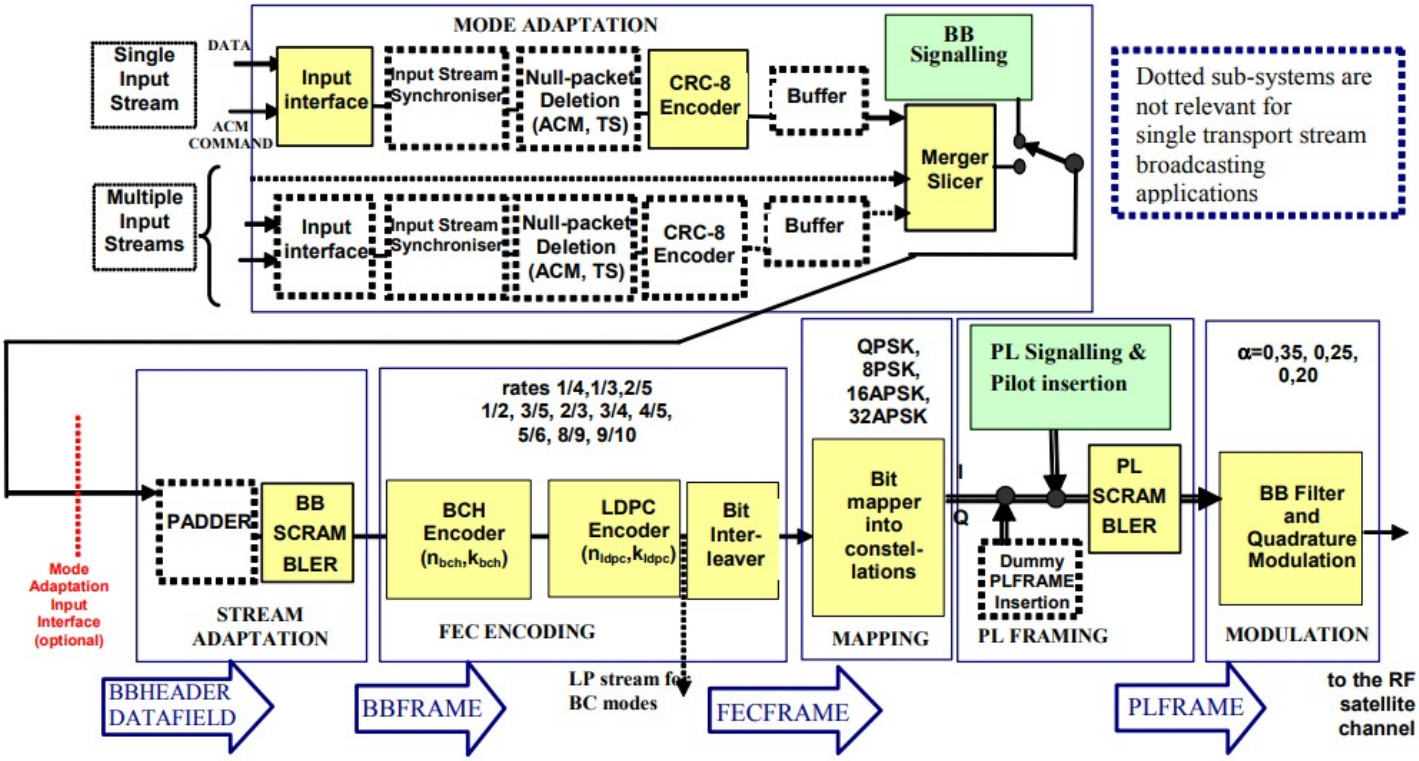


Figure 1: Functional block diagram of the DVB-S2 System

Extract from reference document [1]

Configuration

Synthesis-time configuration parameters

The following constants are user-defined in the *DVBS2_TX.vhd* component generic section or *DVB2_TX_PKG* package section prior to synthesis. These parameters generally affect the size of the transmitter embodiment.

Synthesis-time configuration parameters	Configuration
EXT_MODE_ADAPT	Optional mode Adaptation input interface with in-band signaling. When enabled, the input streams interface is disabled. See [1] Annex I.2
N_TS	Number of parallel input streams (transport streams or generic streams)
AWGN_INST	Additive White Gaussian Noise generator instantiation (1). (0) during operations to save space in FPGA (and to increase clock speed.
POWER_ MEASUREMENT_INST	Signal and noise power measurements at the transmitter output. 1 to instantiate, 0 otherwise

Run-time configuration parameters

The user can set and modify the following controls at run-time through the top level component interface:

Modulator Parameters (common to all input streams)	Configuration
MOD_SYMBOL_RATE (32:0)	Symbol rate expressed as 2^32* symbol rate / DAC sampling rate f_{CLK_TXg} Maximum symbol rate = DAC sampling rate
MOD_CENTER_FREQ (31:0)	Modulated signal center frequency. Expressed as 2^32 * fc/ f_{CLK_TXg}
MOD_RO(2:0)	Square root raised cosine filter roll-off factor: 0= 35%, 1 = 25%, 2 = 20%, 4 = 15%, 5 = 10%, 6 = 5%
MOD_CONTROL(7:0)	bit 0: spectrum inversion enabled (1) or not (0) bit 1: unmodulated carrier output test mode
MOD_SIGNAL_ SCALING(15:0)	Output amplitude scaling factor. 16-bit unsigned
AWGN_SIGNAL_ SCALING(15:0)	Additive White Gaussian Noise level (amplitude) 16-bit unsigned

Individual stream configuration, fixed at reset	Configuration
STREAMS_ TYPE (1:0)	TS/GS field (2 bits): Transport Stream Input or Generic Stream Input (packetized or continuous) 11 = transport stream, 188B frame 00 = generic stream, packetized, user-defined fixed length UPL 01 = generic bit stream
STREAMS_UPL (15:0)	User Packet Length in bits, in the range 0 to 65 535 fixed 188 Bytes for transport stream, up to 65535 bits for generic stream If UPL is greater than 65535 bits, use generic bit stream. For packetized stream, UPL includes the sync byte
STREAMS_ ISSYI	Input stream synchronization indicator. See [1] annex D.2
STREAMS_NPD	Null packet detection. Generally enabled for transport stream and/or ACM

Note: when using the optional mode adaptation input interface, these configuration parameters are embedded within the 10-Byte header of the input BBFRAME.

Individual stream configuration, dynamic (can change every BBFRAME)	Configuration
STREAMS_FL (1:0)	Frame length 0: DVB-S2 normal frame n_{ldpc}=64800 1: DVB-S2 and DVB-S2X short frame n_{ldpc}=16200 2: DVB-S2X medium frame n_{ldpc}=32400
STREAMS_ MODULATION (5:0)	Constellation 1: DVB-S2 QPSK 2: DVB-S2 8-PSK 3: DVB-S2 16-APSK 4: DVB-S2 32-APSK
STREAMS_ CODING(4:0)	Coding rate (LDPC code identifier) 0: rate 1/4 or 1/5 [normal,short,medium frames] 1: rate 1/3 [normal,short,medium frames] 2: rate 2/5 [normal,short frames] 3: rate 1/2 [normal,short frames] 4: rate 3/5 [normal,short frames] 5: rate 2/3 [normal,short frames] 6: rate 3/4 [normal,short frames] 7: rate 4/5 [normal,short frames] 8: rate 5/6 [normal,short frames] 9: rate 8/9 [normal,short frames] 10: rate 9/10 [normal frames] 11: rate 11/45 [short,medium frames] 12: rate 4/15 [short frames] 13: rate 14/45 [short frames] 14: rate 7/15 [short frames] 15: rate 8/15 [short frames] 16: rate 26/45 [short frames] 17: rate 32/45 [short frames]

Note: when using the optional mode adaptation input interface, these configuration parameters are embedded within the 2-Byte transport header before each BBFRAME.

I/Os

General

Two independent clock domains are used in *DVBS2_TX.vhd*:

CLK for mode adaptation, BCH encoding, LDPC encoding and bit interleaving. These functions process 8-bit wide data samples.

CLK_TXg for modulation and DAC sampling interface. Because the output interface is DDR, the actual DAC sampling rate is twice the **CLK_TXg** frequency.

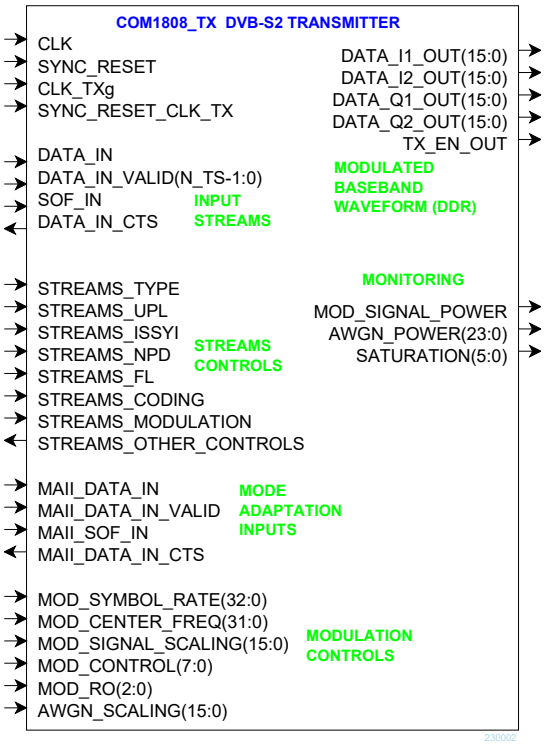
Of course, each clock timing period must be constrained in the constraint file (.xdc for Xilinx Vivado) associated with the project.

There is no need for inter-clock timing constraints between **CLK** and **CLK_TXg**. (use set_false_path tcl command in the constraint file).

These two clocks must be global clocks (i.e. use BUFG before supplying the clock to the transmitter).

Two sync resets (**SYNC_RESET** and **SYNC_RESET_CLK_TX**) must be supplied, one for each clock domain. The recommended use is to keep the resets high until both clocks are stable (i.e. PLL or MMCM locked).

Transmitter



Data Path

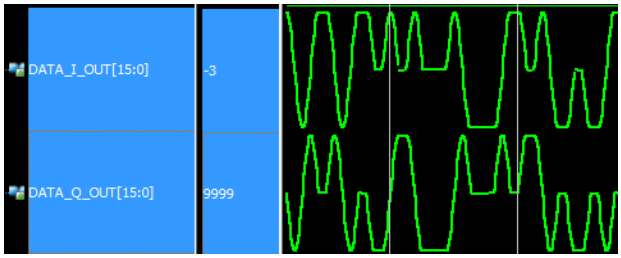
DATA_IN is an array of **N_TS** byte-wide input streams. Bit order: MSb first.

DATA_IN_VALID(N_TS-1:0): input.
1 CLK-wide pulses indicating that the associated **DATA_IN** stream input Byte is valid.

SOF_IN(N_TS-1:0): optional input Start Of Frame. 1 CLK-wide pulse. The SOF is aligned with **DATA_IN_VALID**. Required for transport streams and generic packetized streams.

DATA_IN_CTS: output.
Clear-To-Send flow control. '1' indicates that the transmitter is ready to accept another input byte. Thanks to an input elastic buffer, the data source is allowed to send a few more bytes after **DATA_IN_CTS** goes low, so timing is generally not critical.

DATA_I/Q_OUT(15:0): Modulated baseband output samples (I = in-phase, Q = quadrature). Double Data Rate output: two output samples every clock. Format: 2's complement (signed)



Operations

Baseband Frame Assembly

User packets are packed to completely fill the data field of the BBFRAME up to its kbch bit size. Thus, there is no need to add zero padding. The start of the data field is not necessarily aligned with the start of a user packet.

Multiple packetized streams

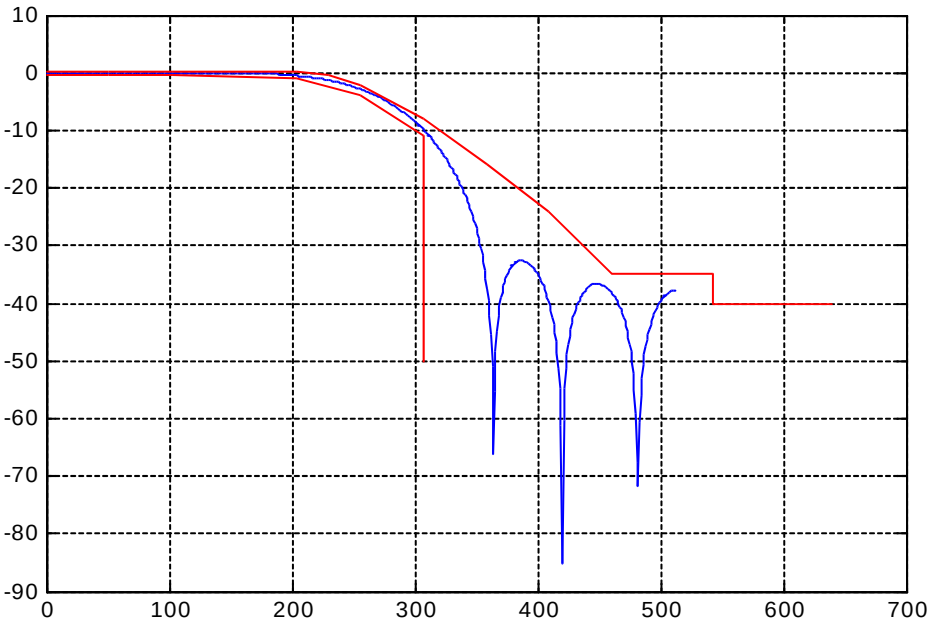
The following rules are used to pack user packets into BBFRAMEs:
- a given BBFRAME contains user packets from a single stream only
- the stream multiplexer uses a round-robin method to assign a stream to the next BBFRAME, provided there is enough data in the stream buffer to fill the kbch bits of the next BBFRAME.

Design considerations

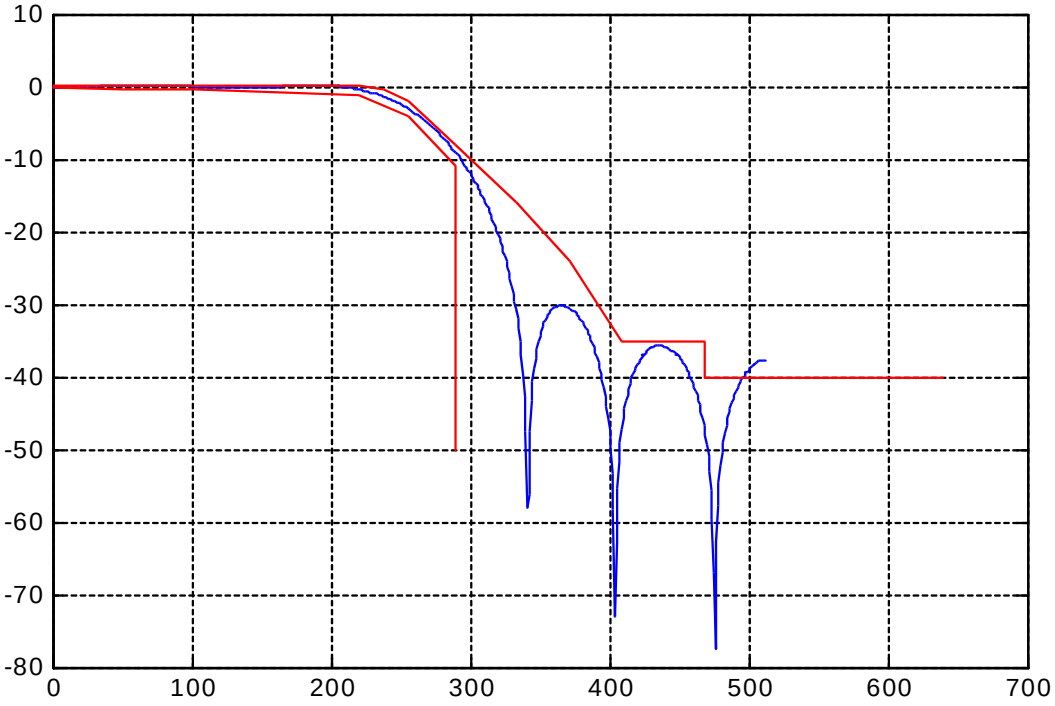
Channel Filter

The two parallel channel filters (processing the complex modulated samples) are implemented as 14-tap FIR filters. Compliance with the specified mask in [1] Appendix A is shown below. Note that some additional filter (either RF at the maximum symbol rate, or digital half-band filter at lower symbol rates are needed to guarantee low out-of-band levels).

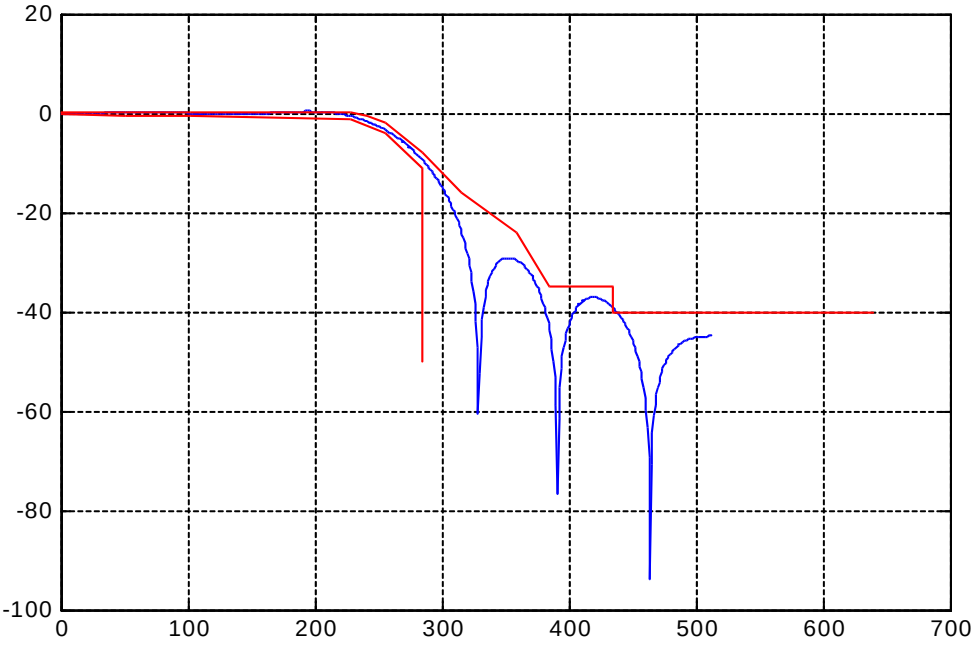
Alpha = 0.35



Alpha = 0.25



Alpha = 0.20



The Matlab program /matlab/dvbs2_firrcos.m is used to generate the FIR coefficients and verify compliance with the spectral mask

Software Licensing

This software is supplied under the following key licensing terms:

1. A nonexclusive, nontransferable license to use the VHDL source code internally, and
2. An unlimited, royalty-free, nonexclusive transferable license to make and use products incorporating the licensed materials, solely in bit stream format, on a worldwide basis.

The complete VHDL/IP Software License Agreement can be downloaded from
http://www.comblock.com/download/softwarelicense.pdf

Portability

The VHDL source code is written in generic VHDL and thus can be ported FPGAs from various vendors.

Configuration Management

The current software revision is 011224.

Directory	Contents
/doc	Specifications, user manual, implementation documents
/src	.vhd source code,.pkg packages, .xdc constraint files (Xilinx) One component per file.
/sim	VHDL test benches
/matlab	Gnuradio project and Matlab .m conversion file for generating stimulus files for VHDL simulation and for end-to-end BER performance analysis at various signal to noise ratios
/bin	.bit configuration files (for use with ComBlock COM-1800 FPGA development platform)

Project files:

Xilinx Vivado v2020 project files:
project_1vivado2020p2.xpr
project_1vivado2020p2.tcl

VHDL development environment

The VHDL software was developed using the following development environment:
Xilinx Vivado 2020 for synthesis, place and route and VHDL simulation

The entire transmitter project fits easily within a Xilinx Artix7-100T. Therefore, the ISE project can be processed using the free Xilinx WebPack tools.

Device Utilization Summary

Transmitter device utilization (no AWGN)
Device: Xilinx xcku5p-ffvb676-2-i

Resource	Estimation	Available	Utilization...
LUT	18145	216960	8.36
LUTRAM	138	99840	0.14
FF	10617	433920	2.45
BRAM	32.50	480	6.77
DSP	100	1824	5.48
IO	273	280	97.50
BUFG	2	256	0.78

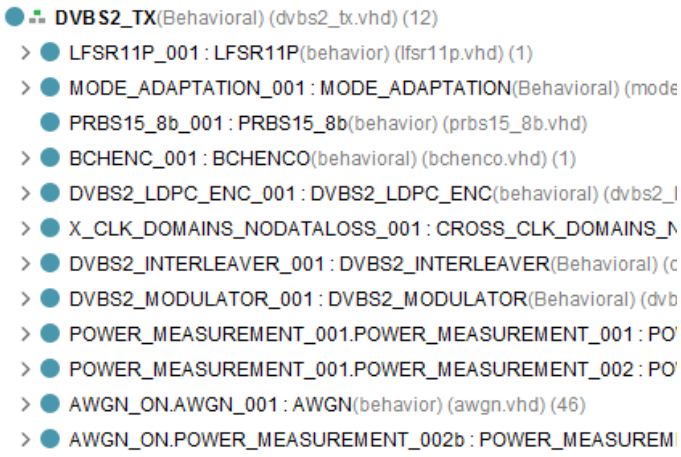
Clock and decoding speed

The entire design two global clocks CLK (encoding) and CLK_TXg (modulation). Typical maximum clock frequencies for representative FPGA families are listed below:

Device family	**Transmitter**
Xilinx Kintex7 ultrascale+ -2 speed grade	CLK_Txg: 318 MHz CLK: 345 MHz

VHDL components overview

Modulator top level



DVBS2_TX.vhd is the transmitter top level component. Inputs consist of one or several streams (transport, generic). The output is a DDR complex baseband modulated signal with two samples per CLK_TXg clock. The maximum modulation rate is thus f_{clk_TXg} symbols/s.

The *MODE_ADAPTATION.vhd* component implements [1] section 5.1, namely "Input Interfacing, Input Stream Synchronization (optional), Null-packet deletion (for TS input streams and ACM only), CRC-8 encoding for error detection (for packetized input streams only), input stream merging (for multiple input streams only) and input stream slicing in DATA FIELDs. Finally, base-band signaling is inserted, to notify the receiver of the adopted Mode Adaptation format. "

The *MODE_ADAPTATION_INPUT_INTERFACE* component handles a Byte-stream input from an external mode adaptation block. It is instantiated when **EXT_MODE_ADAPT** is enabled. See [1] Annex I.2.

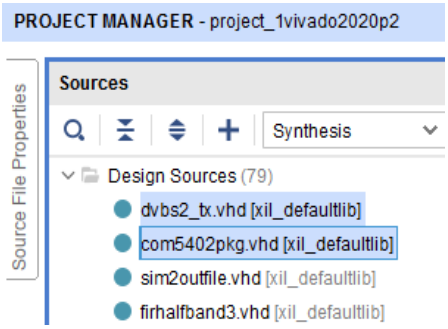
The *PRBS15_8B.vhd* component generates the BB frame scrambling sequence.

BCHENCO.vhd is the BCH error correction encoding (outer coding), as per [1] section 5.3.1.

SIGNED_SIN_COS_TBL3.vhd stores sine and cosine functions in ROM. It is used to convert phase to complex I/Q baseband output samples.

COM1808_TOP.vhd: is mostly a use example when the DVBS2 transmitter is implemented on a ComBlock COM-1800 FPGA development platform.

Note for Xilinx Vivado: when creating the project, the compile order is unimportant, except for the two highlighted files which may require a higher priority:



Ancillary components

LFSR11P.vhd is a pseudo-random sequence generator used for test purposes. It generates a PRBS11 test sequence commonly used for bit error rate testing at the receiving end of a transmission channel.

AWGN.vhd generates a precise Additive White Gaussian Noise. The noise bandwidth is 2*symbol rate.

BRAM_DP2.vhd is a generic dual-port memory, used as input and output elastic buffers. Memory is inferred (no Xilinx primitive is used).

INFILE2SIM.vhd reads an input file. This component is used by the testbench to read a modulated samples file generated by the `siggen_fsk1.m` Matlab program for various Eb/No and frequency offset cases.

SIM2OUTFILE.vhd writes three 12-bit data variables to a tab delimited file which can be subsequently read by Matlab (load command) for plotting or analysis.

VHDL simulation

VHDL testbenches are located in the /sim directory.

The `tb_dvbs2_tx.vhd` sends two transport streams through the transmitter to illustrate the streams multiplexing. The output consists of modulated complex baseband samples.

The `tb_dvbs2_tx2.vhd` sends a single DVBS2 generic packetized stream of length STREAMS_UPL with variable coding and modulation (VCM): coding and modulation change frequently. The output consists of modulated complex baseband samples.

The `tb_dvbs2_txrx.vhd` connects the transmitter and receiver back to back for end-to-end VHDL simulation. It's use should be restricted to symbol rates below CLK_TXg/8 as the coarse resampling between the CLK_TXg transmitter sampling clock and CLK_ADCg receiver sampling clock is too coarse for the higher symbol rates. The transmitter includes a built-in pseudo-random sequence generator and the receiver includes a built-in Bit Error Rate Tester.

GNU radio + Matlab simulation

GNU radio project(s) and Matlab programs are located in the /matlab directory.

The `dvbs2_tx312MS.grc` is a GNU radio configuration file to generate a DVB-S2 modulation waveform. It is used primarily to verify a receiver compliance with the DVB-S2 standard.

The `read_waveform.m` program opens a *waveform.dat* complex samples file generated by GNU radio, reformats it to 2 columns of signed integers 12-bit precision then saves it to the input.txt file. It can also add white Gaussian noise to the waveform as needed.

The `dvbs2_firrcos.m` matlab program helps selecting the minimum size FIR filter to comply with the standard spectral masks for various root raised cosine filter rolloff factors.

Reference documents

[1] DVB-S2 specifications, ETSI EN 302 307-1 V1.4.1 (2014-11)

[2] DVB-S2 Extensions (DVB-S2X) specifications ETSI EN 302 307-2 V1.1.1 (2015-02)

Acronyms

Acronym	Definition
ACM	Adaptive Coding and Modulation
AWGN	Additive White Gaussian Noise
CCM	Constant Coding and Modulation
CTS	Clear-To-Send flow control flag
DDR	Dual Data Rate
DVB	Digital Video Broadcasting
FPGA	Field Programmable Gate Array
GS	Generic Stream
GbE	Gigabit Ethernet
LSb	Least Significant bit in a word
MPEG	Moving Pictures Experts Group
MSb	Most Significant bit in a word
RF	Radio Frequency
SRRC	Square Root Raised Cosine (filter)
TS	Transport Stream
tx	Transmit
VCM	Variable Coding and Modulation

ComBlock Ordering Information

COM-1808SOFT_TX DVB-S2 transmitter, VHDL source code / IP core

ECCN: EAR99

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